GENERAL DESCRIPTION

MX1210 is a highly integrated current mode PWM controller, optimized for high performance, low standby power consumption and wide output voltage range PD adapter solutions. The circuit is as well compatible with cost effective offline flyback converter applications covering a wide output range.

At full loading, the IC operates in fixed frequency mode. When the loading goes low, it operates in Green mode with valley switching for high power conversion efficiency can be achieved in the whole loading range.

MX1210 offers complete protection coverage including cycle-by-cycle current limiting (OCP), over load protection (OLP), over temperature protection (OTP), output short current protection (SCP), output and VDD over voltage protection (OVP & VDD OVP). Excellent EMI performance is achieved with MAXIN proprietary frequency shuffling technique. The tone energy at below 22kHz is minimized to avoid audio noise during operation.

MX1210 is offered in SOT23-6 package.

Applications

Battery chargers

PD adapters

Wide output range adapters

Set-Top Box power supply

FEATURES

♦ Multi-Mode Operation

- ●65kHz fixed frequency mode @ Full Load
- ●Valley switching operation @ Green mode
- ●Burst Mode @ Light Load and No Load

♦Adaptive loop gain compensation with Iovp current detection

♦Ultra low operation current at light and no load

♦Internal OCP compensation for universal line voltage

♦Extend burst mode control for improved efficiency and low standby power

♦Power on soft start reducing MOSFET VDS stress

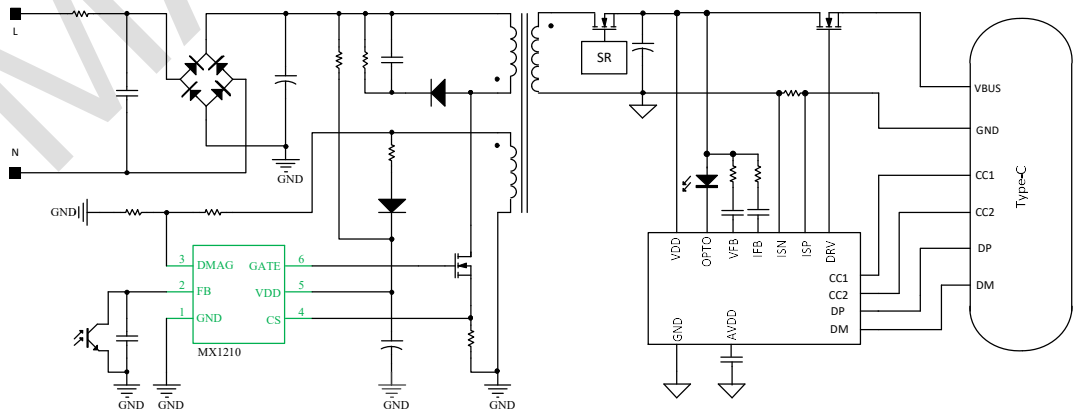
♦Frequency shuffling for EMI

♦Audio noise free operation

♦Comprehensive protection coverage

- ●VDD under voltage lockout with hysteresis (UVLO)
- ●Cycle-by-cycle over current protection (OCP) with auto recovery
- ●External over temperature protection (EXT_OTP)
- ●VDD over voltage protection
- ●Output over voltage protection
- ●Output short current protection (SCP) with auto recovery
- ●Brownout protection with auto recovery
- ●Output diode short protection with auto recovery

Typical Application



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General information

Ordering information

Part Number	Description
MX1210	SOT23-6，Halogen-free，RoHS

Package dissipation rating

Package	RθJA（℃/W）
SOT23-6	200

Absolute maximum ratings

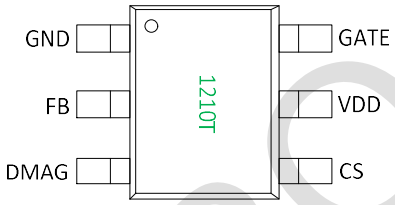
Parameter	Value
VDD DC supply voltage	60V
FB input voltage	-0.3 to 7V
CS input voltage	-0.3 to 7V
DMAG input voltage	-0.3 to 7V
Junction temperature T_J	-40 to 150℃
Ambient temperature T_A	-40 to 85℃
Storage temperature T_{STG}	-55 to 150℃
ESD(HBM)	±2.0kV
Leading temperature （soldering, 10secs）	260℃

Note: stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Recommended operating condition

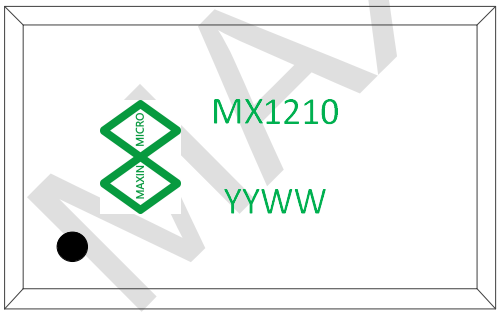
Symbol	Parameter	Range
VDD	VDD supply voltage	10-48V
PD	Power dissipation @TA=25℃	0.59W

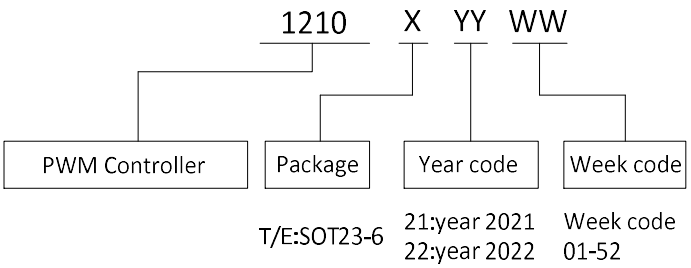
Terminal assignments



PIN NO.	PIN name	Description
1	GND	Ground pin.
2	FB	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and current-sense signal CS pin.
3	DMAG	Demagnetization input. Input and output voltages are sensed from the auxiliary winding.
4	CS	Current sense pin, connect resistors to ground.
5	VDD	Power supply.
6	GATE	Gate driver for external MOSFET.

Marking information





Device comparison table

Type	V_{DD_OVP}	V_{O_OVP}	EXT_OTP	$V_{TH_OVP_SS}$	V_{TH_OVP}	Other protection
MX1210T	Latch	Latch	Latch	1.0V TYP	2.15V TYP	Auto-Retry
MX1210E	Auto-Retry	Auto-Retry	Auto-Retry	NO	3.30V TYP	Auto-Retry

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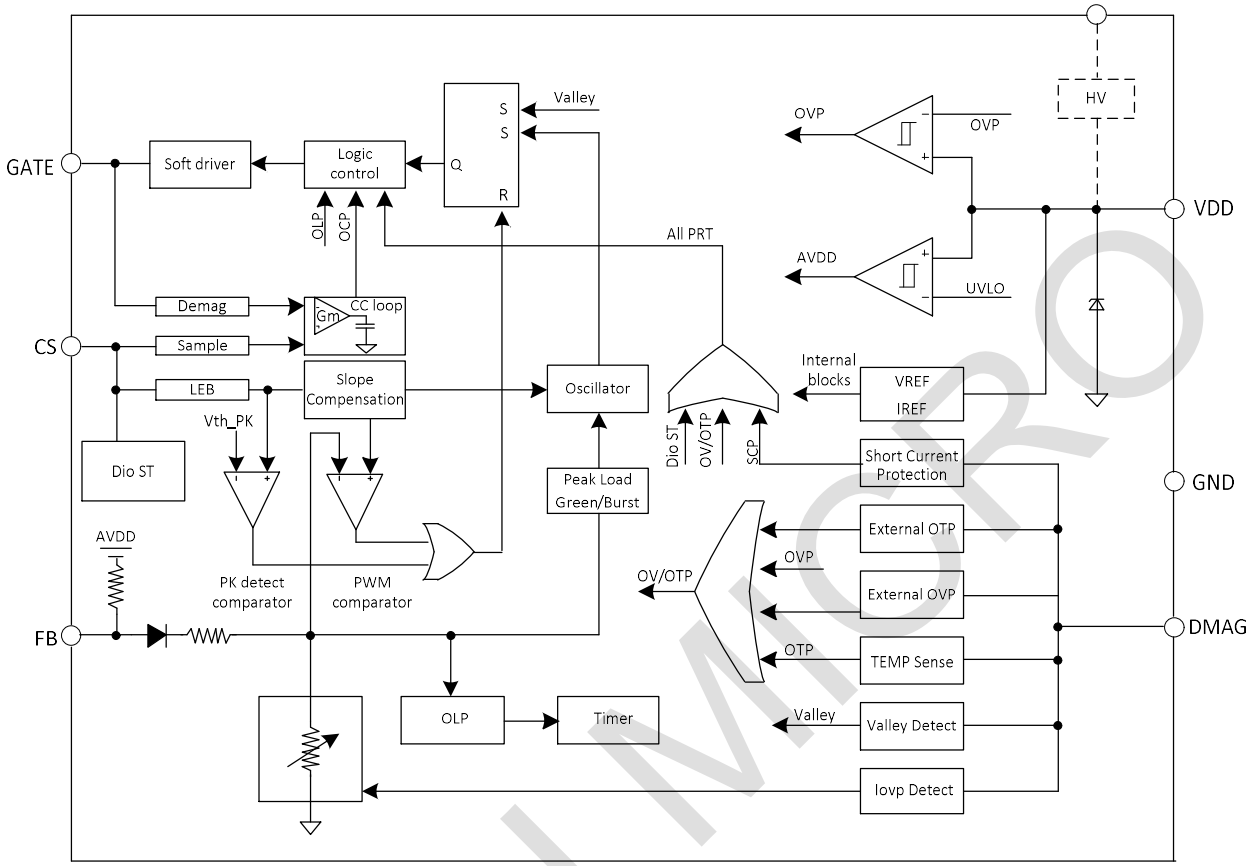
Block Diagram



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Electrical characteristics

（TA=25℃，VDD=18V，unless otherwise noted）

Symbol	Parameter	Test condition	Min	Typ.	Max	Unit
VDD supply voltage						
I startup	VDD startup current	VDD=UVLO_OFF-1V		5.0	20.0	μA
I_VDD	VDD normal operation current	V_{FB}=3V		2.8	3.3	mA
I_ Burst	Burst mode operation current	VFB=0.5V		0.45	0.48	mA
UVLO_ON	VDD under voltage lockout enter		6.7	7.2	7.7	V
UVLO_OFF	VDD under voltage lockout exit		15.5	16.5	17.5	V
V_Pull/up	Pull-up PMOS active			10		V
V_{DD_OVP}	Over voltage protection voltage	FB=3V, VDD ramp up until gate clock is off	50.0	52.0	54.0	V
V_Latch	Latch release voltage	External OTP/VDD_OVP/VO_OVP		4.8		V
T_recovery	Restart time for auto-recovery protection	Other protection		1.4		s
FB pin – Feedback input section						
V_{FB_Open}	FB open loop voltage			5.1		V
Avcs	PWM input gain ΔVFB/ΔVCS	VDMAG>1.25V		3.5		V/V
		VDMAG<1.25V		4.5		V/V
D_MAX	Max duty cycle @ VDD=18V, VFB=3V, VCS=0.3V		70		90	%
I_{FB_short}	FB pin short circuit current	Current for short FB to GND		250		μA
V_{FB_green}	The threshold enters green mode			2.05		V
$V_{REF_burst_H}$	The threshold exits burst mode			1.2		V
$V_{REF_burst_L}$	The threshold enters burst mode			1.1		V
V_{FB_OLP}	Over load protection		4.0	4.4	4.8	V
T_{D_OLP}	Over load debounce time			60		ms
R_{FB_IN}	Input impedance			20		kΩ
CS pin – Current sense input						
T_{CS_SST}	Soft start time of CS threshold			4.0		ms
T_blanking	Leading edge blanking time			300		ns
T_{D_OC}	Over current detection and delay	From over current occurs till gate driver turns off		90		ns
V_{CS_PK}	Internal current limiting threshold voltage with zero duty cycle		0.492	0.500	0.508	V
$V_{CS_PKclamp}$	CS voltage clamper			0.715		V
V_{CS_SRST}	Secondary rectifier diode short protection threshold voltage		1.1	1.2	1.3	V
V_{CS_EXOTP}	External OTP threshold voltage	DMAG=1.8V		0.80		V
T_{D_EXOTP}	External OTP delay time		42	49	56	ms

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Oscillator						
F_{OSC_NOM}	Normal frequency of high output voltage	VDD=15V, FB=3V，CS=0V	60	65	70	kHz
F_{OSC_JT}	Frequency jittering		-7		+7	%
$F_{OSC_shuffling}$	Shuffling frequency			240		Hz
F_{OSC_TEMP}	Frequency temperature stability			1.0		%
F_{OSC_VDD}	Frequency VDD voltage stability			1.0		%
F_{OSC_burst}	Burst mode frequency			22		kHz
Gate driver						
V_{GL}	Gate low voltage @ VDD=15V, Io=20mA				1.0	V
V_{GH}	Gate high voltage @ VDD=15V, Io=20mA		8.0			V
$V_{G_clamping}$	Gate clamp voltage			11.5		V
T_rise	Gate voltage rising time 1.2V ~ 10.8V @ CL=1000pF			240		ns
T_fall	Gate voltage falling time 10.8V ~ 1.2V @ CL=1000pF			25		ns
DMAG pin						
$V_{TH_OVP_SS}$	Output over voltage protection threshold voltage during start-up (30ms)	MX1210T only		1.0		V
V_{TH_OVP}	Output over voltage protection threshold voltage	MX1210T only	2.04	2.15	2.26	V
V_{TH_OVP}	Output over voltage protection threshold voltage	MX1210E only	3.20	3.30	3.40	V
V_{TH_UVP}	Output under-voltage protection threshold voltage		0.30	0.35	0.40	V
T_{D_UVP}	Output under voltage protection delay time		9	12	15	ms
T_{BLK_LL}	Blanking time of DMAG pin @ light load	V_{FB}<2.05V		1.7		μs
T_{BLK_HL}	Blanking time of DMAG pin @ high load	V_{FB}>2.05V		2.3		μs
I_{DMAG_BNI}	Brown in protection threshold current		115	130	145	μA
I_{DMAG_BNO}	Brown out protection threshold current		120	135	150	μA
T_{D_BNO}	Brown out protection delay time	FOSC=83KHz	42	49	56	ms
I_{DMAG_HVHYS}	Hysteresis of high VIN entry			7.5		μA
I_{DMAG_MAX}	Maximum DMAG sourcing current		1000			μA
Internal OTP						
OTP_in				155		℃

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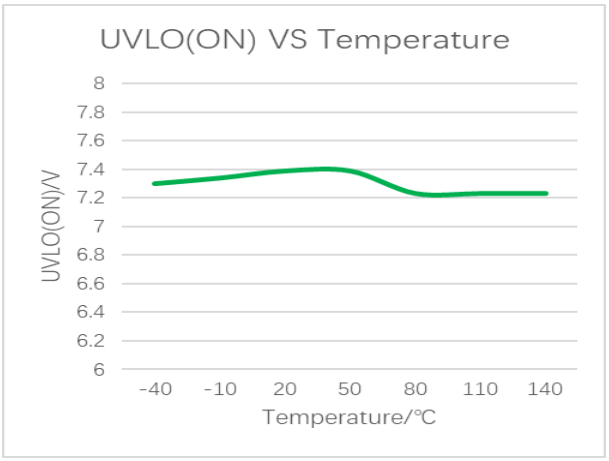
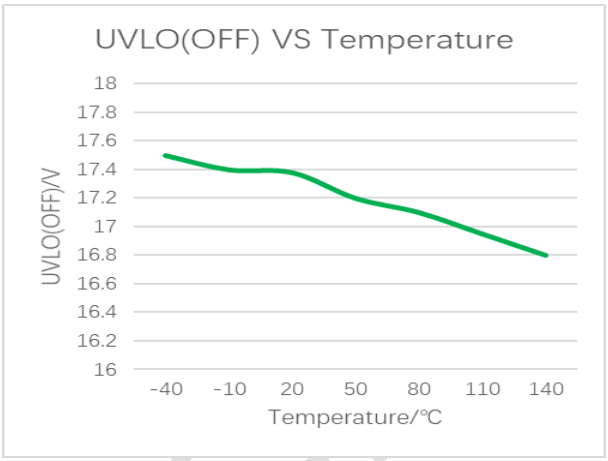
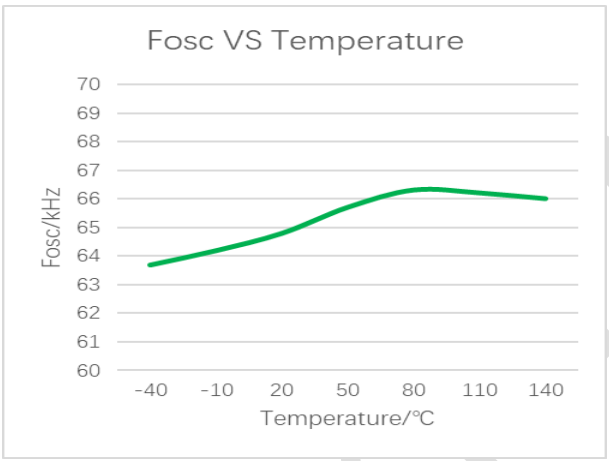
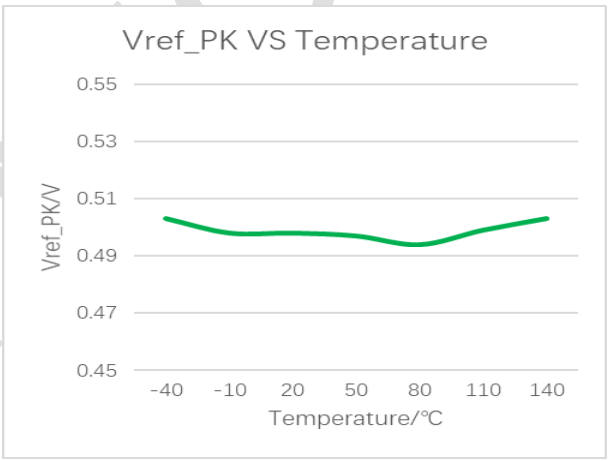
Characteristic plots

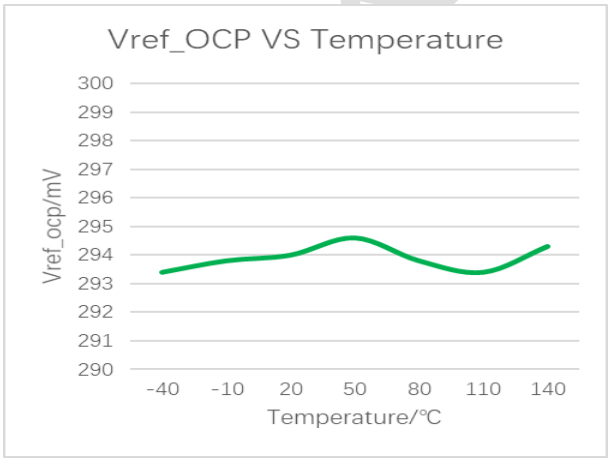
VDD=18V

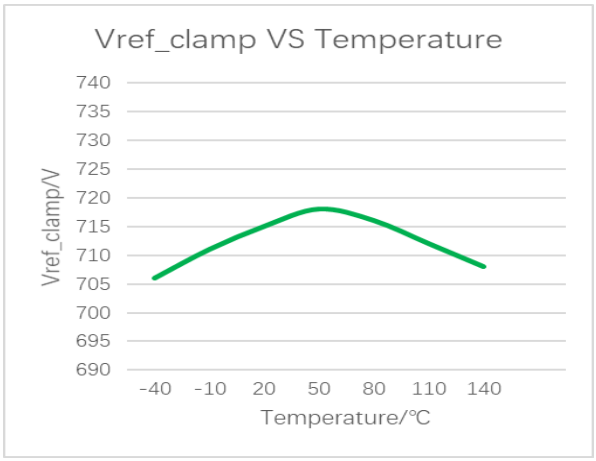


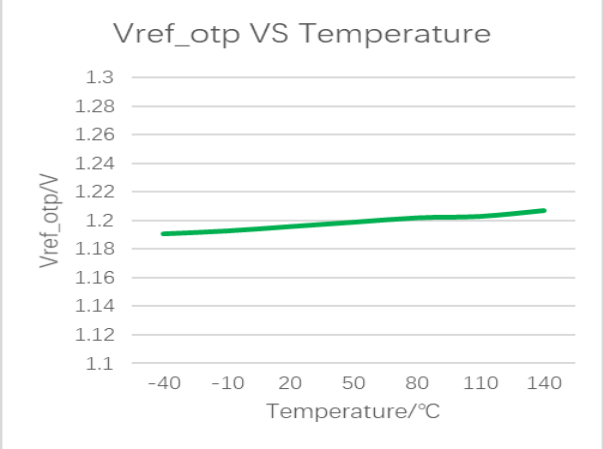


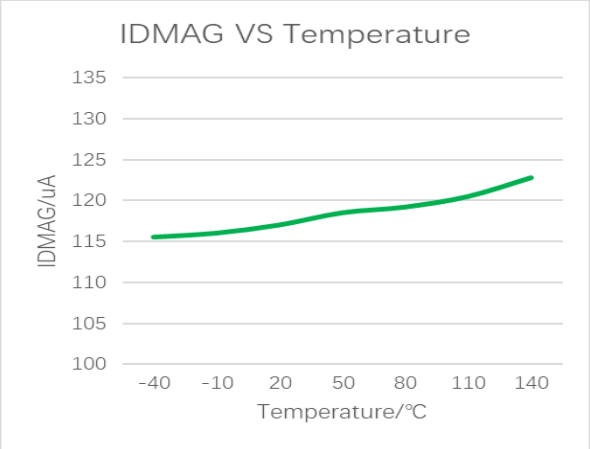


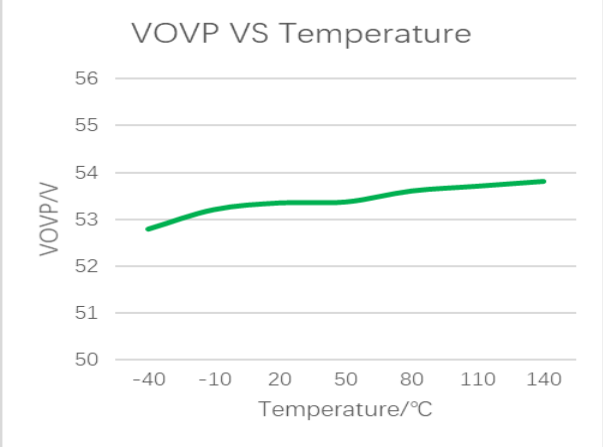


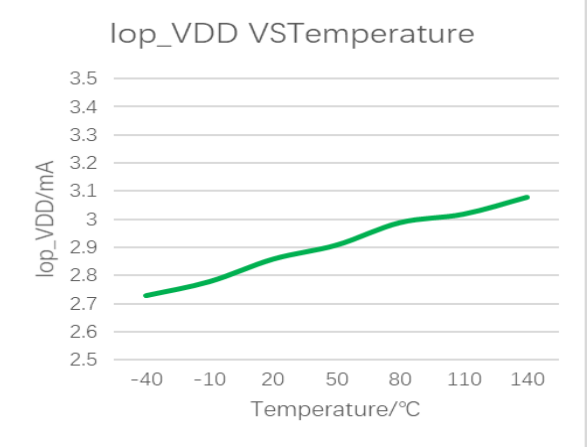





Vref_otp VS Temperature
Vref_otp/V
1.3
1.28
1.26
1.24
1.22
1.2
1.18
1.16
1.14
1.12
1.1
-40 -10 20 50 80 110 140
Temperature/℃


IDMAG VS Temperature
IDMAG/uA
135
130
125
120
115
110
105
100
-40 -10 20 50 80 110 140
Temperature/℃


VOVP VS Temperature
VOVP/V
56
55
54
53
52
51
50
-40 -10 20 50 80 110 140
Temperature/℃


Iop_VDD VSTemperature
Iop_VDD/mA
3.5
3.4
3.3
3.2
3.1
3
2.9
2.8
2.7
2.6
2.5
-40 -10 20 50 80 110 140
Temperature/℃

Operation description

MX1210 is a highly integrated current mode PWM controller, optimized for high performance, low standby power consumption and wide output voltage range PD adapter solutions. Together with PD secondary controller. The power circuit is as well compatible with cost effective offline flyback converter applications covering a wide output range. The extended burst mode control greatly reduces the standby power consumption and helps the design easily to meet the international power conservation requirements.

Startup and Internal under voltage lockout

Startup current of MX1210 is designed to be very low so that VDD could be charged up to UVLO_OFF threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet achieve a reliable startup in application.

To optimize power efficiency, startup resistors can be added to the AC line, which not only can reduce power loss but can reset latched mode protections faster.

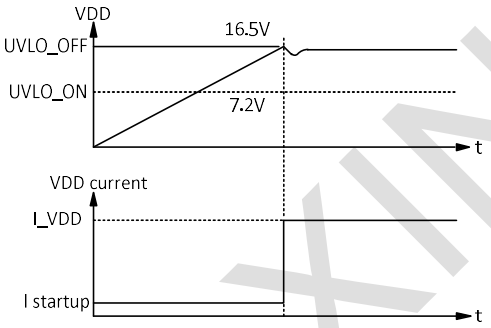


Fig1 startup current timing

Operation current

The typical operating current of MX1210 is 2.8mA. Good efficiency is achieved with this low operating current together with the extended burst mode control features.

Soft start

MX1210 features an internal 4ms soft start to soften the electrical stress occurring in the power supply during startup. It is activated during the power in sequence. As soon as VDD reaches UVLO_OFF, the CS peak voltage is gradually increased from 0V to the maximum level. Every restart up begins with a soft start.

Adaptive loop gain compensation

With MAXIN proprietary technology, an adaptive loop compensation is implemented to ensure the system loop stability for wide output voltage range according to I_OVP current detection.

Frequency shuffling for EMI improvement

The frequency shuffling is implemented in MX1210. The oscillation frequency is modulated so that the tone energy is spread out. The spread spectrum minimizes the system design.

Extended burst mode operation

At light load or no-load condition, most of the power dissipation in a switching mode power supply is from switching loss of the MOSFET, the core loss of the transformer and the loss of the snubber circuit. The magnitude of power loss is in proportion to the switching frequency. Lower switching frequency leads to the reduction on the power loss and thus conserves the energy.

The switching frequency is internally adjusted at light load or no-load condition. The switching frequency reduces at light load or no load to improve the conversion efficiency. At light load or no-load condition, the FB input drops below $V_{REF_burst_L}$ and system enters burst mode. The gate drive output switches when FB input rise back to $V_{REF_burst_H}$. Otherwise the gate drive remains at off state to minimize the switching loss and reduces the standby power consumption to the greatest extend.

Oscillator operation

During the full load power operation, MX1210 operates at 65kHz fixed frequency of high output voltage （V_{FB}>2.05V typical）. The efficiency and system cost are controlled at an optimal level. At light load, MX1210 enters the light load mode, where the output current is reduced. The switching losses are reduced by lowering the switching frequency.

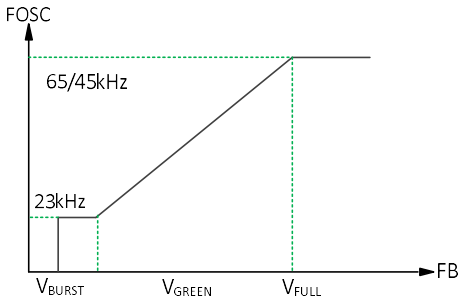


Fig2 FB voltage vs frequency

Current sensing and leading-edge blanking

Cycle by cycle current limiting is offered in MX1210 current

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mode PWM control. The switch current is detected by a sense resistor into CS pin. At internal leading-edge blanking circuit chops off the sensed voltage spike at initial internal power MOSFET on state due to snubber diode reverse recovery and surge gate current of power MOSFET. The current limiting comparator is disabled and cannot turn off the power MOSFET during the blanking period. The PWM duty cycle is determined by the current sense voltage and the FB voltage.

Internal synchronized slope compensation

Built-in slope compensation circuit adds voltage ramp into the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

Demagnetization detection

The transformer core demagnetization is detected by monitoring the voltage activity on the auxiliary windings. This voltage features a flyback polarity. After the on time, the switch is off and the flyback stoke starts. After the fly-back stroke, the drain voltage shows an oscillation with a frequency of approximately $1/2\pi\sqrt{L_P C_D}$, where L_P is the primary inductance of primary winding and C_D is the capacitance on the drain node.

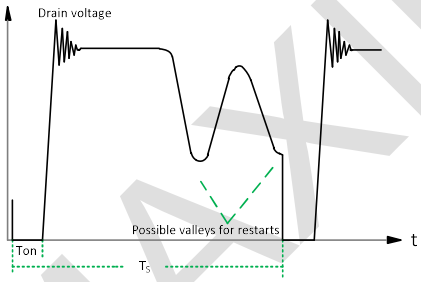

Fig3 valley detection

The typical detection level is fixed at 85mV at the DMAG pin. Demagnetization is recognized by detection of a possible valley when the voltage at DMAG pin is below 85mV in falling edge.

During the power MOSFET on time, the auxiliary winding voltage is negative, and the MX1210 outputs a clamp current to clamp the DMAG voltage at 0V. The MX1210 has built in characteristics, a DMAG brown in protection threshold current I_{DMAG_BNI} (135uA typical) and a DMAG brown out protection threshold I_{DMAG_BNO}, for the DMAG pin. The bulk-capacitor brown in and brown out voltages, V_{BULK_BNI} and V_{BULK_BNO}, can be programmed by adjusting R_{D1} and R_{D2} at the DMAG pin, as shown in Figure4. Once the brown in or brown out threshold voltage is set, the other one will be determined accordingly. The bulk capacitor brown-out threshold voltage V_{BULK_BNO} can be obtained according to the following equation:

$$\frac{V_{BULK_BNO}}{I_{DMAG_BNO}} = \frac{V_{BULK_BNI}}{I_{DMAG_BNI}}$$

When the MOSFET turns off, the DMAG pin senses the output voltage of the power stage across the auxiliary winding, with a ratio equal to the turn ratio of the auxiliary and secondary windings, and then scaled with the resistor divider R_{D2}/R_{D1}, as shown in Figure4. The voltage divider and R_{D1}/R_{D2} can be calculated by the following equation:

$$\frac{N_A}{N_P} \cdot V_{BULK_BNO} \cdot R_{D2} = I_{DMAG_BNO} \quad \text{(For brown out)}$$

$$\frac{N_A}{N_S} \cdot V_{OUT_OVP} \cdot \frac{R_{D1}}{R_{D1}+R_{D2}} = V_{TH_OVP} \quad \text{(For } V_{OUT_OVP}\text{)}$$

Where the V_{TH_OVP} is 2.15V（typical）for MX1210T and 3.30V （typical）for MX1210E.

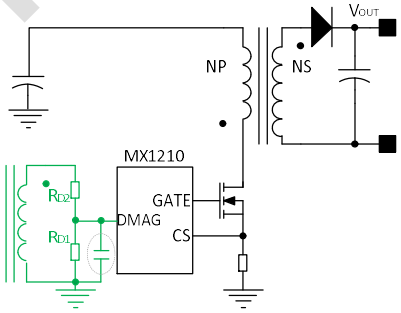

Fig4 DMAG pin application

In addition, when the MOSFET just turns off, leakage inductance of the transformer and parasitic capacitance of the MOSFET induces resonant oscillations on the DMAG pin. The resonant oscillations may cause the MX1210 to falsely trigger DMAG over voltage protection, which thus fails to reflect actual output over voltage fault condition so that the circuit may not function properly. As load increases, the duration of the resonant oscillation may also increase. A small bypass capacitor which sized from 15-33pF and placed as close to the DMAG pin as possible is recommended to be added to suppress such noises on the DMAG pin as shown in Figure4. If a larger bypass capacitor may cause the DMAG voltage to be phase shifted too much for the MOSFET not be switched on at exact valley points.

Protection controls

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Good power supply system reliability is achieved with auto recovery protection features including OCP, output short protection (SCP), Under Voltage Lockout on VDD (UVLO) and peak load protection, and latched shutdown features including Over Temperature Protection, VDD and output Over Voltage Protection (OVP).

With MAXIN proprietary technology, the OCP is line voltage compensated to achieve constant output OCP limit over the universal input voltage range and its dependency on primary inductance and frequency is removed.

At overload condition when FB pin input voltage exceeds power limit threshold value for more than Td_OLP, control circuit reacts to shut down the converter. It restarts when VDD voltage drops below UVLO limit. For protection with latched shut down mode, control circuit shuts down (latch) the power MOSFET when an over temperature condition or over voltage condition is detected until VDD drops below 4.8V （Latch release voltage）, and the device enters power on restart-up sequence thereafter.

Over current protection

MX1210 provides an adaptive cycle-by-cycle OCP compensation method varying with gate on duty cycle in Figure6. The maximum cycle-by-cycle OCP threshold voltage, Vth_PK, is 0.715V.

At PWM off state, 100uA current flows out of CS pin to generate a voltage through R1 and Rsense. The final CS peak clamping voltage threshold is adjusted by the added voltage.

$$V_{CS_PKclamp} = V_{CS_PK} + R1 \cdot 100\ uA$$

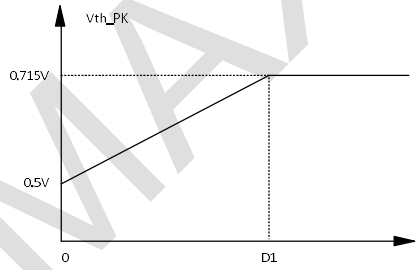

Figure5 cycle by cycle OCP compensation

Pin floating and short protection

MX1210 provides pin floating protection for all the pins and pin short protection for adjacent pins. In the cases when a pin is floating or two adjacent pins are shorted, Gate switching is disabled.

Programmable external over temperature protection

The MX1210T includes programmable external over temperature protection, implemented with a fast diode and a resistive voltage divider, which consists of an external NTC resistor to sense the power system temperature, as shown in figure6. During the MOSFET off time, the auxiliary winding voltage V_{AUX} is constant, and the CS voltage, sampled as a fraction of the clamped voltage V_{AUX_CLAMP} and compared with the internal reference voltage to set the over temperature protection threshold voltage. When the system temperature gets higher, the resistance of NTC resistor becomes smaller. By adjusting the value of the setting resistor R_{SET}, the threshold temperature for over temperature protection can be programmed. During the MOSFET off time, if the sampled CS voltage exceeds the external OTP threshold voltage V_{TH_OTP} and sustains for the external OTP delay time TD_OTP, the controller will be shut down and the switching will be stopped. If the OTP condition is removed, the controller will automatically resume operation. The design equation for the external OTP threshold voltage is expressed as below:

$$V_{TH_OTP} = \left[\frac{N_A}{N_S} \times \left(V_{O_MAX} + V_{F_OUT}\right) - V_{F_OTP}\right] \times \frac{R_{CSP} + R_{CS}}{R_{CSP} + R_{CS} + R_{NTC} + R_{SET}}$$

Where V_{O_MAX} is the maximum normal output voltage, and R_{NTC} is the NTC resistance at the threshold temperature for external OTP. It is highly recommended to use a fast diode (CT≤5pF and Trr≤50ns), ex. 1N4148 series, for external OTP application to prevent the CS pin from wrong regulation or being damaged by the negative voltage spikes.

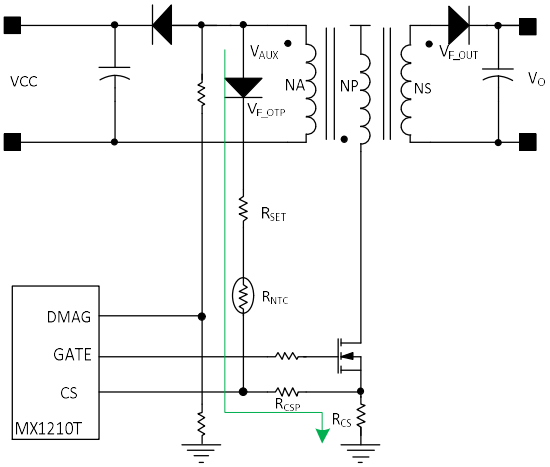

Figure6 external over temperature protection application

Feedback resistors

To enhance efficiency at light load, the power loss caused by

the feedback resistors, in parallel with the opto-coupler as shown in Figure7, must be reduced. Since the current through the feedback resistor is very small, a shunt regulator, especially with its minimum regulated current, should be carefully chosen to ensure that the shunt regulator can still regulate the output voltage at such a small cathode current.

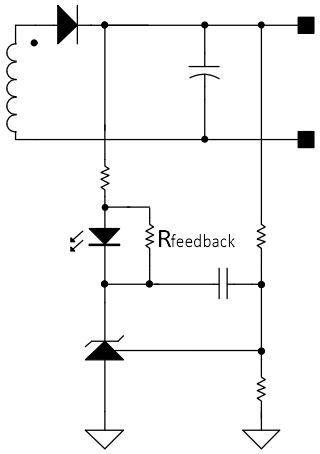

Figure7 Feedback resistor

Driver

The power MOSFET is driven by a dedicated gate driver for power switch control. Too weak the gate driver strength results in higher conduction and switch loss of MOSFET while too strong gate driver strength results the compromise of EMI.

A good tradeoff is achieved through the built-in totem pole gate design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme.

Layout considerations

A proper PCB layout can alleviate unknown noise interference and EMI emission in a switch mode power supply. It is recommended to follow the following PCB layout guidelines when a switch mode power supply is to be designed:

♦The current path A, starting from the bulk capacitor, through the transformer, the MOSFET, the resistor Rcs and back to the bulk capacitor, is a high frequency and high current loop. This path should be kept as small as possible to decrease noise coupling and kept away from other low voltage traces, such as control paths.

♦The path B, starting from the auxiliary winding, through the resistor, the diode, and VDD capacitor to the VDD pin, is also recommended to be as short as possible. Besides, the VDD capacitor should placed as close to the VDD pin as possible.

♦The path C, from the RCD snubber circuit to the MOSFET should also be kept short as it is also a loop with high frequency.

♦The path D, starting from the second winding, through the rectifier diode, the rectifier capacitor, back to second winding, is also recommended to be as short as possible. In addition, the copper areas at the anode and cathode of the diode must be large enough to ease sinking heat from the diode.

♦The path E which is from the GATE pin, through the MOSFET, the current sense resistor and back to the MX1210 ground should be kept as small as possible.

♦The ground traces of the bulk capacitor Cg, the current sense resistor Rg， the VDD capacitor CEg, the auxiliary winding Nag, and the power circuit Ug, should be separated to reduce noise, output ripple and EMI emission. The ground traces of the auxiliary winding Na and the MX1210 are connected together at the VDD capacitor ground. Then the connected ground trace goes through the VDD capacitor, the current sense ground, and to the bulk capacitor ground in turn. The area of the bulk capacitor ground trace should be large enough.

♦The bypass capacitor should be placed as closed to the power circuit as possible.

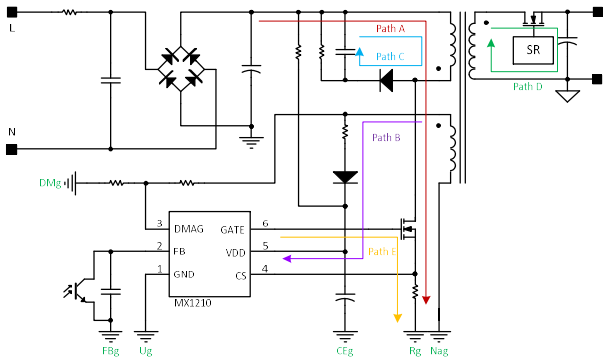

Figure8 PCB layout guide

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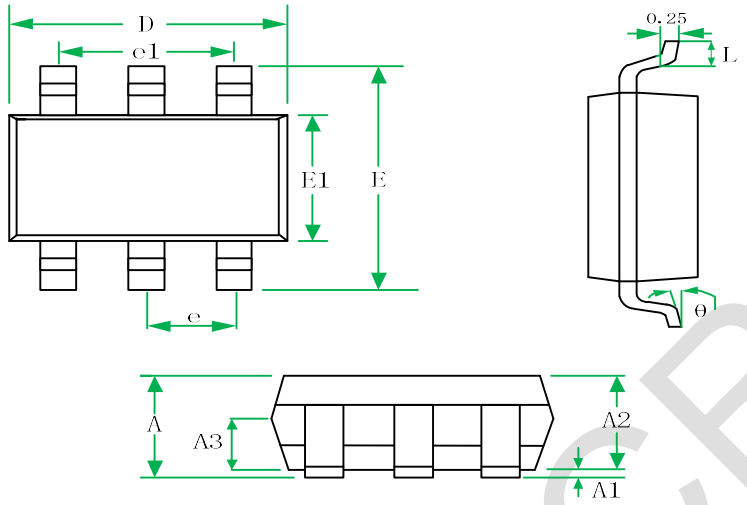
Package information



SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A						
A1	0.04		0.15	0.0016		0.0059
A2	1.00	1.10	1.20	0.039	0.043	0.047
A3	0.55	0.65	0.75	0.022	0.026	0.029
D	2.72	2.92	3.12	0.107	0.115	0.123
E	2.60	2.80	3.00	0.102	0.110	0.118
E1	1.40	1.60	1.80	0.055	0.063	0.071
e	0.95BSC			0.037BSC		
e1	1.90BSC			0.074BSC		
L	0.30		0.60	0.012		0.024
θ	0		8°	0		8°

SOT23-6 for MX1210

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