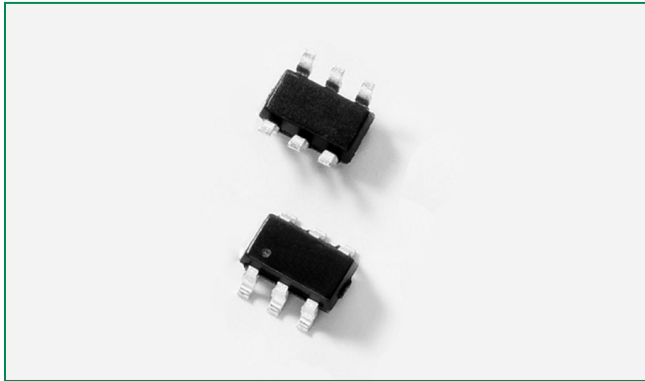
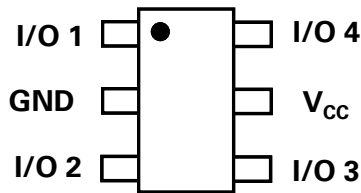


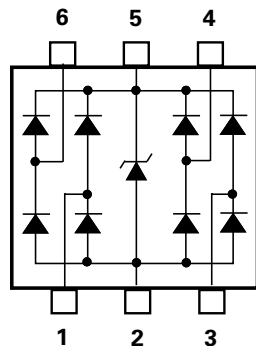
## SP3051 Series 6V 20A Diode Array



### Pinout



### Functional Block Diagram



### Description

The SP3051 integrates low capacitance rail-to-rail diodes with an additional zener diode to protect each I/O pin against ESD and high surge events. This robust device can safely absorb 20A of current per IEC61000-4-5 ( $t_p=8/20\mu s$ ) without performance degradation and a minimum  $\pm 30kV$  ESD per IEC61000-4-2. Their very low loading capacitance also makes them ideal for protecting high speed signal pins.

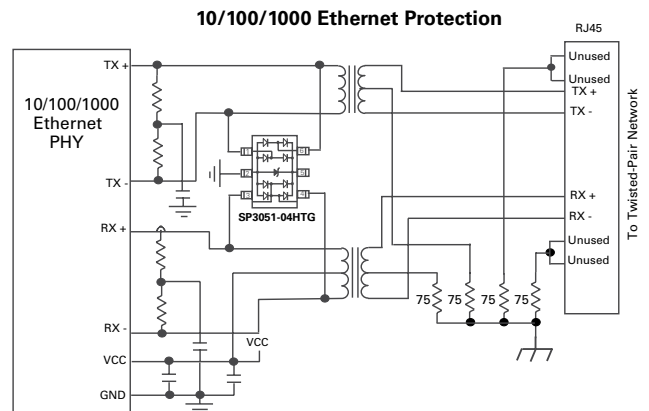
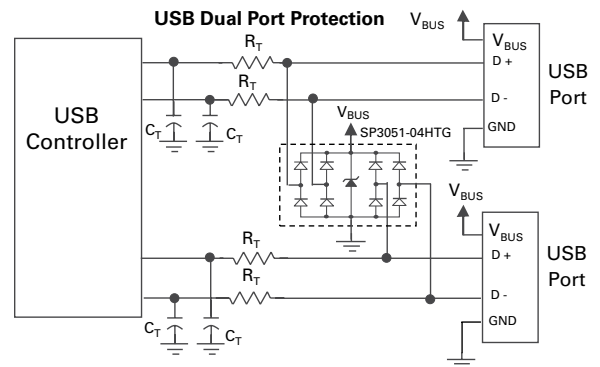
### Features

- ESD, IEC61000-4-2,  $\pm 30kV$  contact,  $\pm 30kV$  air
- EFT, IEC61000-4-4, 40A (5/50ns)
- Lightning, IEC61000-4-5, 20A (8/20 $\mu s$ )
- Low capacitance of 3.8pF (TYP) per I/O
- Low leakage current of 0.5 $\mu A$  (MAX) at 5V
- Small SOT23-6 (JEDEC MO-178AB) packaging

### Applications

- LCD/PDP TVs
- Monitors
- Notebooks
- 10/100/1000 Ethernet
- Firewire
- Set Top Boxes
- Flat Panel Displays
- Portable Medical

### Application Examples



Life Support Note:

**Not Intended for Use in Life Support or Life Saving Applications**

The products shown herein are not designed for use in life sustaining or life saving applications unless otherwise expressly indicated.

**Absolute Maximum Ratings**

Symbol	Parameter	Value	Units
$I_{PP}$	Peak Current ( $t_p=8/20\mu s$ ) <sup>1</sup>	20	A
$P_{PK}$	Peak Pulse Power ( $t_p=8/20\mu s$ )	400	W
$T_{OP}$	Operating Temperature	-40 to 125	°C
$T_{STOR}$	Storage Temperature	-55 to 150	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

**Thermal Information**

Parameter	Rating	Units
Storage Temperature Range	-55 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 20-40s)	260	°C

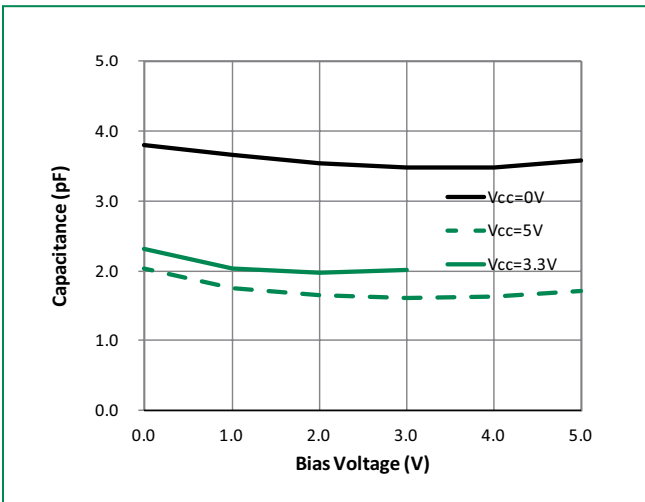
**Electrical Characteristics ( $T_{OP}=25^\circ C$ )**

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reverse Standoff Voltage	$V_{RWM}$	$I_R \leq 1\mu A$			6.0	V
Breakdown Voltage	$V_R$	$I_R = 1mA$		8.0		V
Reverse Leakage Current	$I_{LEAK}$	$V_R=5V$		0.1	0.5	$\mu A$
Clamp Voltage <sup>1</sup>	$V_C$	$I_{PP}=1A, t_p=8/20\mu s, I/O \text{ to GND}^2$		9.0	10.5	V
		$I_{PP}=10A, t_p=8/20\mu s, I/O \text{ to GND}^2$		11.5	15.0	V
		$I_{PP}=20A, t_p=8/20\mu s, I/O \text{ to GND}^2$		14.3	17.0	V
Dynamic Resistance	$R_{DYN}$	$(V_{C2} - V_{C1}) / (I_{PP2} - I_{PP1})$		0.3		$\Omega$
ESD Withstand Voltage <sup>1</sup>	$V_{ESD}$	IEC61000-4-2 (Contact)	$\pm 30$			kV
		IEC61000-4-2 (Air)	$\pm 30$			kV
Diode Capacitance <sup>1</sup>	$C_{I/O-GND}$	Reverse Bias=0V		3.8	4.2	pF
		Vcc=5V, Reverse Bias=2.5V		1.7	2.0	pF
Diode Capacitance <sup>1</sup>	$C_{I/O-I/O}$	Reverse Bias=0V		2.0		pF

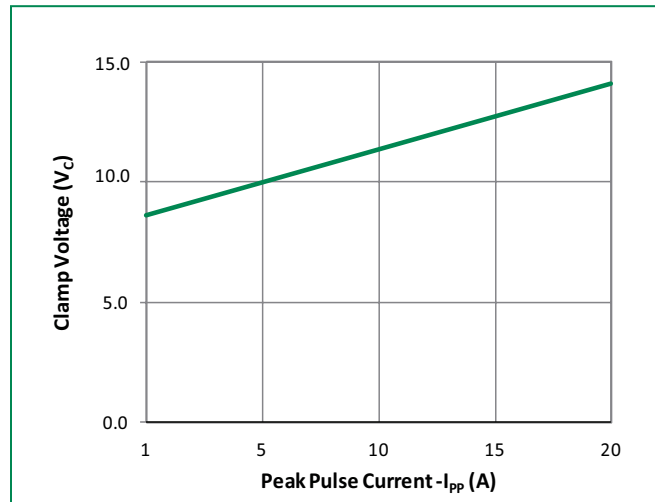
Notes: <sup>1</sup> Parameter is guaranteed by design and/or device characterization.

<sup>2</sup> Repetitive pulse per waveform shown on page 3.

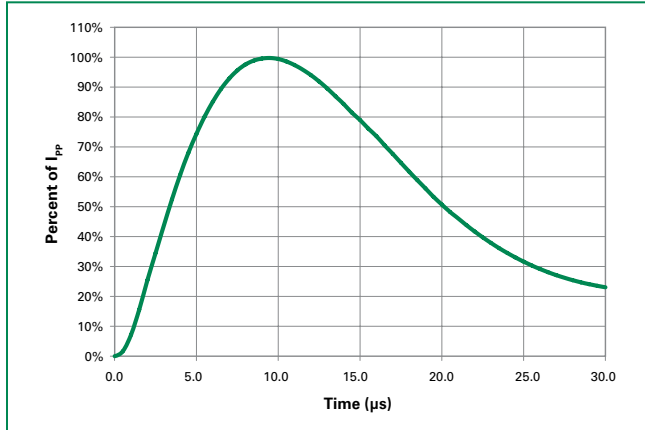
**Capacitance vs. Reverse Voltage**



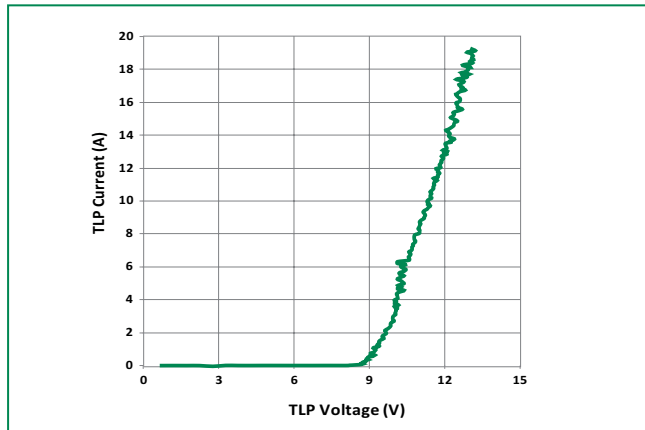
**Clamping Voltage vs. Peak Pulse Current**



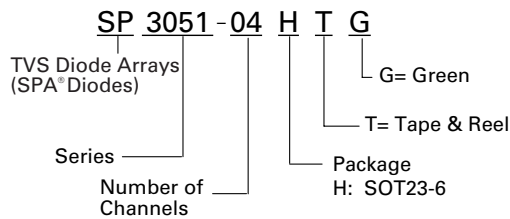
**Pulse Waveform**



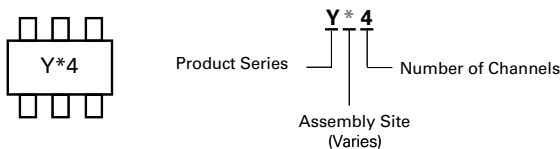
**Transmission Line Pulsing (TLP) Plot**



**Part Numbering System**



**Part Marking System**



**Ordering Information**

Part Number	Package	Marking	Min. Order Qty.
SP3051-04HTG	SOT23-6	YH4	3000

**Product Characteristics**

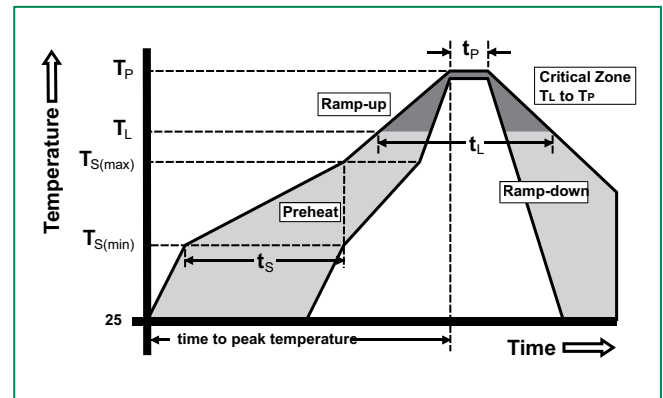
<b>Lead Plating</b>	Matte Tin
<b>Lead Material</b>	Copper Alloy
<b>Lead Coplanarity</b>	0.0004 inches (0.102mm)
<b>Substitute Material</b>	Silicon
<b>Body Material</b>	Molded Epoxy
<b>Flammability</b>	UL 94 V-0

Notes :

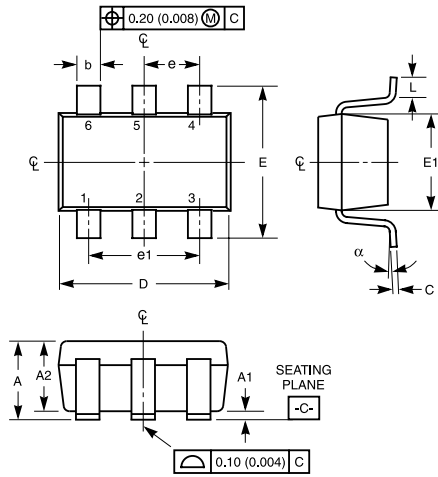
1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
5. Package surface matte finish VDI 11-13.
6. All specifications comply to JEDEC Spec MO-178AB Issue C

**Soldering Parameters**

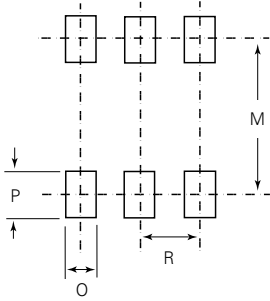
Reflow Condition	Pb – Free assembly	
Pre Heat	- Temperature Min ( $T_{s(min)}$ )	150°C
	- Temperature Max ( $T_{s(max)}$ )	200°C
	- Time (min to max) ( $t_s$ )	60 – 180 secs
Average ramp up rate (Liquidus) Temp ( $T_L$ ) to peak	3°C/second max	
$T_{S(max)}$ to $T_L$ - Ramp-up Rate	3°C/second max	
Reflow	- Temperature ( $T_L$ ) (Liquidus)	217°C
	- Temperature ( $t_L$ )	60 – 150 seconds
Peak Temperature ( $T_p$ )	260 <sup>+0/-5</sup> °C	
Time within 5°C of actual peak Temperature ( $t_p$ )	20 – 40 seconds	
Ramp-down Rate	6°C/second max	
Time 25°C to peak Temperature ( $T_p$ )	8 minutes Max.	
Do not exceed	260°C	



**Package Dimensions – SOT23-6**



**Recommended Solder Pad Layout**



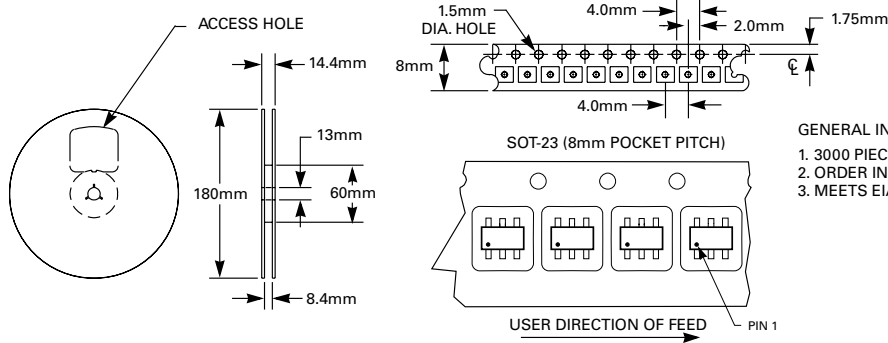
Package	SOT23				Notes
Pins	6				
JEDEC	MO-178AB				
	Millimeters		Inches		
	Min	Max	Min	Max	
<b>A</b>	0.900	1.450	0.035	0.057	-
<b>A1</b>	0.000	0.150	0.000	0.006	-
<b>A2</b>	0.900	1.300	0.035	0.051	-
<b>b</b>	0.350	0.500	0.0138	0.0196	-
<b>C</b>	0.080	0.220	0.0031	0.009	-
<b>D</b>	2.800	3.000	0.11	0.118	3
<b>E</b>	2.600	3.000	0.102	0.118	-
<b>E1</b>	1.500	1.750	0.06	0.069	3
<b>e</b>	0.95 Ref		0.0374 ref		-
<b>e1</b>	1.9 Ref		0.0748 Ref		-
<b>L</b>	0.30	0.600	0.012	0.023	4,5
<b>N</b>	6		6		6
<b>alpha</b>	0°	8°	0°	8°	-
<b>M</b>	2.590		0.102		-
<b>O</b>	0.690		.027 TYP		-
<b>P</b>	0.990		.039 TYP		-
<b>R</b>	0.950		0.038		-

Notes:

1. Dimensioning and tolerancing Per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC-74 (1992).
3. Dimensions D and E1 are exclusive of mold flash, protrusions, or gate burrs.
4. Foot length L measured at reference to seating plane.
5. "L" is the length of flat foot surface for soldering to substrate.
6. "N" is the number of terminal positions.
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

**Embossed Carrier Tape & Reel Specification – SOT23-6**

8mm TAPE AND REEL



- GENERAL INFORMATION**
1. 3000 PIECES PER REEL.
  2. ORDER IN MULTIPLES OF FULL REELS ONLY.
  3. MEETS EIA-481 REVISION "A" SPECIFICATIONS.