Delson
Technology Co, Ltd.

D936865G28MG
128M x 64 HIGH PERFORMANCE PC3 -10600
UNBUFFERED DDR3 SDRAM SODIMM

Features

- 240-Pin Dual In-Line Memory Module (UDIMM)
- Inputs and outputs are SSTL-15 compatible
- $V_{DD} = V_{DDQ} = 1.5V \pm 0.075V$
- Differential clock inputs
- Data is read or written on both clock edges
- DRAM DLL aligns DQ and DQS transitions with clock t
- Address and control signals are fully synchronous to positive clock edge
- Extended operating temperature rage
- Auto Self-Refresh option
- Serial Presence Detect
- Gold contacts
- 1GB: SDRAMs are in 78-ball BGA Package
- RoHS compliance and Halogen Free

Description

The D936865G28MG memory module is organized as 128M x 64 bits in a 204 pin memory module.
The 128M x 64 memory module uses 8 pcs 128M X8 DDR3 SDRAMs
The x64 module are ideal for use in high performance computer systems where increased memory density and fast access times are required.

SO-DIMM Pin Description

Pin Name	Description	Number	Pin Name	Description	Number
CK0, CK1	Clock Inputs, positive line	2	DQ0-DQ63	Data Input/Output	64
$\overline{CK}0$, $\overline{CK}1$	Clock Inputs, negative line	2	DM0-DM7	Data Masks/ Data strobes, Termination data strobes	8
CKE0, CKE1	Clock Enables	2	DQS0-DQS7	Data strobes	8
$\overline{RAS}$	Row Address Strobe	1	$\overline{DQS}0$-$\overline{DQS}7$	Data strobes complement	8
$\overline{CAS}$	Column Address Strobe	1	$\overline{RESET}$	Reset Pin	1
$\overline{WE}$	Write Enable	1	TEST	Logic Analyzer specific test pin (No connect on SODIMM)	1
$\overline{S}0$, $\overline{S}1$	Chip Selects	2	V_{DD}	Core and I/O Power	18
A0-A9, A11, A13-A15	Address Inputs	14	V_{SS}	Ground	52
A10/AP	Address Input/Autoprecharge	1	V_{REFDQ} V_{REFCA}	Input/Output Reference	2
A12/$\overline{BC}$	Address Input/Burst chop	1	V_{DDSPD}	SPD and Temp sensor Power	1
BA0-BA2	SDRAM Bank Addresses	3	V_{TT}	Termination Voltage	2
ODT0, ODT1	On-die termination control	2	NC	Reserved for future use	3
SCL	Serial Presence Detect (SPD) Clock Input	1		Total	204
SDA	SPD Data Input/Output	1			
SA0-SA1	SPD Address	2			

*The V_{DD} and V_{DDQ} pins are tied common to a single power-plane on these designs.

Pin Assignments

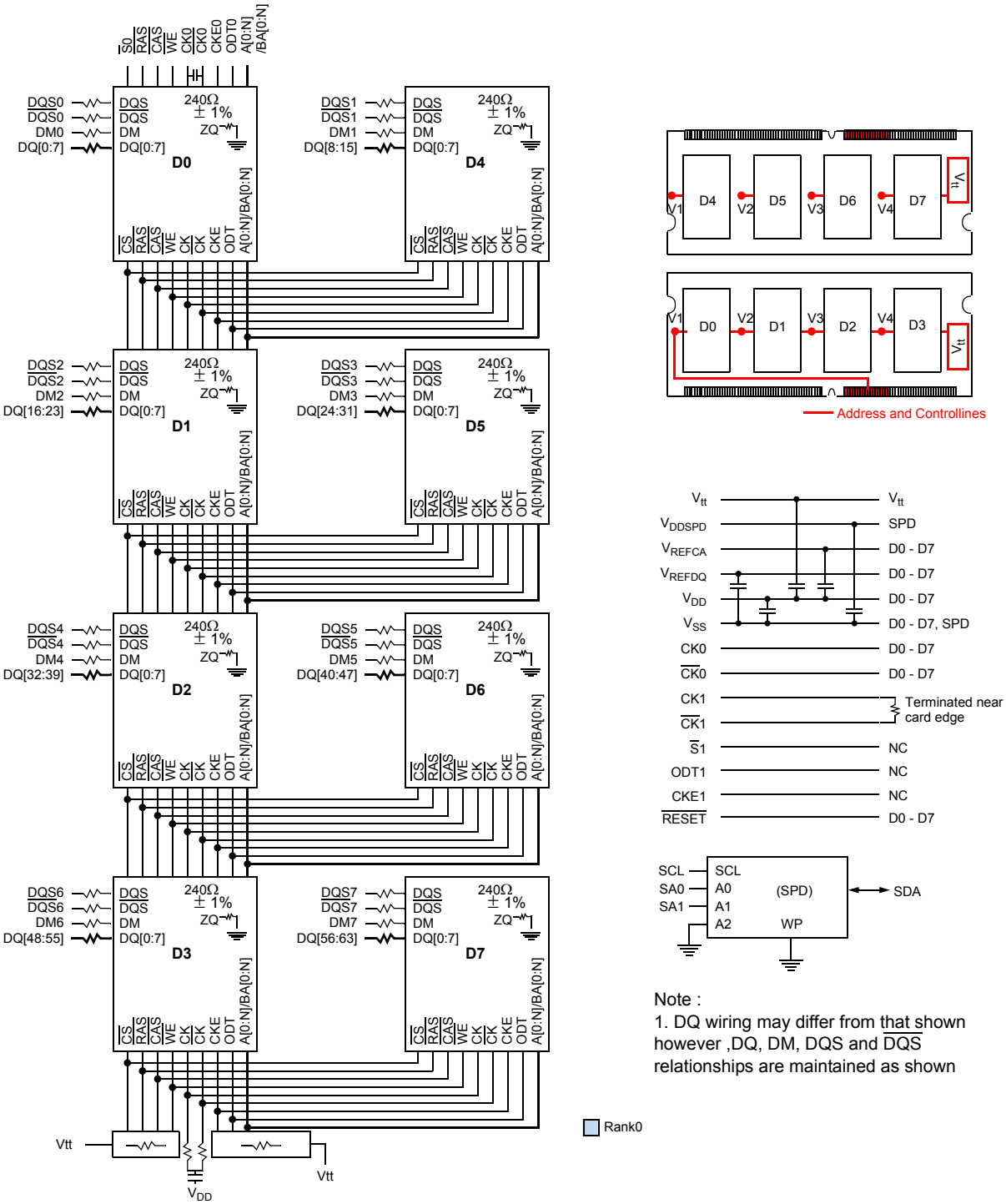
Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side
1	$V_{REF}DQ$	2	V_{SS}	53	DQ19	54	V_{SS}	105	V_{DD}	106	V_{DD}	157	DQ42	158	DQ46
3	V_{SS}	4	DQ4	55	V_{SS}	56	DQ28	107	A10/AP	108	BA1	159	DQ43	160	DQ47
5	DQ0	6	DQ5	57	DQ24	58	DQ29	109	BA0	110	$\overline{RAS}$	161	V_{SS}	162	V_{SS}
7	DQ1	8	V_{SS}	59	DQ25	60	V_{SS}	111	V_{DD}	112	V_{DD}	163	DQ48	164	DQ52
9	V_{SS}	10	$\overline{DQS}0$	61	V_{SS}	62	$\overline{DQS}3$	113	$\overline{WE}$	114	$\overline{S}0$	165	DQ49	166	DQ53
11	DM0	12	DQS0	63	DM3	64	DQS3	115	$\overline{CAS}$	116	ODT0	167	V_{SS}	168	V_{SS}
13	V_{SS}	14	V_{SS}	65	V_{SS}	66	V_{SS}	117	V_{DD}	118	V_{DD}	169	$\overline{DQS}6$	170	DM6
15	DQ2	16	DQ6	67	DQ26	68	DQ30	119	A13[2]	120	ODT1	171	DQS6	172	V_{SS}
17	DQ3	18	DQ7	69	DQ27	70	DQ31	121	$\overline{S}1$	122	NC	173	V_{SS}	174	DQ54
19	V_{SS}	20	V_{SS}	71	V_{SS}	72	V_{SS}	123	V_{DD}	124	V_{DD}	175	DQ50	176	DQ55
21	DQ8	22	DQ12	73	CKE0	74	CKE1	125	TEST	126	$V_{REF}CA$	177	DQ51	178	V_{SS}
23	DQ9	24	DQ13	75	V_{DD}	76	V_{DD}	127	V_{SS}	128	V_{SS}	179	V_{SS}	180	DQ60
25	V_{SS}	26	V_{SS}	77	NC	78	A15[2]	129	DQ32	130	DQ36	181	DQ56	182	DQ61
27	$\overline{DQS}1$	28	DM1	79	BA2	80	A14[2]	131	DQ33	132	DQ37	183	DQ57	184	V_{SS}
29	DQS1	30	$\overline{RESET}$	81	V_{DD}	82	V_{DD}	133	V_{SS}	134	V_{SS}	185	V_{SS}	186	$\overline{DQS}7$
31	V_{SS}	32	V_{SS}	83	A12/$\overline{BC}$	84	A11	135	$\overline{DQS}4$	136	DM4	187	DM7	188	DQS7
33	DQ10	34	DQ14	85	A9	86	A7	137	DQS4	138	V_{SS}	189	V_{SS}	190	V_{SS}
35	DQ11	36	DQ15	87	V_{DD}	88	V_{DD}	139	V_{SS}	140	DQ38	191	DQ58	192	DQ62
37	V_{SS}	38	V_{SS}	89	A8	90	A6	141	DQ34	142	DQ39	193	DQ59	194	DQ63
39	DQ16	40	DQ20	91	A5	92	A4	143	DQ35	144	V_{SS}	195	V_{SS}	196	V_{SS}
41	DQ17	42	DQ21	93	V_{DD}	94	V_{DD}	145	V_{SS}	146	DQ44	197	SA0	198	$\overline{EVENT}$
43	V_{SS}	44	V_{SS}	95	A3	96	A2	147	DQ40	148	DQ45	199	VDD_{SPD}	200	SDA
45	$\overline{DQS}2$	46	DM2	97	A1	98	A0	149	DQ41	150	V_{SS}	201	SA1	202	SCL
47	DQS2	48	V_{SS}	99	V_{DD}	100	V_{DD}	151	V_{SS}	152	$\overline{DQS}5$	203	V_{TT}	204	V_{TT}
49	V_{SS}	50	DQ22	101	CK0	102	CK1	153	DM5	154	DQS5				
51	DQ18	52	DQ23	103	$\overline{CK0}$	104	$\overline{CK1}$	155	V_{SS}	156	V_{SS}				

NC = No Connect; RFU = Reserved Future Use

1. TEST (pin 125) is reserved for bus analysis probes and is NC on normal memory modules.
2. This address might be connected to NC balls of the DRAMs (depending on density); either way they will be connected to the termination resistor.

Block Diagram

1GB, 128Mx64 Module



Note :

1. DQ wiring may differ from that shown however ,DQ, DM, DQS and $\overline{DQS}$ relationships are maintained as shown

Absolute Maximum Ratings

Absolute Maximum DC Ratings

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to Vss	- 0.4 V ~ 1.975 V	V	1,
VDDQ	Voltage on VDDQ pin relative to Vss	- 0.4 V ~ 1.975 V	V	1,
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	- 0.4 V ~ 1.975 V	V	1
T_{STG}	Storage Temperature	-55 to +100	^{o}C	1, 2

Notes:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300mV of each other at all times; and VREF must not be greater than 0.6XVDDQ,When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

DRAM Component Operating Temperature Range

Temperature Range

Symbol	Parameter	Rating	Units	Notes
T_{OPER}	Normal Operating Temperature Range	0 to 85	^{o}C	1,2
	Extended Temperature Range	85 to 95	^{o}C	1,3

Notes:

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 - 85^{o}C under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85^{o}C and 95^{o}C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
   a. Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range. Please refer to the DIMM SPD for option availability
   b. If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b). Hynix DDR3 SDRAMs support Auto Self-Refresh and Extended Temperature Range and please refer to Hynix component datasheet and/or the DIMM SPD for tREFI requirements in the Extended Temperature Range.

AC & DC Operating Conditions

Recommended DC Operating Conditions

Recommended DC Operating Conditions

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.425	1.500	1.575	V	1,2
VDDQ	Supply Voltage for Output	1.425	1.500	1.575	V	1,2

Notes:

1. Under all conditions, VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

AC & DC Input Measurement Levels

AC and DC Logic Input Levels for Single-Ended Signals

AC and DC Input Levels for Single-Ended Command and Address Signals

Single Ended AC and DC Input Levels for Command and ADDress

Symbol	Parameter	DDR3-800/1066/1333		Unit	Notes
		Min	Max		
VIH.CA(DC100)	DC input logic high	Vref + 0.100	VDD	V	1
VIL.CA(DC100)	DC input logic low	VSS	Vref - 0.100	V	1
VIH.CA(AC175)	AC input logic high	Vref + 0.175		V	1
VIL.CA(AC175)	AC input logic low	Vref - 0.175		V	1
VIH.CA(AC150)	AC Input logic high	Vref + 0.150		V	1
VIL.CA(AC150)	AC input logic low		Vref - 0.150	V	1
$V_{RefCA(DC)}$	Reference Voltage for ADD, CMD inputs	0.49 * VDD	0.51 * VDD	V	2, 3

Notes:

1. For input only pins except $\overline{\text{RESET}}$, Vref = VrefCA (DC).
2. The ac peak noise on V_{Ref} may not allow V_{Ref} to deviate from $V_{RefCA(DC)}$ by more than +/-1% VDD (for reference: approx. +/- 15 mV).
3. For reference: approx. VDD/2 +/- 15 mV.

AC and DC Input Levels for Single-Ended Signals

DDR3 SDRAM will support two Vih/Vil AC levels for DDR3-800 and DDR3-1066 as specified in the table below.

Single Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	DDR3-800/1066		DDR3-1333		Unit	Notes
		Min	Max	Min	Max		
VIH.CA(DC100)	DC input logic high	Vref + 0.100	VDD	Vref + 0.100	VDD	V	1
VIL.CA(DC100)	DC input logic low	VSS	Vref - 0.100	VSS	Vref - 0.100	V	1
VIH.CA(AC175)	AC input logic high	Vref + 0.175		-	-	V	1
VIL.CA(AC175)	AC input logic low		Vref - 0.175	-	-	V	1
VIH.CA(AC150)	AC Input logic high	Vref + 0.150	Vref + 0.150			V	1
VIL.CA(AC150)	AC input logic low		Vref - 0.150		Vref - 0.150	V	1
$V_{RefDQ(DC)}$	Reference Voltage for DQ, DM inputs	0.49 * VDD	0.51 * VDD	0.49 * VDD	0.51 * VDD	V	2,3

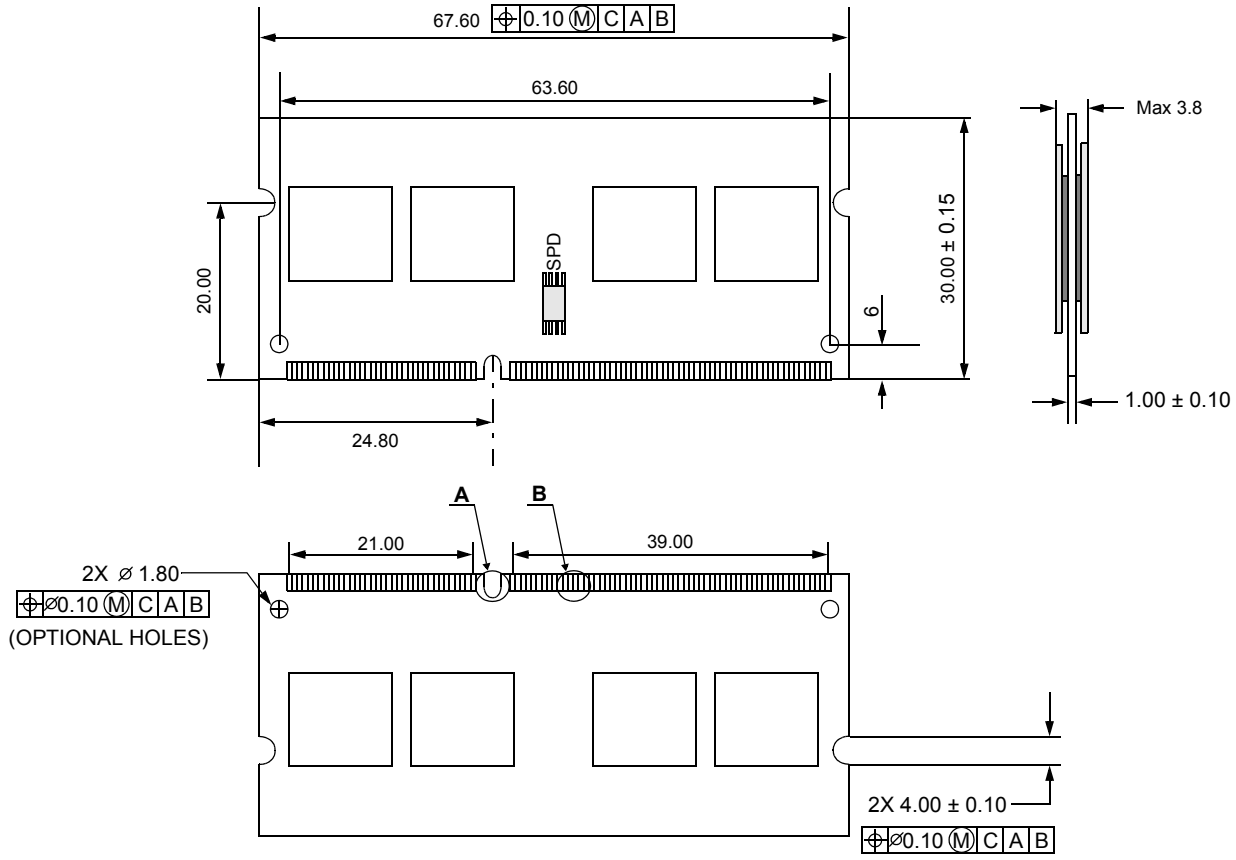
Notes:

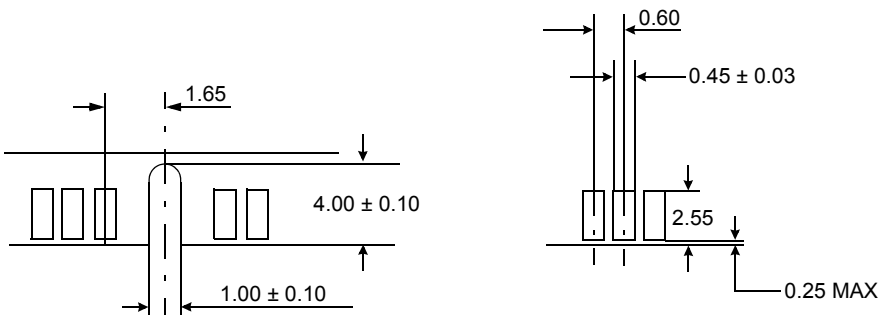
1. Vref = VrefDQ (DC).
2. The ac peak noise on V_{Ref} may not allow V_{Ref} to deviate from $V_{RefDQ(DC)}$ by more than +/-1% VDD (for reference: approx. +/- 15 mV).
3. For reference: approx. VDD/2 +/- 15 mV.

Package Dimension

(1GB, 1 Ranks, 128Mx8 DDR3 SDRAMs)

Units : Millimeters





Detail A **Detail B**

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