Delson
Technology Co, Ltd.

D83CDG08(80A/168)PB
HIGH PERFORMANCE 8Gbit DDR4 SDRAM
16 BANKS X 64Mbit X 8
8 BANKS X 64Mbit X 16

	L15	M17	N19	unit
	DDR4-2133	DDR4-2400	DDR4-2666	
System Frequency (f_{CK})	1066 MHz	1200 MHz	1333 MHz	MHz
Clock Cycle Time (t_{CK})	0.938	0.833	0.75	ns
$\overline{CAS}$ latency (CL)	15	17	19	t_{CK}

Specifications

- Density : 8G bits
- Organization :
  - 1GB bit x8 ,64M words x 8 bits x 16 banks (D83CDG0880APB)
  - 512Mbit x16 ,64M words x 16 bits x 8 banks (D83CDG08168PB)
- Package :
  - 78-ball FBGA for X8 / 96-ball FBGA for X16
  - Lead-free (RoHS compliant) and Halogen-free
- Power supply :
  - VDD, VDDQ = 1.2V ± 60mV
  - VPP = 2.5V, -125mV / +250mV
- Data rate : 2133Mbps/2400Mbps/2666Mbps
- 1KB page size for X8 / 2KB page size for X16
  - Row address: A0 to A15
  - Column address: A0 to A9
- Sixteen-banks(4 bank group with 4 banks for each bank group) for X8 and eight-banks(2 bank group with 4 banks for each bank group) for X16
- Burst lengths (BL) : BL8, BC4, BC4 or 8 on the fly
- Burst type (BT) : Sequential, Interleave
- $\overline{CAS}$ Latency (CL) : 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21
- $\overline{CAS}$ Write Latency (CWL) : 9, 10, 11, 12, 14, 16, 18
- Additive Latency (AL) : 0, CL-1, CL-2
- $\overline{CS}$ to Command Address Latency (AL) : 3, 4, 5, 6, 8
- Command Address Parity Latency : 4, 5, 6
- Write Recovery time : 10, 12, 14, 16, 18, 20, 24
- Driver strength : RZQ/7, RZQ/5 (RZQ = 240 Ω)
- RTT_PARK(34/40/48/60/80/120/240)
- RTT_NOM(34/40/48/60/80/120/240)
- RTT_WR(80/120/240)
- Read Preamble (1T/2T)
- Write Preamble (1T/2T)
- LPASR(Manual:Normal/Reduced/Extended, Auto:TS)
- Refresh cycles (Average refresh period) :
  - 7.8 μs at 0°C ≤ Tc ≤ +85°C
  - 3.9 μs at +85°C < Tc ≤ +95°C
- Operating case temperature range
  - Comercial Tc = 0°C to +95°C
  - Industrial Tc = -40°C to +95°C

Features

- 1.2V pseudo open-drain interface
- 8n prefetch architecture
- Internal VREFDQ training
- Programmable data strobe preambles
- Data strobe preamble training
- Command/Address latency (CAL)
- Multipurpose register READ and WRITE capability
- Write and read leveling
- Auto refresh and self refresh Modes
- Low-power auto self refresh (LPASR)
- Auto Self Refresh (ASR) by DRAM built-in TS
- Fine granularity refresh
- Self refresh abort
- Maximum power saving
- Output driver calibration
- Configurable on-die termination (ODT)
- Data bus inversion (DBI) for data bus
- Command/Address (CA) parity
- Databus write cyclic redundancy check (CRC)
- Per-DRAM addressability
- Connectivity test (x16)

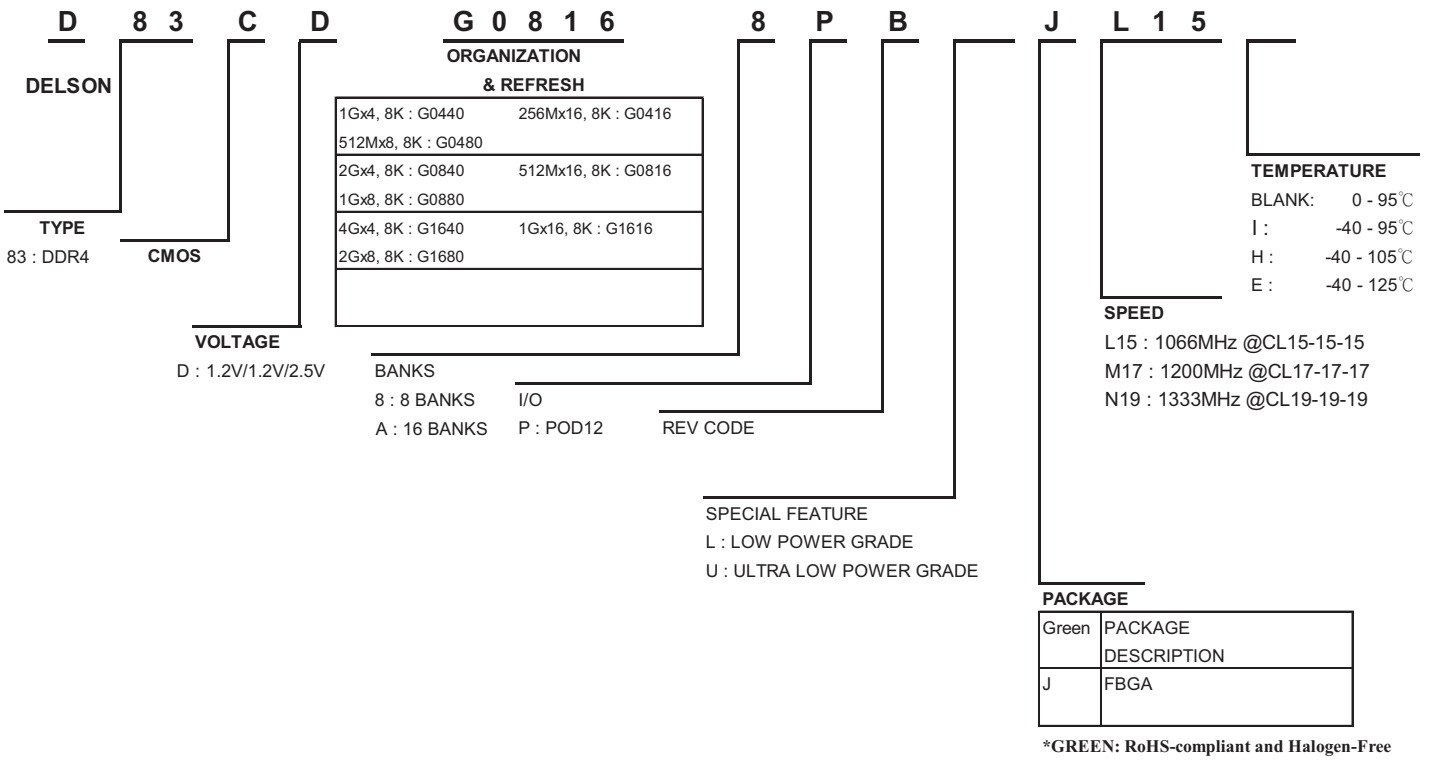
Device Usage Chart

Operating Temperature Range	Package Outline	Speed			Power	Temperature Mark
	78-ball FBGA 96-ball FBGA	- L15	- M17	- N19	Std.	
0°C ≤ Tc ≤ 95°C	•	•	•	•	•	Blank
-40°C ≤ Tc ≤ 95°C	•	•	•	•	•	I

DDR4 Speed Bin and operation frequency support

Speed	DDR4-2666	DDR4-2400	DDR4-2133	DDR4-1866	DDR4-1600	Unit
	19-19-19	17-17-17	15-15-15	13-13-13	11-11-11	
tCK (min)	0.75	0.833	0.938	1.071	1.25	ns
CAS Latency (min)	19	17	15	13	11	nCK
tRCD (min)	14.25	14.16	14.07	13.92	13.75	ns
tRP (min)	14.25	14.16	14.07	13.92	13.75	ns
tRAS (min)	32	32	33	34	35	ns
tRC (min)	46.25	46.16	47.06	47.92	48.75	ns
D83CDG0880APBJN19	2666	2400	2133	1866	1600	Mbps
D83CDG08168PBJN19	2666	2400	2133	1866	1600	Mbps
D83CDG0880APBJM17	--	2400	2133	1866	1600	Mbps
D83CDG08168PBJM17	--	2400	2133	1866	1600	Mbps
D83CDG0880APBJL15	--	--	2133	1866	1600	Mbps
D83CDG08168PBJL15	--	--	2133	1866	1600	Mbps

Part Number Information



***GREEN: RoHS-compliant and Halogen-Free**

8Gb DDR4 SDRAM Addressing

Configuration	1Gb x 8	512Mb x 16
# of Bank	16	8
Bank Address	BA0 ~ BA1	BA0 ~ BA1
Bank Group	BG0 ~ BG1	BG0
Auto precharge	A10/AP	A10/AP
Row Address	A0 ~ A15	A0 ~ A15
Column Address	A0 ~ A9	A0 ~ A9
BC switch on the fly	A12/$\overline{BC}$	A12/$\overline{BC}$
Page size	1 KB	2 KB

Pin Configurations

78-ball FBGA (x8 configuration)

	1	2	3	4	5	6	7	8	9	
A	V_{DD}	V_{SSQ}	$\overline{TDQS}$				$\overline{DM}/\overline{DBI}/TDQS$	V_{SSQ}	V_{SS}	**A**
B	V_{PP}	V_{DDQ}	$\overline{DQS}$				DQ1	V_{DDQ}	ZQ	**B**
C	V_{DDQ}	DQ0	DQS				V_{DD}	V_{SS}	V_{DDQ}	**C**
D	V_{SSQ}	DQ4	DQ2				DQ3	DQ5	V_{SSQ}	**D**
E	V_{SS}	V_{DDQ}	DQ6				DQ7	V_{DDQ}	V_{SS}	**E**
F	V_{DD}	NC	ODT				CK	$\overline{CK}$	V_{DD}	**F**
G	V_{SS}	NC	CKE				$\overline{CS}$	NC	TEN	**G**
H	V_{DD}	$\overline{WE}$/A14	$\overline{ACT}$				$\overline{CAS}$/A15	$\overline{RAS}$/A16	V_{SS}	**H**
J	V_{REFCA}	BG0	A10/AP				A12/$\overline{BC}$	BG1	V_{DD}	**J**
K	V_{SS}	BA0	A4				A3	BA1	V_{SS}	**K**
L	$\overline{RESET}$	A6	A0				A1	A5	$\overline{ALERT}$	**L**
M	V_{DD}	A8	A2				A9	A7	V_{PP}	**M**
N	V_{SS}	A11	PAR				NC	A13	V_{DD}	**N**

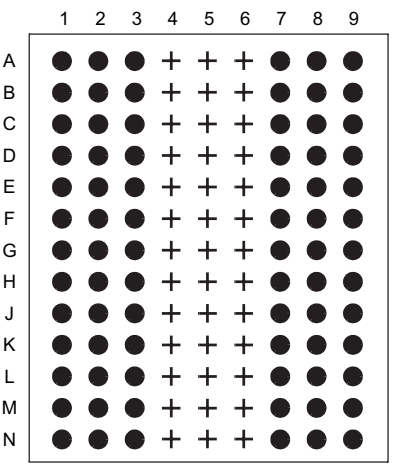
Ball Locations (x8)

● Populated ball

\+ Ball not populated

Top view

(See the balls through the package)



Pin Configurations

96-ball FBGA (x16 configuration)

	1	2	3	4	5	6	7	8	9	
A	V_{DDQ}	V_{SSQ}	DQ8				$\overline{DQSU}$	V_{SSQ}	V_{DDQ}	**A**
B	V_{PP}	V_{SS}	V_{DD}				DQSU	DQ9	V_{DD}	**B**
C	V_{DDQ}	DQ12	DQ10				DQ11	DQ13	V_{SSQ}	**C**
D	V_{DD}	V_{SSQ}	DQ14				DQ15	V_{SSQ}	V_{DDQ}	**D**
E	V_{SS}	$\overline{UDM}/\overline{UDBI}$	V_{SSQ}				$\overline{LDM}/\overline{LDBI}$	V_{SSQ}	V_{SS}	**E**
F	V_{SSQ}	V_{DDQ}	$\overline{DQSL}$				DQ1	V_{DDQ}	ZQ	**F**
G	V_{DDQ}	DQ0	DQSL				V_{DD}	V_{SS}	V_{DDQ}	**G**
H	V_{SSQ}	DQ4	DQ2				DQ3	DQ5	V_{SSQ}	**H**
J	V_{DD}	V_{DDQ}	DQ6				DQ7	V_{DDQ}	V_{DD}	**J**
K	V_{SS}	CKE	ODT				CK	$\overline{CK}$	V_{SS}	**K**
L	V_{DD}	$\overline{WE}$/A14	$\overline{ACT}$				$\overline{CS}$	$\overline{RAS}$/A16	V_{DD}	**L**
M	V_{REFCA}	BG0	A10/AP				A12/$\overline{BC}$	$\overline{CAS}$/A15	V_{SS}	**M**
N	V_{SS}	BA0	A4				A3	BA1	TEN	**N**
P	$\overline{RESET}$	A6	A0				A1	A5	$\overline{ALERT}$	**P**
R	V_{DD}	A8	A2				A9	A7	V_{PP}	**R**
T	V_{SS}	A11	PAR				NC	A13	V_{DD}	**T**

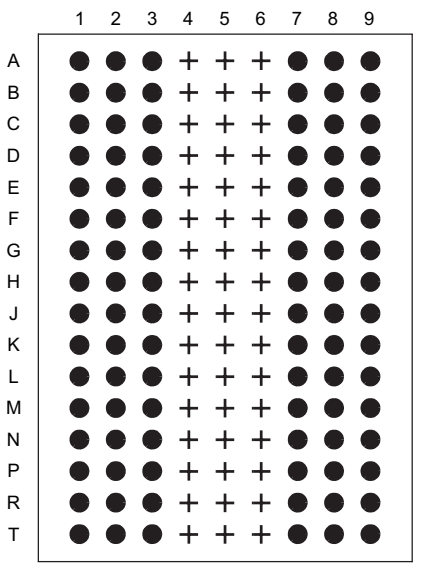
Ball Locations (x16)

● Populated ball

\+ Ball not populated

Top view

(See the balls through the package)



Signal Pin Description

Pin	Type	Function
CK, $\overline{CK}$	Input	**Clock :** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$.
CKE	Input	**Clock Enable :** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (Row Active in any bank). CKE is asynchronous for self refresh exit. After V_{REFCA} has become stable during the power on and initialization sequence, it must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self -Refresh.
$\overline{CS}$	Input	**Chip Select :** All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command code.
ODT	Input	**On Die Termination :** ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When ODT is enabled, on-die termination (RTT) is applied only to each DQ, DQS, $\overline{DQS}$, $\overline{DM}$/$\overline{DBI}$/TDQS, and $\overline{TDQS}$ signal for x4, x8 configurations (when the TDQS function is enabled via mode register). For the x16 configuration, RTT is applied to each DQ, DQSU, $\overline{DQSU}$, DQSL, $\overline{DQSL}$, $\overline{UDM}$, and $\overline{LDM}$ signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
BA0 - BA2	Input	**Bank Address Inputs :** BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
BG0 - BG1	Input	**Bank group address inputs:** Define the bank group to which a REFRESH, ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. X4/8 have BG0 and BG1 but X16 has only BG0.
$\overline{ACT}$	Input	Command input: $\overline{ACT}$ defines the Activation command being entered along with $\overline{CS}$. The input into $\overline{RAS}$/A16, $\overline{CAS}$/A15 and $\overline{WE}$/A14 will be considered as Row Address A16, A15 and A14
$\overline{RAS}$ / A16 $\overline{CAS}$ / A15 $\overline{WE}$ / A14	Input	**Command Inputs :** $\overline{RAS}$/A16, $\overline{CAS}$/A15 and $\overline{WE}$/A14 (along with $\overline{CS}$) define the command being entered. Those pins have multi function. For example, for activation with $\overline{ACT}$ Low, those are Addressing like A16,A15 and A14 but for non-activation command with $\overline{ACT}$ High, those are Command pins for Read, Write and other command defined in command truth table.
A10 / AP	Input	**Autoprecharge :** A10 is sampled during Read/Write commands to determine whether Autoprecharge should be per-formed to the accessed bank after the Read/Write operation. (HIGH:Autoprecharge; LOW: No Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). if only one bank is to be precharged, the bank is selected by bank addresses.
A12 / $\overline{BC}$	Input	**Burst Chop :** A12 is sampled during Read and Write commands to determine if burst chop(on-the-fly) will be per-formed. (HIGH : no burst chop, LOW : burst chopped). See command truth table for details.
A0 - A17	Input	**Address Inputs :** Provided the row address for Active commands and the column address for Read / Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/$\overline{BC}$, $\overline{WE}$/A14, $\overline{CAS}$/A15, $\overline{RAS}$/A16 have additional functions, see individual entries in this table). The address inputs also provide the op-code during the MODE REGISTER SET command. A16 is used on some 8Gb and 16Gb parts while A17 is only used on some 16Gb parts.

Pin	Type	Function
PAR	Input	**Parity for command and address :** DDR4 Supports Even Parity check in DRAM with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with $\overline{ACT}$, $\overline{RAS}$/A16, $\overline{CAS}$/A15, $\overline{WE}$/A14, A12/$\overline{BC}$, A10/$\overline{AP}$, A17-A0, BA0-BA1, and BG0-BG1. Input parity should maintain at the rising edge of the clock and at the same time with command & address with $\overline{CS}$ LOW. Control pins NOT covered by the PARITY signal are $\overline{CS}$, CKE, and ODT. Unused address pins that are density and configuration specific should be treated internally as 0s by the DRAM parity logic.
DQ	Input/output	**Data input/output :** Bidirectional data bus. DQ represents DQ[3:0], DQ[7:0], and DQ[15:0] for the x4, x8, and x16 configurations, respectively. If Write CRC is enabled via Mode register then the Write CRC code is added at the end of Data Burst. Either anyone or all DQ0, DQ1, DQ2, and DQ3 is used as monitoring of internal Vref level during test via Mode Register Setting MR4[4]=High, training times change when enabled. During this mode, RTT value should be set to Hi-Z. This measurement is for verification purposes and is NOT an external voltage supply pin.
DQS, $\overline{DQS}$ DQSL, $\overline{DQSL}$ DQSU, $\overline{DQSU}$	Input/ Output	**Data Strobe :** Output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQ0-DQ7; DQSU corresponds to the data on DQ8-DQ15. For the x4 and x8 configurations, DQS corresponds to the data on DQ0-DQ3 and DQ0-DQ7 respectively. DDR4 SDRAM supports a differential data strobe only and does not support a single-ended data strobe.
TDQS, $\overline{TDQS}$	Output	**Termination Data Strobe :** TDQS/$\overline{TDQS}$ is applicable for x8 DRAMs only. When enabled via Mode Register A11=1 in MR1, DRAM will enable the same termination resistance function on TDQS/$\overline{TDQS}$ that is applied to DQS/$\overline{DQS}$. When the TDQS function is disabled via the mode register, the $\overline{DM}$/$\overline{DBI}$/TDQS pin will provide the data mask ($\overline{DM}$) function or Data Bus Inversion ($\overline{DBI}$) depending on MR5, and the $\overline{TDQS}$ pin is not used. The TDQS function must be disabled in the mode register for both the x4 and x16 configurations.
$\overline{DM}$ $\overline{LDM}$, $\overline{UDM}$	Input	**Input Data Mask :** $\overline{DM}$ is an input mask signal for write data. Input data is masked when $\overline{DM}$ is sampled LOW coincident with that input data during a Write access. $\overline{DM}$ is sampled on both edges of DQS. $\overline{DM}$ is muxed with $\overline{DBI}$ function by Mode Register A[12:10] setting in MR5. For x8 device, the function of $\overline{DM}$ or TDQS is enabled by Mode Register A11 setting in MR1. $\overline{DBI}$ is an input/output identifing whether to store/output the true or inverted data. If $\overline{DBI}$ is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if $\overline{DBI}$ is HIGH. DM is not supported in X4.
$\overline{DBI}$ $\overline{UDBI}$, $\overline{LDBI}$	Input/Output	**DBI input/output :** Data bus inversion. DBI is an input/output signal used for data bus inversion in the x8 configuration. $\overline{UDBI}$ and $\overline{LDBI}$ are used in the x16 configuration; $\overline{UDBI}$ is associated with DQ8-DQ15, and LDBI is associated with DQ0-DQ7. The DBI feature is not supported on x4 configurations. $\overline{DBI}$ can be configured for both READ (output) and WRITE (input) operations depending on the mode register settings. The DM, DBI, and TDQS functions are enabled by mode egister settings. See Data Bus Inversion (DBI).
$\overline{ALERT}$	Output	**Alert output :** It has multi functions such as CRC error flag , Command and Address Parity error flag as Output signal. If there is error in CRC, then $\overline{ALERT}$ goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then $\overline{ALERT}$ goes LOW for relatively long period until on going DRAM internal recovery transaction to complete. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, open-drain $\overline{ALERT}$ Pin must be bounded to VDD on board.
TEN	Input	**Connectivity test mode :** Connectivity Test Mode is active when TEN is HIGH, and inactive when TEN is LOW. TEN must be LOW during normal operation. TEN is a CMOS rail-to-rail signal with AC HIGH and LOW at 80% and 20% of VDD (960mV for DC HIGH and 240mV for DC LOW). Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS.
ZQ	Input	**Reference pin for ZQ calibration :** This ball is tied to an external 240Ω resistor (RZQ), which is tied to VSSQ.

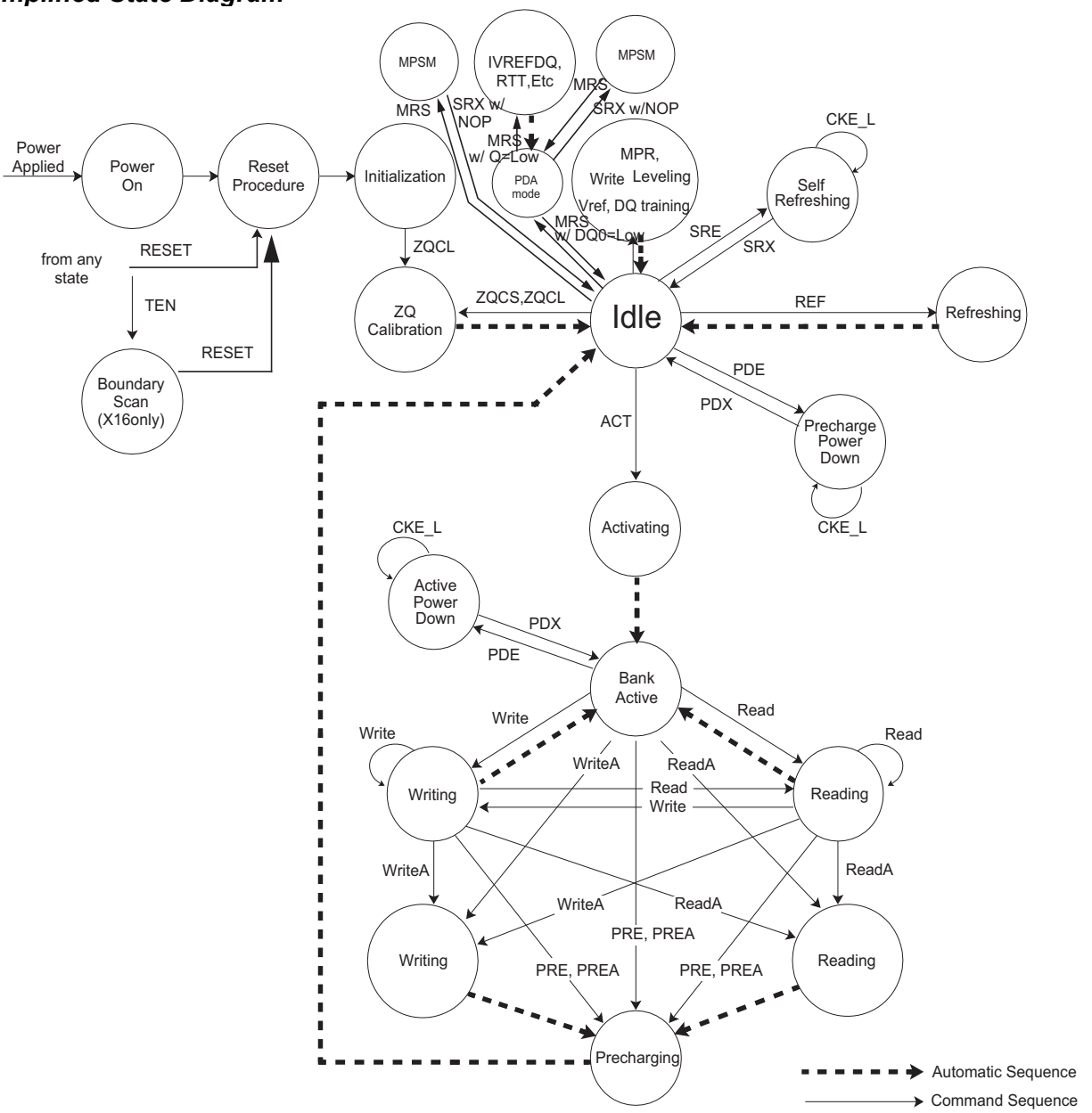
Pin	Type	Function
$\overline{\text{RESET}}$	Input	**Active Low Asynchronous Reset :** Reset is active when $\overline{\text{RESET}}$ is LOW, and inactive when $\overline{\text{RESET}}$ is HIGH. $\overline{\text{RESET}}$ must be HIGH during normal operation. $\overline{\text{RESET}}$ is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD, i.e. 1.20V for DC high and 0.30V for DC low.
VPP	Supply	**DRAM activating power supply :** 2.5V (2.375V min , 2.75V max)
VDD	Supply	**Power Supply :** 1.2V ± 0.060V
VDDQ	Supply	**DQ Power Supply :** 1.2V ± 0.060V
VSS	Supply	**Ground**
VSSQ	Supply	**DQ Ground**
VREFCA	Supply	**Reference Voltage for CA**
NC	-	**No Connect :** No internal electrical connection is present.
NF	-	**No function :** May have internal connection present, but has no function.
RFU	-	Reserved for future use.

NOTE :

1. Input only pins (BG0-BG1, BA0-BA2, A0-A17, $\overline{\text{RAS}}$/A16, $\overline{\text{CAS}}$/A15, $\overline{\text{WE}}$/A14, $\overline{\text{CS}}$, CKE, ODT and $\overline{\text{RESET}}$) do not supply termination.
2. The signal may show up in a different symbol but it indicates the same thing. e.g., /CK = CK# = #CK = $\overline{\text{CK}}$ = CKb = CK_n, /DQS = DQS# = #DQS = $\overline{\text{DQS}}$ = DQSb = DQS_n, /CS = CS# = #CS = $\overline{\text{CS}}$ = CSb = CS_n.

Functional Description

Simplified State Diagram



Abbreviation	Function	Abbreviation	Function	Abbreviation	Function
ACT	Activate	Read	RD,RDS4, RDS8	PDE	Enter Power-down
PRE	Precharge	Read A	RDA, RDAS4, RDAS8	PDX	Exit Power-down
PREA	PRECHARGE All	Write	WR, WRS4, WRS8 with/without CRC	SRE	Self-Refresh entry
MRS	Mode Register Set	Write A	WRA,WRAS4, WRAS8 with/without CRC	SRX	Self-Refresh exit
REF	Refresh, Fine granularity Refresh	RESET_n	Start RESET procedure	MPR	Multi Purpose Register
TEN	Boundary Scan Mode Enable				

NOTE This simplified State Diagram is intended to provide an overview of the possible state transitions and the commands to control them. In particular, situations involving more than on bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.

Basic Functionality

The DDR4 SDRAM is a high-speed dynamic random-access memory internally conured as sixteen-banks, 4 bank group with 4 banks for each bank group for x4/x8 and eight-banks, 2 bank group with 4 banks for each bankgroup for x16 DRAM. The DDR4 SDRAM uses a 8n prefetch architecture to achieve high-speed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR4 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write operation to the DDR4 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an ACTIVATE Command, which is then followed by a Read or Write command. The address bits registered coincident with the ACTIVATE Command are used to select the bank and row to be activated (BG0-BG1 in x4/8 and BG0 in x16 select the bankgroup; BA0-BA1 select the bank; A0-A15 select the row; refer to Addressing section for more details. The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register.

Prior to normal operation, the DDR4 SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions, and device operation.

RESET and Initialization Sequence

For power-up and reset initialization, in order to prevent DRAM from functioning improperly, default values for the following MR settings are defined:

Gear down mode (MR3 A[3]): 0 = 1/2 Rate
Per DRAM Addressability (MR3 A[4]): 0 = Disable
Max Power Saving Mode (MR4 A[1]): 0 = Disable
CS to Command/Address Latency (MR4 A[8:6]): 000 = Disable
CA Parity Latency Mode (MR5 A[2:0]): 000 = Disable

Power-up and Initialization Sequence

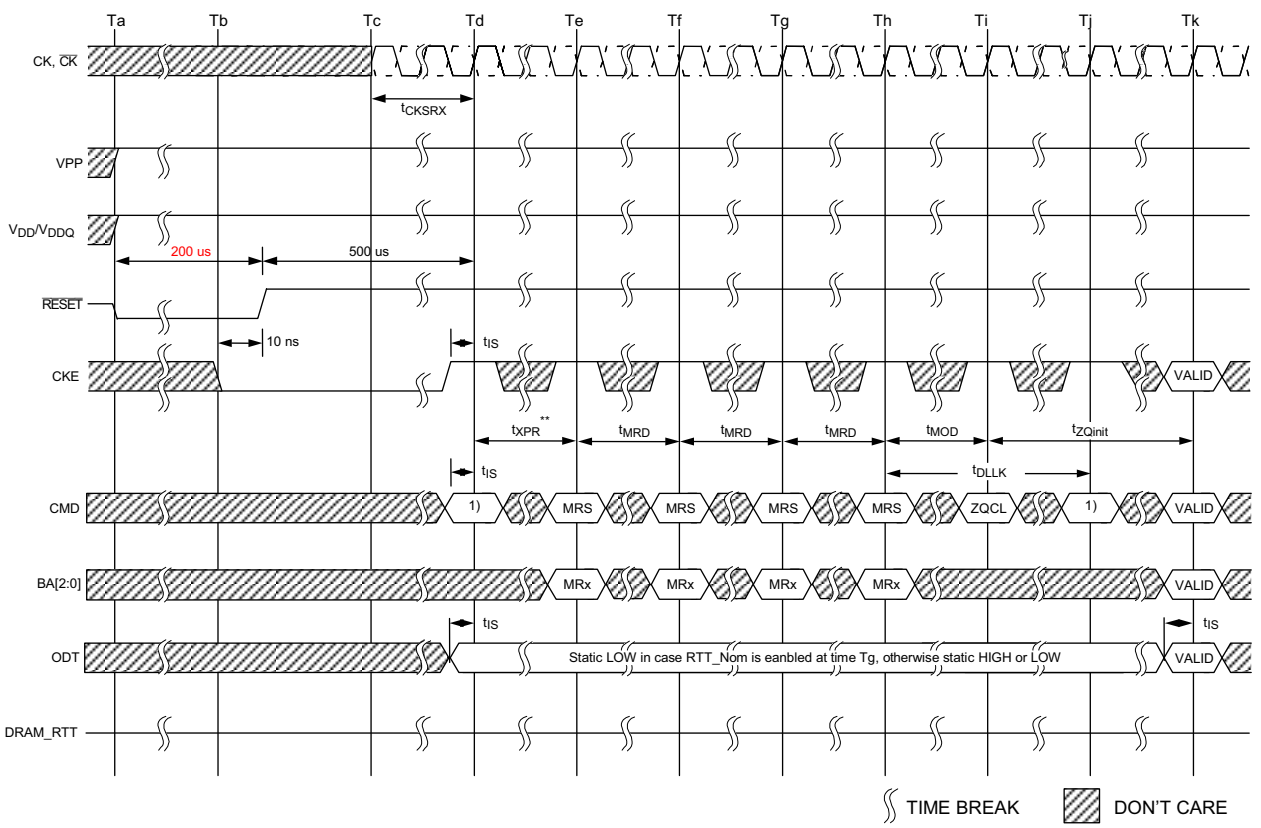
The following sequence is required for power-up and initialization:

1. Apply power ($\overline{\text{RESET}}$ is recommended to be maintained below 0.2 x VDD; all other inputs may be undefined). $\overline{\text{RESET}}$ needs to be maintained for minimum 200us with stable power. CKE is pulled LOW anytime before $\overline{\text{RESET}}$ is being deasserted (MIN time 10ns). The power voltage ramp time between 300mV to VDD, min must be no greater than 200ms, and, during the ramp, VDD must be greater than or equal to VDDQ and (VDD - VDDQ) < 0.3V. VPP must ramp at the same time or earlier than VDD, and VPP must be equal to or higher than VDD at all times.
   - VDD and VDDQ are driven from a single power converter output, AND
   - The voltage levels on all pins other than VDD,VDDQ,VSS,VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side. In addition, VTT is limited to TBDV max once power ramp is finished, AND
   - VREFCA tracks TBD.

   or
   - Apply VDD without any slope reversal before or at the same time as VDDQ.
   - Apply VDDQ without any slope reversal before or at the same time as VTT & VREFCA.
   - Apply VPP without any slope reversal before or at the same time as VDD.
   - The voltage levels on all pins other than VDD,VDDQ,VSS,VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.
2. After $\overline{\text{RESET}}$ is de-asserted, wait for another 500us until CKE becomes active. During this time, the DRAM will start internal state initialization; this will be done independently of external clocks.
3. Clocks (CK, $\overline{\text{CK}}$) need to be started and stabilized for at least 10ns or 5tCK (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding setup time to clock (tIS) must be met. Also a NOP or Deselect

command must be registered (with tIS set up time to clock) before CKE goes active. Once the CKE registered “High” after Reset, CKE needs to be continuously registered “High” until the initialization sequenceis finished, including expiration of tDLLK and tZQinit.

4. The DDR4 SDRAM keeps its on-die termination in high-impedance state as long as $\overline{\text{RESET}}$ is asserted. Further, the SDRAMkeeps its on-die termination in high impedance state after $\overline{\text{RESET}}$ deassertion until CKE is registered HIGH. The ODT inputsignal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signalmay be statically held at either LOW or HIGH. If RTT_NOM is to be enabled in MR1 the ODT input signal must be statically heldLOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expirationof tDLLK and tZQinit.
5. After CKE is registered high, wait minimum of Reset CKE Exit time, tXPR, before issuing the first MRS command to load mode register.(tXPR=Max(tXS, 5tCK))
6. Issue MRS Command to load MR3 with all application settings(To issue MRS command to MR3, provide “Low” to BG0, “High” to BA1, BA0)
7. Issue MRS command to load MR6 with all application settings (To issue MRS command to MR6, provide “Low” to BA0, “High” to BG0, BA1)
8. Issue MRS command to load MR5 with all application settings (To issue MRS command to MR5, provide “Low” to BA1, “High” to BG0, BA0)
9. Issue MRS command to load MR4 with all application settings (To issue MRS command to MR4, provide “Low” to BA1, BA0, “High” to BG0)
10. Issue MRS command to load MR2 with all application settings (To issue MRS command to MR2, provide “Low” to BG0, BA0, “High” to BA1)
11. Issue MRS command to load MR1 with all application settings (To issue MRS command to MR1, provide “Low” to BG0, BA1, “High” to BA0)
12. Issue MRS command to load MR0 with all application settings (To issue MRS command to MR0, provide “Low” to BG0, BA1, BA0)
13. Issue ZQCL command to starting ZQ calibration
14. Wait for both tDLLK and tZQ init completed
15. The DDR4 SDRAM is now ready for read/Write training (include VREF training and Write leveling).

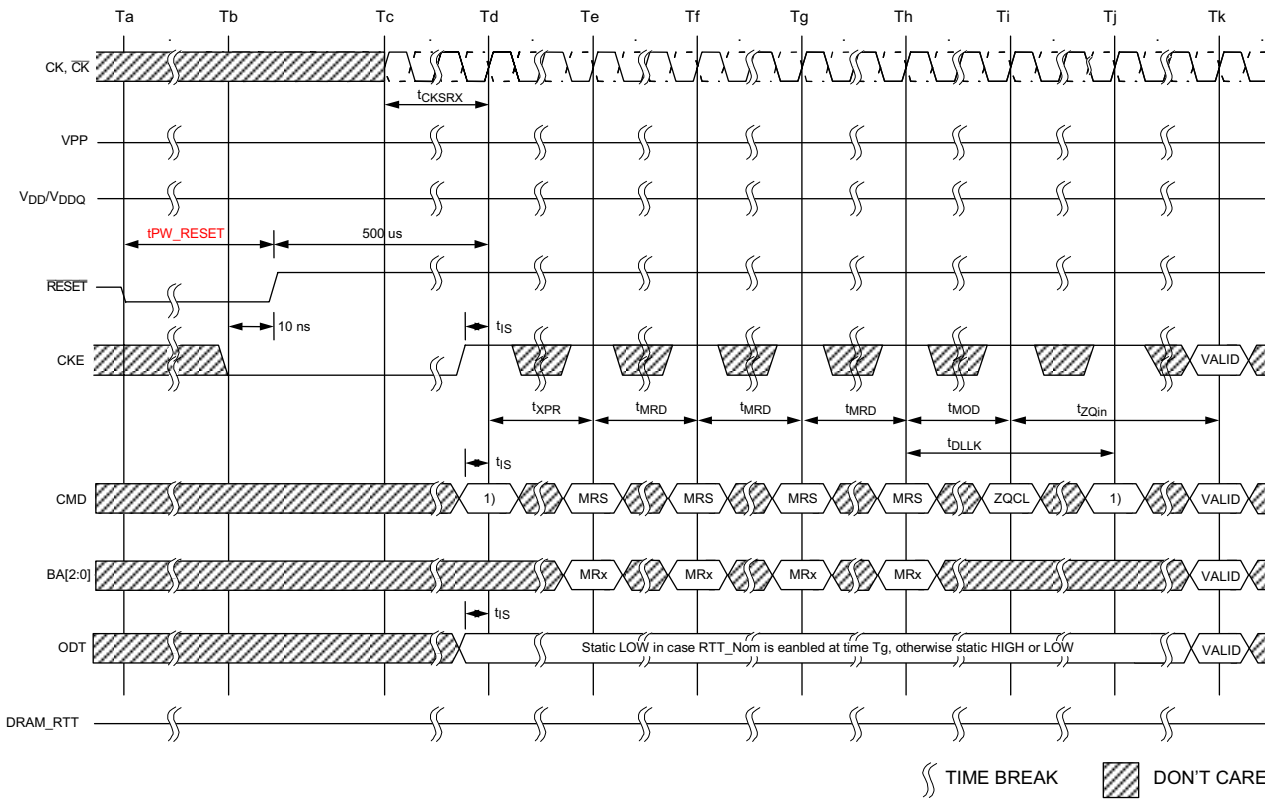


NOTE 1 From the time point Td until Tk, a DES command must be applied between MRS and ZQCL commands.
NOTE 2 MRS commands must be issued to all mode registers that have defined settings.
NOTE 3 In general, there is no specific sequence for setting the MRS locations (except for dependent or co-related features, such as ENABLE DLL in MR1 prior to RESET DLL in MR0, for example).
NOTE 4 TEN is not shown; however, it is assumed to be held LOW.

Reset and Initialization with Stable Power

The following sequence is required for RESET at no power interruption initialization:

1. Assert RESET below 0.2 x VDD anytime when reset is needed (all other inputs may be undefined). RESET needs to be maintained for minimum tPW_RESET. CKE is pulled low before RESET being de-asserted (minimum time 10ns).
2. Follow steps 2 to 10 in “Power-up Initialization Sequence”.
3. The Reset sequence is now completed, DDR4 SDRAM is ready for Read/Write training (include VREF training and Write leveling).

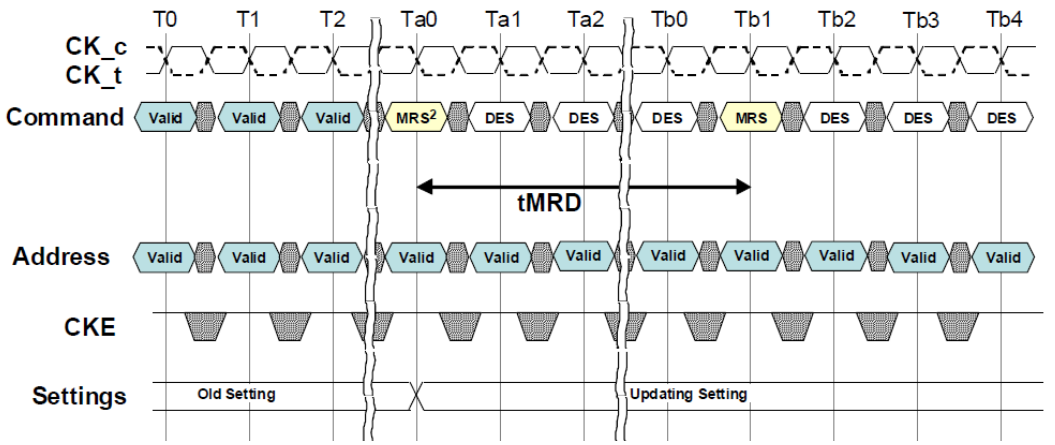


NOTE 1 From the time point Td until Tk, a DES command must be applied between MRS and ZQCL commands.
NOTE 2 MRS commands must be issued to all mode registers that have defined settings.
NOTE 3 In general, there is no specific sequence for setting the MRS locations (except for dependent or co-related features, such as ENABLE DLL in MR1 prior to RESET DLL in MR0,for example).
NOTE 4 TEN is not shown; however, it is assumed to be held LOW.

Register Definition

Programming the mode registers

For application flexibility, various functions, features, and modes are programmable in seven Mode Registers, provided by the DDR4 SDRAM, as user defined variables and they must be programmed via a Mode Register Set (MRS) command. The mode registers are divided into various fields depending on the functionality and/or modes. As not all the Mode Registers (MR#) have default values defined, contents of Mode Registers must be initialized and/or re-initialized, i. e. written, after power up and/or reset for proper operation. Also the contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS command and DLL Reset do not affect array contents, which means these commands can be executed any time after power-up without affecting the array contents. The mode register set command cycle time, tMRD is required to complete the write operation to the mode register and is the minimum time required between two MRS commands.



NOTE 1 This timing diagram shows C/A Parity Latency mode is “Disable” case.

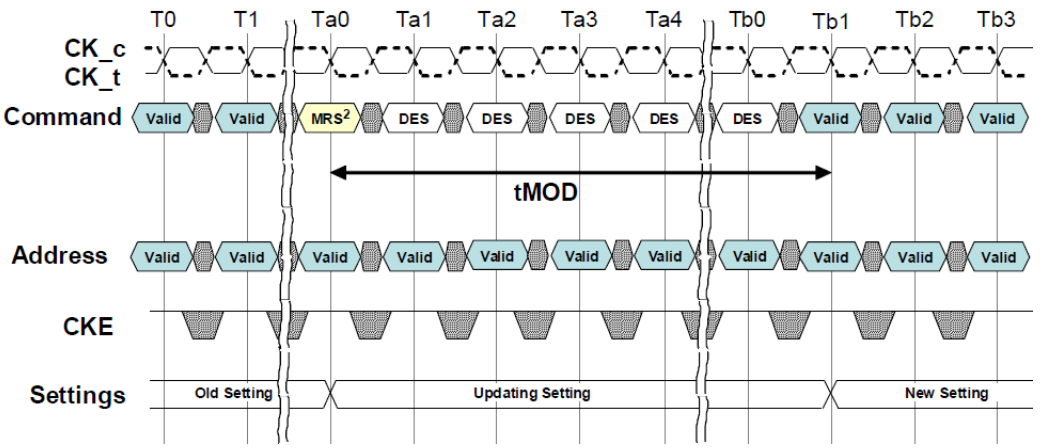
NOTE 2 List of MRS commands exception that do not apply to tMRD

- Gear down mode
- C/A Parity Latency mode
- CS to Command/Address Latency mode
- Per DRAM Addressability mode
- VREFDQ training Value, VREFDQ Training mode and VREFDQ training Range

Some of the Mode Register setting affect to address/command/control input functionality. These case, next MRS command can be allowed when the function updating by current MRS command completed.

This type of MRS command does not apply tMRD timing to next MRS command is listed in Note 2 of tMRD figure. These MRS command input cases have unique MR setting procedure, so refer to individual function description.

The most MRS command to Non-MRS command delay, tMOD, is required for the DRAM to update the features, and is the minimum time required from an MRS command to a non-MRS command excluding DES.



NOTE 1 This timing diagram shows C/A Parity Latency mode is “Disable” case.

NOTE 2 List of MRS commands exception that do not apply to tMOD

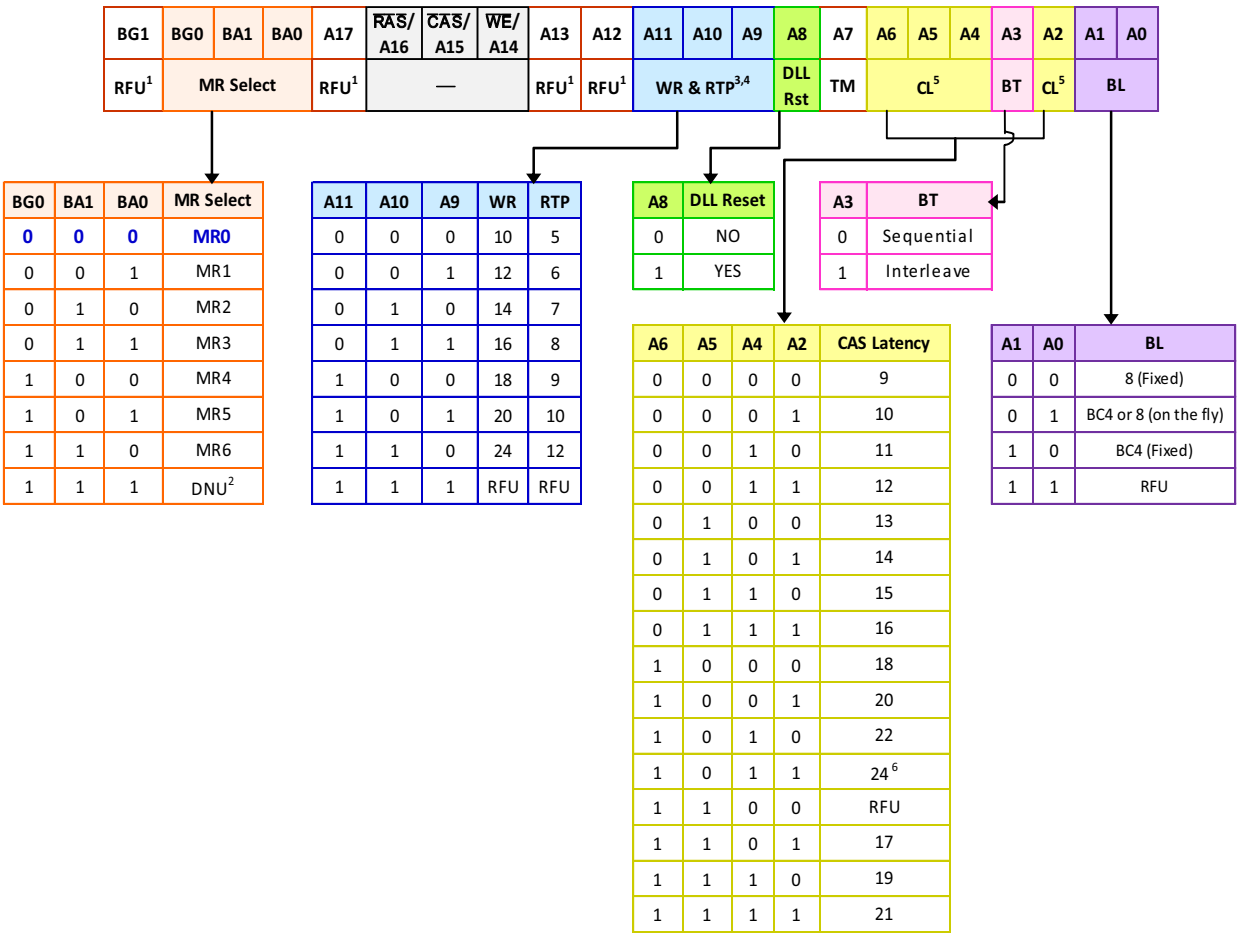
- DLL Enable, DLL Reset
- VREFDQ training Value, internal VREF Monitor, VREFDQ Training mode and VREFDQ training Range
- Gear down mode
- Per DRAM Addressability mode
- Maximum power saving mode
- CA Parity mode

The mode register contents can be changed using the same command and timing requirements during normal operation as long as the DRAM is in idle state, i.e., all banks are in the precharged state with tRP satisfied, all data bursts are completed and CKE is high prior to writing into the mode register. For MRS command, If RTT_Nom function is intended to change (enable to disable and vice versa) or already enabled in DRAM MR, ODT signal must be registered Low ensuring RTT_NOM is in an off state prior to MRS command affecting RTT_NOM turn-on and off timing. Refer to note2 of tMOD figure for this type of MRS. The ODT signal may be registered high after tMOD has expired. ODT signal is a don’t care during MRS command if DRAM RTT_Nom function is disabled in the mode register prior and after an MRS command.

Some of the mode register setting cases, function updating takes longer than tMOD. This type of MRS does not apply tMOD timing to next valid command excluding DES is listed in note 2 of tMOD figure. These MRS command input cases have unique MR setting procedure, so refer to individual function description.

Mode Register

Mode Register MR0



BG0	BA1	BA0	MR Select
0	0	0	MR0
0	0	1	MR1
0	1	0	MR2
0	1	1	MR3
1	0	0	MR4
1	0	1	MR5
1	1	0	MR6
1	1	1	DNU[2]

A11	A10	A9	WR	RTP
0	0	0	10	5
0	0	1	12	6
0	1	0	14	7
0	1	1	16	8
1	0	0	18	9
1	0	1	20	10
1	1	0	24	12
1	1	1	RFU	RFU

A8	DLL Reset
0	NO
1	YES

A3	BT
0	Sequential
1	Interleave

A6	A5	A4	A2	CAS Latency
0	0	0	0	9
0	0	0	1	10
0	0	1	0	11
0	0	1	1	12
0	1	0	0	13
0	1	0	1	14
0	1	1	0	15
0	1	1	1	16
1	0	0	0	18
1	0	0	1	20
1	0	1	0	22
1	0	1	1	24[6]
1	1	0	0	RFU
1	1	0	1	17
1	1	1	0	19
1	1	1	1	21

A1	A0	BL
0	0	8 (Fixed)
0	1	BC4 or 8 (on the fly)
1	0	BC4 (Fixed)
1	1	RFU

NOTE 1 Please refer to addressing table. If the address is available, it must be programmed to 0 during MRS
NOTE 2 Reserved for Register control word setting. DRAM ignores MR command with BG0,BA[1:0]=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.
NOTE 3 WR (write recovery for autoprecharge)min in clock cycles is calculated by dividing tWR(in ns) by tCK(in ns) and rounding up to the next integer:WRmin[cycles] = Roundup(tWR[ns] / tCK[ns]). The WR value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with tRP to determine tDAL.
NOTE 4 The table shows the encodings for Write Recovery and internal Read command to Precharge command delay. For actual Write recovery timing, please refer to AC timing table.
NOTE 5 The table only shows the encodings for a given Cas Latency. For actual supported Cas Latency, please refer to speed bin tables for each frequency.
NOTE 6 When CL is equal to 24 or more than 24, AL does not support CL-1.

Burst Length, Type and Order

Accesses within a given burst may be programmed to sequential or interleaved order. The burst type is selected via bit A3 of Mode Register MR0. The ordering of accesses within a burst is determined by the burst length, burst type, and the starting column address as shown in the following table. The burst length is defined by bits A0-A1 of Mode Register MR0. Burst length options include fixed BC4, fixed BL8, and 'on the fly' which allows BC4 or BL8 to be selected coincident with the registration of a Read or Write command via A12/$\overline{BC}$.

Burst Length	Read/ Write	Starting Column Adress(A2,A1,A0)	burst type = Sequential (decimal) A3=0	burst type = Interleaved (decimal) A3=1	NOTE
BC4	Read	0 0 0	0,1,2,3,T,T,T,T	0,1,2,3,T,T,T,T	1,2,3
		0 0 1	1,2,3,0,T,T,T,T	1,0,3,2,T,T,T,T	1,2,3
		0 1 0	2,3,0,1,T,T,T,T	2,3,0,1,T,T,T,T	1,2,3
		0 1 1	3,0,1,2,T,T,T,T	3,2,1,0,T,T,T,T	1,2,3
		1 0 0	4,5,6,7,T,T,T,T	4,5,6,7,T,T,T,T	1,2,3
		1 0 1	5,6,7,4,T,T,T,T	5,4,7,6,T,T,T,T	1,2,3
		1 1 0	6,7,4,5,T,T,T,T	6,7,4,5,T,T,T,T	1,2,3
		1 1 1	7,4,5,6,T,T,T,T	7,6,5,4,T,T,T,T	1,2,3
	Write	0 v v	0,1,2,3,X,X,X,X	0,1,2,3,X,X,X,X	1,2,4,5
		1 v v	4,5,6,7,X,X,X,X	4,5,6,7,X,X,X,X	1,2,4,5
BL8	Read	0 0 0	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2
		0 0 1	1,2,3,0,5,6,7,4	1,0,3,2,5,4,7,6	2
		0 1 0	2,3,0,1,6,7,4,5	2,3,0,1,6,7,4,5	2
		0 1 1	3,0,1,2,7,4,5,6	3,2,1,0,7,6,5,4	2
		1 0 0	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3	2
		1 0 1	5,6,7,4,1,2,3,0	5,4,7,6,1,0,3,2	2
		1 1 0	6,7,4,5,2,3,0,1	6,7,4,5,2,3,0,1	2
		1 1 1	7,4,5,6,3,0,1,2	7,6,5,4,3,2,1,0	2
	Write	v v v	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2,4

NOTE 1 In case of burst length being fixed to 4 by MR0 setting, the internal write operation starts two clock cycles earlier than for the BL8 mode. This means that the starting point for tWR and tWTR will be pulled in by two clocks. In case of burst length being selected on-the-fly via A12/$\overline{BC}$, the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for tWR and tWTR will not be pulled in by two clocks.

NOTE 2 0...7 bit number is value of CA[2:0] that causes this bit to be the first read during a burst.

NOTE 3 T : Output driver for data and strobes are in high impedance.

NOTE 4 V : A valid logic level (0 or 1), but respective buffer input ignores level on input pins.

NOTE 5 X : Don't Care.

CAS Latency (CL)

The CAS latency setting is defined in the MR0 Register Definition table. CAS latency is the delay, in clock cycles, between the internal READ command and the availability of the first bit of output data. DDR4 SDRAM does not support any half-clock latencies. The overall read latency (RL) is defined as additive latency (AL) + CAS latency (CL); RL = AL + CL.

Test Mode

The normal operating mode is selected by MR0[7] and all other bits set to the desired values shown in the MR0 Register Definition table. Programming MR0[7] to a 1 places the DDR4 SDRAM into a DRAM manufacturer defined test mode that is to be used only by the DRAM manufacturer; and should not be used by the end user. No operations or functionality is specified if MR0[7] = 1.

Write Recovery/Read to Precharge

The programmed WR value MR0[11:9] is used for the auto precharge feature along with tRP to determine tDAL. WR (write recovery for auto precharge) MIN in clock cycles is calculated by dividing tWR (in ns) by tCK (in ns) and rounding up to the next integer:

WRmin[cycles] = roundup (tWR[ns]/tCK[ns])

The WR must be programmed to be equal to or larger than tWR(MIN). When both DM and Write CRC are enabled in the DRAM mode register, the DRAM calculates CRC before sending the write data into the array; tWR values will change when enabled. If there is a CRC error, the DRAM blocks the write operation and discards the data.

RTP (internal READ command to PRECHARGE command delay for auto precharge) min in clock cycles is calculated by dividing tRTP (in ns) by tCK (in ns) and rounding up to the next integer:

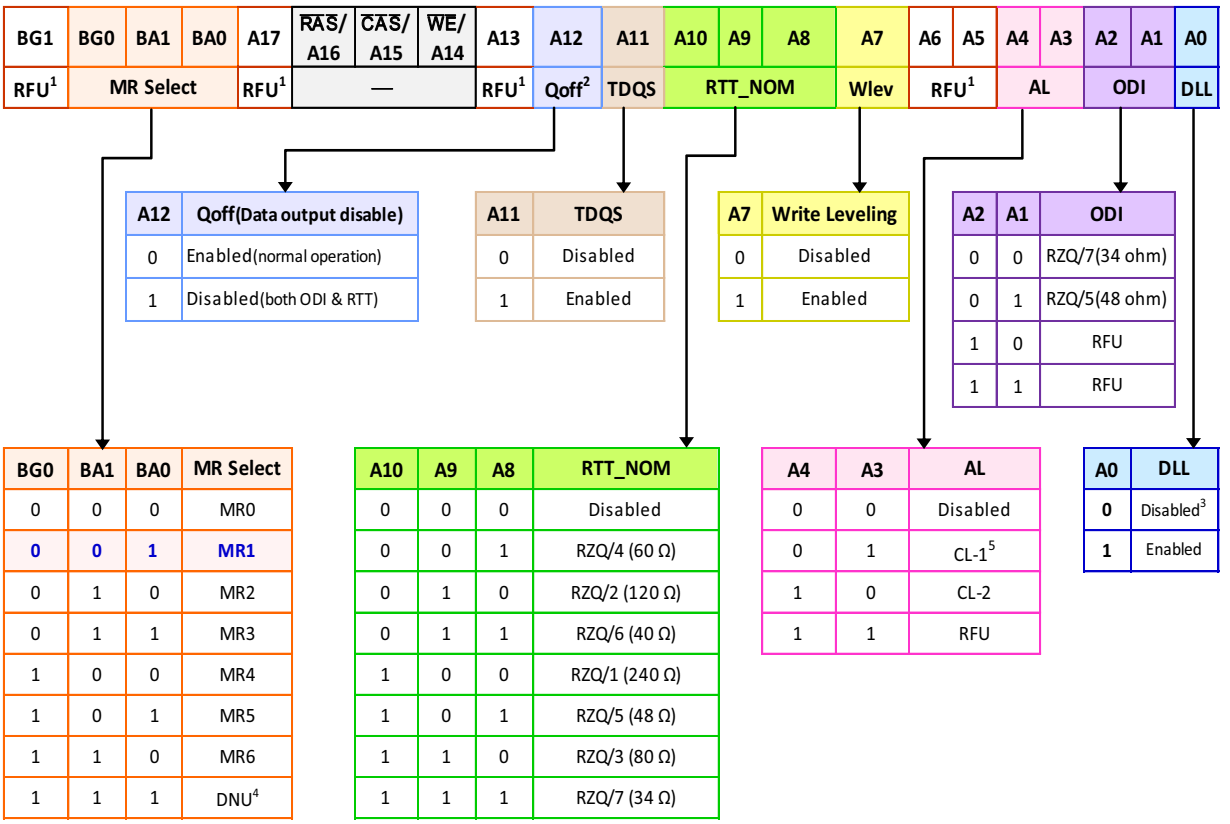
RTPmin[cycles] = roundup (tRTP[ns]/tCK[ns])

The RTP value in the mode register must be programmed to be equal or larger than RTPmin. The programmed RTP value is used with tRP to determine the act timing to the same bank.

DLL Reset

The DLL reset bit is self-clearing, meaning that it returns back to the value of 0 after the DLL reset function has been issued. After the DLL is enabled, a subsequent DLL RESET should be applied. Any time that the DLL reset function is used, tDLLK must be met before any functions that require the DLL can be used (for example, READ commands or ODT synchronous operations).

Mode Register MR1



NOTE 1 Please refer to addressing table. If the address is available, it must be programmed to 0 during MRS

NOTE 2 Outputs disabled - DQs, DQSs, $\overline{\text{DQS}}$s.

NOTE 3 States reversed to “0 as Disable” with respect to DDR4.

NOTE 4 Reserved for Register control word setting. DRAM ignores MR command with BG0,BA[1:0]=111 and doesn’t respond. When RFU MR code setting is inputted, DRAM operation is not defined.

NOTE 5 Not allowed when 1/4 rate geardown mode is enabled.

DLL Enable/DLL Disable

The DLL must be enabled for normal operation and is required during power-up initialization and upon returning to normal operation after having the DLL disabled. During normal operation, (DLL-enabled) with MR1[0], the DLL is automatically disabled when entering the SELF REFRESH operation and is automatically re-enabled upon exit of the SELF REFRESH operation. Any time the DLL is enabled and subsequently reset, tDLLK clock cycles must occur before a READ or SYNCHRONOUS ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tDQSCK, tAON, or tAOF parameters.

During tDLLK, CKE must continuously be registered HIGH. DDR4 SDRAM does not require DLL for any WRITE operation, except when RTT_WR is enabled and the DLL is required for proper ODT operation.

The direct ODT feature is not supported during DLL-off mode. The ODT resistors must be disabled by continuously registering the ODT pin LOW and/or by programming the RTT_NOM bits MR1[9,6,2] = 000 via a MODE REGISTER SET command during DLL-off mode.

The dynamic ODT feature is not supported in DLL-off mode; to disable dynamic ODT externally, use the MRS command to set RTT_WR, MR2[10:9] = 00.

Output Driver Impedance Control

The output driver impedance of the DDR4 SDRAM device is selected by MR1[2,1].

ODT RTT_NOM Values

DDR4 SDRAM is capable of providing three different termination values: RTT_Static, RTT_NOM, and RTT_WR. The nominal termination value, RTT_NOM, is programmed in MR1. A separate value (RTT_WR) may be programmed in MR2 to enable a unique RTT value when ODT is enabled during WRITEs. The RTT_WR value can be applied during WRITEs even when RTT_NOM is disabled. A third RTT value, RTT_Static, is programed in MR5. RTT_Static provides a termination value when the ODT signal is LOW.

Additive Latency (AL)

The additive latency (AL) operation is supported to make command and data bus efficient for sustainable bandwidths in DDR4 SDRAM. In this operation, the DDR4 SDRAM allows a READ or WRITE command (either with or without AUTO PRECHARGE) to be issued immediately after the ACTIVE command. The command is held for the time of AL before it is issued inside the device. The read latency (RL) is controlled by the sum of the AL and CAS latency (CL) register settings. Write latency (WL) is controlled by the sum of the AL and CAS write latency (CWL) register settings.

Write Leveling

For better signal integrity, DDR4 memory modules use fly-by topology for the commands,addresses, control signals, and clocks. Fly-by topology has the benefit of reducing the number of stubs and their length, but it also causes flight-time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the controller to maintain tDQSS, tDSS, and tDSH specifications. Therefore, the DDR4 SDRAM supports a write-leveling feature, which allows the controller to compensate for skew.

Output Disable

The DDR4 SDRAM outputs may be enabled/disabled by MR1[12]. When MR1[12] = 1 is enabled, all output pins (such as DQ, DQS, and $\overline{\text{DQS}}$) are disconnected from the device, which removes any loading of the output drivers. This feature may be useful when measuring module power, for example.For normal operation, set MR1[12] = 0.

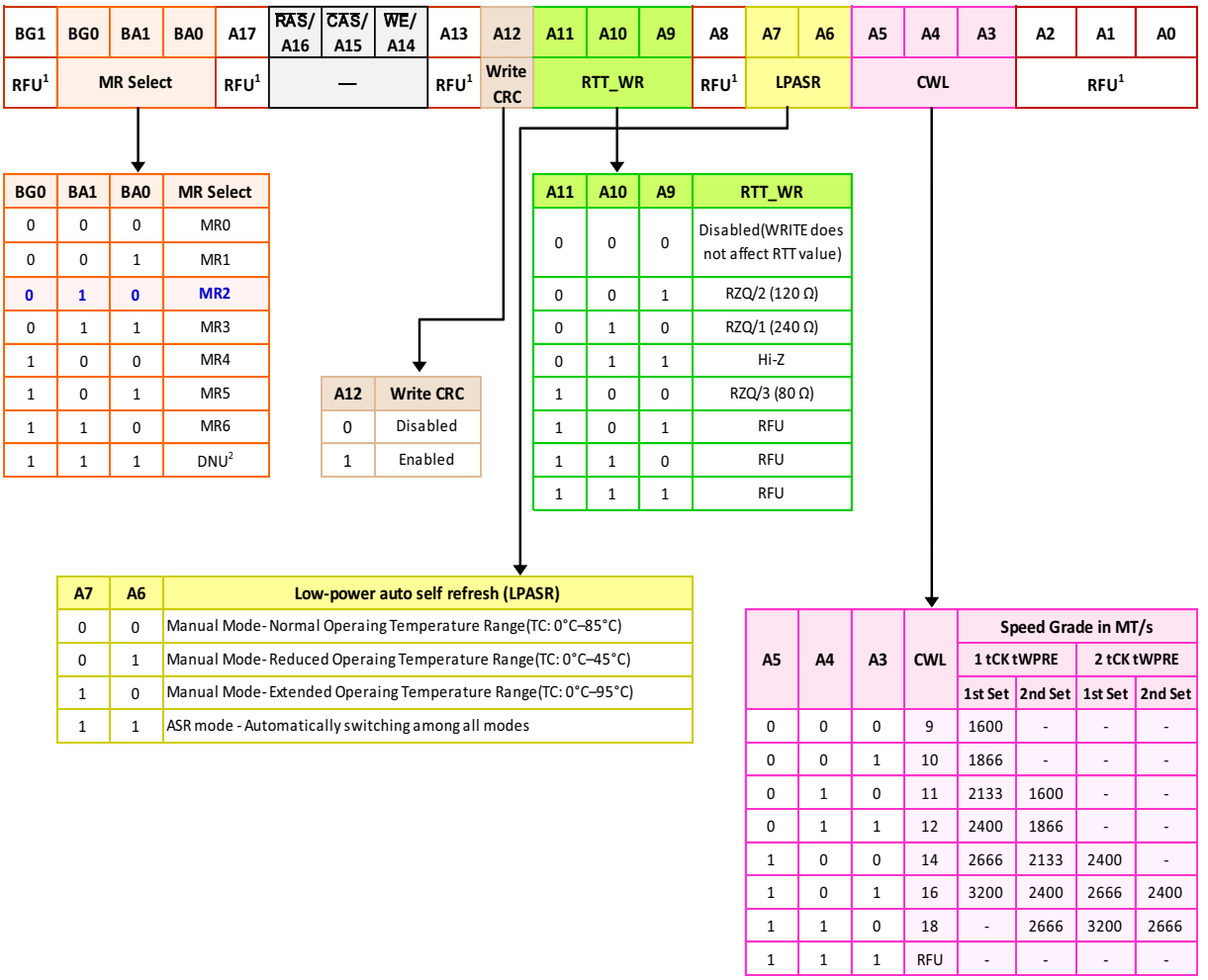
Termination Data Strobe (TDQS)

Termination data strobe (TDQS) is a feature of x8 DDR4 SDRAM and provides additional termination resistance outputs that may be useful in some system configurations. Because the TDQS function is available only in x8 DDR4 SDRAM, it must be disabled for x4 and x16 configurations. TDQS is not supported in x4 or x16 configurations. When enabled via the mode register, the same termination resistance function that is applied to the TDQS and $\overline{\text{TDQS}}$ pins is applied to the DQS and $\overline{\text{DQS}}$ pins.

The TDQS, DBI, and data mask functions share the same pin. When the TDQS function is enabled via the mode register, the data mask and DBI functions are not supported. When the TDQS function is disabled, the data mask and DBI functions can be enabled separately.

TDQS	Data Mask (DM)	WRITE DBI	READ DBI
Disabled	Enabled	Disabled	Enabled or disabled
	Disabled	Enabled	Enabled or disabled
	Disabled	Disabled	Enabled or disabled
Enabled	Disabled	Disabled	Disabled

Mode Register MR2



BG1	BG0	BA1	BA0	A17	RAS/ A16	CAS/ A15	WE/ A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
RFU[1]	MR Select			RFU[1]	—			RFU[1]	Write CRC	RTT_WR			RFU[1]	LPASR		CWL			RFU[1]		

BG0	BA1	BA0	MR Select
0	0	0	MR0
0	0	1	MR1
0	1	0	MR2
0	1	1	MR3
1	0	0	MR4
1	0	1	MR5
1	1	0	MR6
1	1	1	DNU[2]

A12	Write CRC
0	Disabled
1	Enabled

A11	A10	A9	RTT_WR
0	0	0	Disabled(WRITE does not affect RTT value)
0	0	1	RZQ/2 (120 Ω)
0	1	0	RZQ/1 (240 Ω)
0	1	1	Hi-Z
1	0	0	RZQ/3 (80 Ω)
1	0	1	RFU
1	1	0	RFU
1	1	1	RFU

A7	A6	Low-power auto self refresh (LPASR)
0	0	Manual Mode- Normal Operaing Temperature Range(TC: 0°C–85°C)
0	1	Manual Mode- Reduced Operaing Temperature Range(TC: 0°C–45°C)
1	0	Manual Mode- Extended Operaing Temperature Range(TC: 0°C–95°C)
1	1	ASR mode - Automatically switching among all modes

A5	A4	A3	CWL	Speed Grade in MT/s			
				1 tCK tWPRE		2 tCK tWPRE	
				1st Set	2nd Set	1st Set	2nd Set
0	0	0	9	1600	-	-	-
0	0	1	10	1866	-	-	-
0	1	0	11	2133	1600	-	-
0	1	1	12	2400	1866	-	-
1	0	0	14	2666	2133	2400	-
1	0	1	16	3200	2400	2666	2400
1	1	0	18	-	2666	3200	2666
1	1	1	RFU	-	-	-	-

NOTE 1 Please refer to addressing table. If the address is available, it must be programmed to 0 during MRS
NOTE 2 Reserved for Register control word setting. DRAM ignores MR command with BG0, BA[1:0]=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

CAS Write Latency (CWL)

CAS write latency (CWL) is defined by MR2[5:3] as shown in the MR2 Register Definition table. CWL is the delay, in clock cycles, between the internal WRITE command and the availability of the first bit of input data. DDR4 SDRAM does not support any half-clock latencies. The overall write latency (WL) is defined as additive latency (AL) + CAS write latency (CWL); WL = AL + CWL.

Low-Power Auto Self Refresh (LPASR)

Low-power auto self refresh (LPASR) is supported in DDR4 SDRAM. Applications requiring SELF REFRESH operation over different temperature ranges can use this feature to optimize the IDD6 current for a given temperature range as specified in the MR2 Register Definition table.

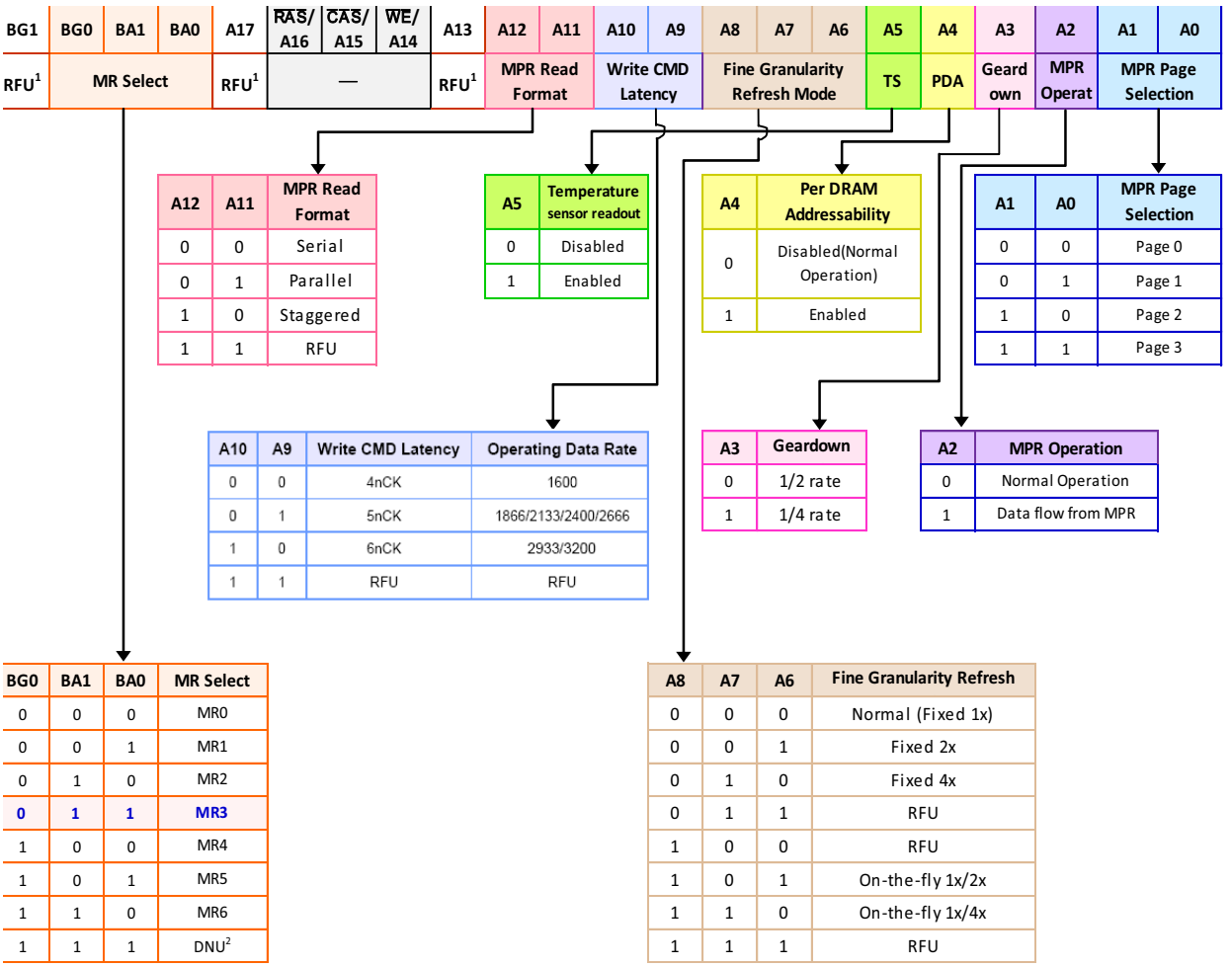
Dynamic ODT (RTT_WR)

In certain applications and to further enhance signal integrity on the data bus, it is desirable to change the termination strength of the DDR4 SDRAM without issuing an MRS command. Configure the Dynamic ODT settings in MR2[11:9]. In write-leveling mode, only RTT_NOM is available.

Write Cyclic Redundancy Check (CRC) Data Bus

The Write cyclic redundancy check (CRC) data bus feature during Writes has been added to DDR4 SDRAM. When enabled via the mode register, the data transfer size goes from the normal 8-bit (BL8) frame to a larger 10-bit UI frame, and the extra 2UIs are used for the CRC information.

Mode Register MR3



NOTE 1 Please refer to addressing table. If the address is available, it must be programmed to 0 during MRS
NOTE 2 Reserved for Register control word setting. DRAM ignores MR command with BG0,BA[1:0]=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

WRITE CMD latency when CRC/DM enabled

The Write Command Latency (WCL) must be set when both Write CRC and DM are enabled for Write CRC persistent mode. This provides the extra time required when completing a Write burst when Write CRC and DM are enabled.

Fine Granularity Refresh Mode

This mode had been added to DDR4 to help combat the performance penalty due to refresh lockout at high densities. Shortening tRFC and increasing cycle time allows more accesses to the chip and can produce higher bandwidth.

Temp Sensor Status

This mode directs the DRAM to update the temperature sensor status at MPR Page 2, MPR0 [4,3]. The temperature sensor setting should be updated within 32ms; at the time of MPR Read of the Temperature Sensor Status bits, the tem-

perature sensor status should be no older than 32ms.

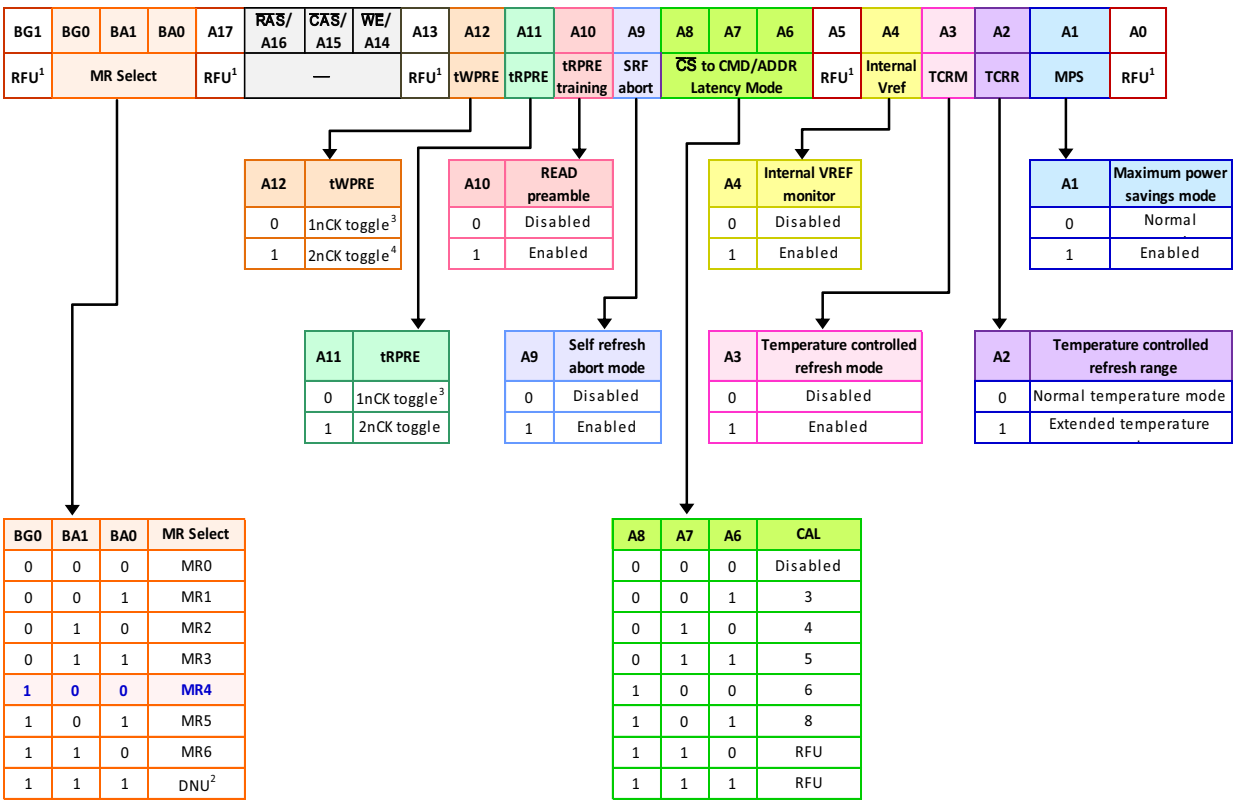
Per-DRAM Addressability

The MRS command mask allows programmability of a given device that may be in the same rank (devices sharing the same command and address signals). As an example, this feature can be used to program different ODT or VREF values on DRAM devices within a given rank.

Gear-down Mode

The DDR4 SDRAM defaults in half-rate (1N) clock mode and utilizes a low frequency MRS command followed by a sync pulse to align the proper clock edge for operating the control lines $\overline{CS}$, CKE, and ODT when in quarter-rate (2N) mode. For operation in half-rate mode, no MRS command or sync pulse is required.

Mode Register MR4



NOTE 1 Please refer to addressing table. If the address is available, it must be programmed to 0 during MRS
NOTE 2 Reserved for Register control word setting .DRAM ignores MR command with BG0,BA[1:0]=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.
NOTE 3 Not allowed when 1/4 rate Gear-down mode is enabled.
NOTE 4 When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range.

WRITE Preamble

DDR4 SDRAM introduces a programmable WRITE preamble tWPRE that can either be set to 1tCK or 2 tCK via the MR4 register. Note the 1tCK setting is similar to DDR3; however, the 2tCK setting is different. When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range. Check the table of CWL Selection for details.

READ Preamble

DDR4 SDRAM introduces a programmable READ preamble tRPRE that can be set to either 1tCK or 2tCK via the MR4 register. Note that both the 1tCK and 2tCK DDR4 preamble settings are different from what DDR3 SDRAM defined. Both of these READ preamble settings may require the memory controller to train (or READ-level) its data strobe receivers using the READ preamble training.

READ Preamble Training

DDR4 supports programmable READ preamble settings (1tCK or 2tCK). This mode can be used by the memory controller to train or READ level its data strobe receivers.

Temperature-Controlled Refresh (MR4[3] = 1 & MR2[6:7]=11)

When temperature-controlled refresh mode is enabled, the DDR4 SDRAM may adjust the internal refresh period to be longer than tREFI of the normal temperature range by skipping external refresh commands with the proper gear ratio. For example, the DRAM temperature sensor detected less than 45'C. Normal temperature mode covers the range of 0'C to 85'C, while the extended temperature range covers 0'C to 95'C.

Command Address Latency (CAL)

DDR4 supports the command address latency (CAL) function as a power savings feature. This feature can be enabled or disabled via the MRS setting. CAL is defined as the delay in clock cycles (tCAL) between a $\overline{CS}$ registered LOW and its corresponding registered command and address. The value of CAL (in clocks) must be programmed into the mode register and is based on the roundup (in clocks) of [tCAL(ns)/tCK(ns)].

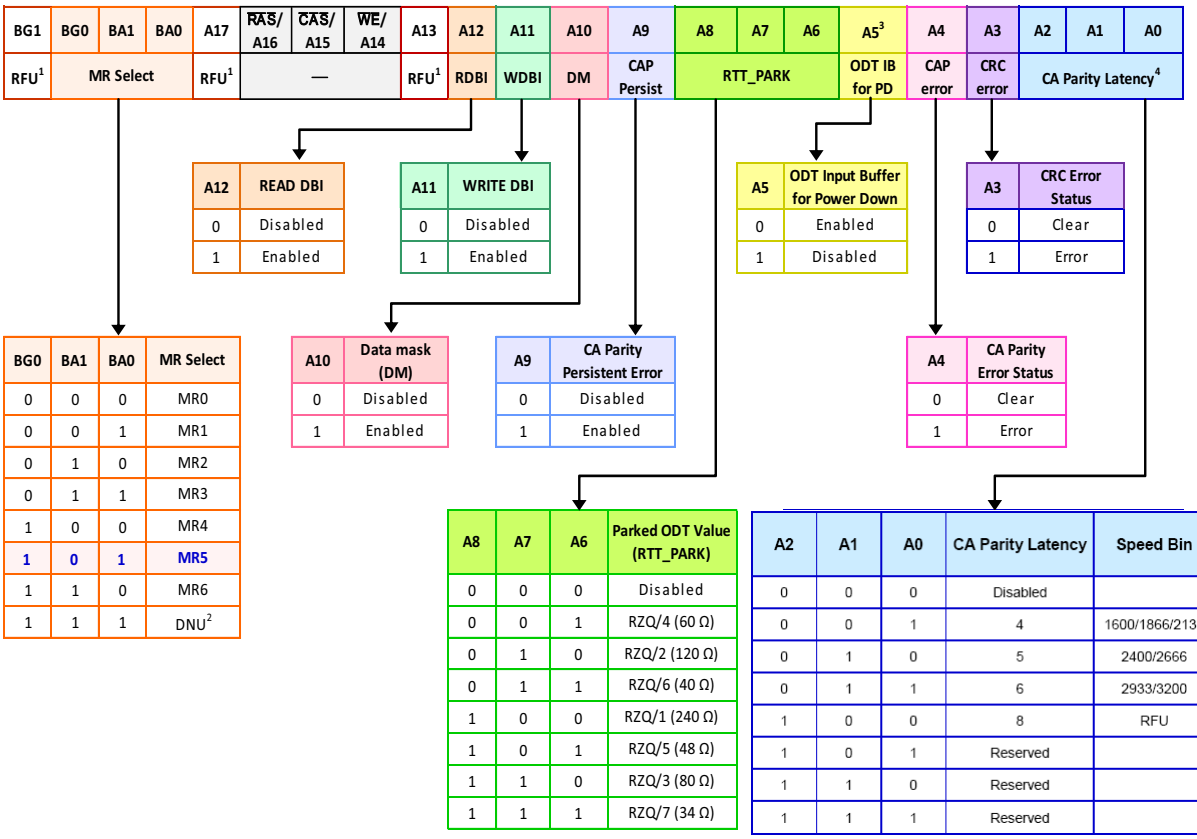
Internal VREF Monitor

DDR4 generates its own internal VREFDQ. This mode is allowed to be enabled during VREFDQ training and when enabled, VREF_time-short and VREF_time-long need to be increased by 10ns if DQ0, or DQ1, or DQ2, or DQ3 have 0pF loading; and add an additional 15ns per pF of added loading.

Maximum Power Savings Mode

This mode provides the lowest power mode where data retention is not required. When DDR4 SDRAM is in the maximum power saving mode, it does not need to guarantee data retention or respond to any external command (except maximum power saving mode exit command and during the assertion of $\overline{RESET}$ signal LOW).

Mode Register MR5



NOTE 1 Please refer to addressing table. If the address is available, it must be programmed to 0 during MRS
NOTE 2 Reserved for Register control word setting. DRAM ignores MR command with BG0,BA[1:0]=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.
NOTE 3 When RTT_NOM Disable is set in MR1, A5 of MR5 will be ignored.
NOTE 4 Parity latency must be programmed according to timing parameters by speed grade table.

Data Bus Inversion (DBI)

The data bus inversion (DBI) function has been added to DDR4 SDRAM and is supported for x8 and x16 configurations only (x4 is not supported). The DBI function shares a common pin with the DM and TDQS functions. The DBI function applies to both READ and WRITE operations and cannot be enabled at the same time the DM function is enabled. Refer to the TDQS Function Matrix table for valid configurations for all three functions (TDQS/DM/DBI).

Data Mask (DM)

The data mask (DM) function, also described as a partial write, has been added to DDR4 SDRAM and is supported for x8 and x16 configurations only (x4 is not supported). The DM function shares a common pin with the DBI and TDQS functions. The DM function applies only to WRITE operations and cannot be enabled at the same time the DBI function is enabled. Refer to the TDQS Function Matrix table for valid configurations for all three functions (TDQS/DM/DBI).

CA Parity Persistent Error Mode

Normal CA Parity Mode (CA Parity Persistent Mode disabled) no longer performs CA parity checking while the parity error status bit remains set at 1. However, with CA Parity Persistent Mode enabled, CA parity checking continues to be performed when the parity error status bit is set to a 1.

ODT Input Buffer for Power Down

Determines whether the ODT input buffer is on or off during Power Down. If the ODT input buffer is configured to be on (enabled during power down), the ODT input signal must be at a valid logic level. If the input buffer is configured to be off (disabled during power down), the ODT input signal may be floating and the DRAM does not provide RTT_NOM termination. The DRAM may, however, provide Rtt_Park termination depending on the MR settings. This is primarily for additional power savings.

CA Parity Error Status

DRAM will set the error status bit to 1 upon detecting a parity error. The parity error status bit remains set at 1 until the DRAM Controller clears it explicitly using an MRS command.

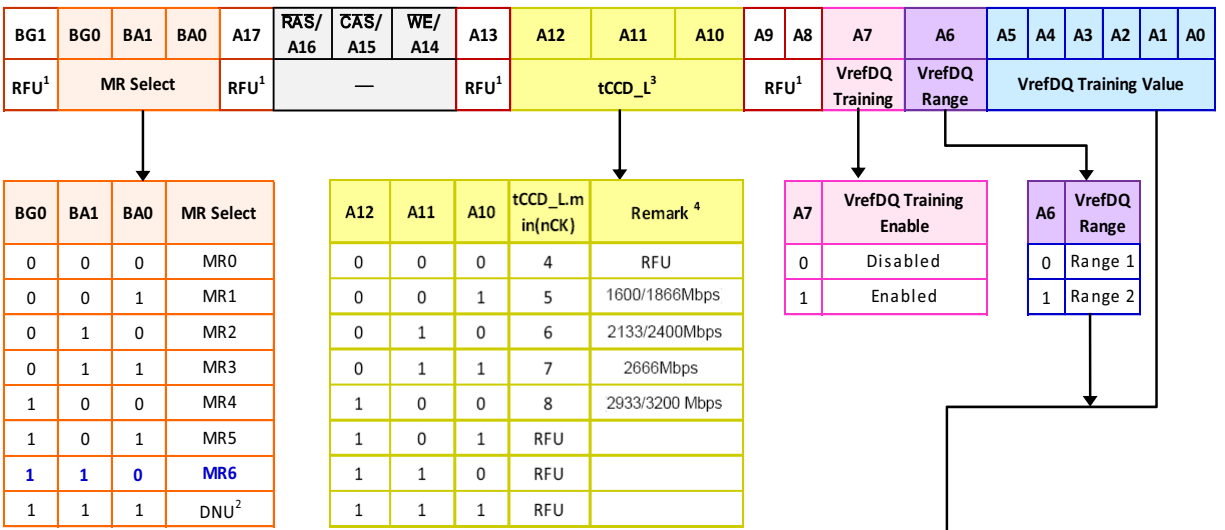
CRC Error Status

DRAM will set the error status bit to 1 upon detecting a CRC error. The CRC error status bit remains set at 1 until the DRAM controller clears it explicitly using an MRS command.

C/A Parity Latency Mode

CA Parity is enabled when a latency value, dependent on tCK, is programmed; this accounts for parity calculation delay internal to the DRAM. The normal state of CA Parity is to be disabled. If CA parity is enabled, the DRAM has to ensure that there are no parity errors before executing the command. CA Parity signal (PAR) covers $\overline{\text{ACT}}$, $\overline{\text{RAS}}$/A16 , $\overline{\text{CAS}}$/A15, $\overline{\text{WE}}$/A14, and the address bus including bank address and bank group bits. The control signals CKE, ODT and $\overline{\text{CS}}$ are not included in the parity calculation.

Mode Register MR6



BG0	BA1	BA0	MR Select
0	0	0	MR0
0	0	1	MR1
0	1	0	MR2
0	1	1	MR3
1	0	0	MR4
1	0	1	MR5
1	1	0	MR6
1	1	1	DNU[2]

A12	A11	A10	tCCD_L.min(nCK)	Remark [4]
0	0	0	4	RFU
0	0	1	5	1600/1866Mbps
0	1	0	6	2133/2400Mbps
0	1	1	7	2666Mbps
1	0	0	8	2933/3200 Mbps
1	0	1	RFU	
1	1	0	RFU	
1	1	1	RFU	

A7	VrefDQ Training Enable
0	Disabled
1	Enabled

A6	VrefDQ Range
0	Range 1
1	Range 2

MR6 [5:0]	Range 1 (MR6[6]=0)	Range 2 (MR6[6]=1)	MR6 [5:0]	Range 1 (MR6[6]=0)	Range 2 (MR6[6]=1)	MR6 [5:0]	Range 1 (MR6[6]=0)	Range 2 (MR6[6]=1)	MR6 [5:0]	Range 1 (MR6[6]=0)	Range 2 (MR6[6]=1)
00 0000	60.00%	45.00%	00 1101	68.45%	53.45%	01 1010	76.90%	61.90%	10 0111	85.35%	70.35%
00 0001	60.65%	45.65%	00 1110	69.10%	54.10%	01 1011	77.55%	62.55%	10 1000	86.00%	71.00%
00 0010	61.30%	46.30%	00 1111	69.75%	54.75%	01 1100	78.20%	63.20%	10 1001	86.65%	71.65%
00 0011	61.95%	46.95%	01 0000	70.40%	55.40%	01 1101	78.85%	63.85%	10 1010	87.30%	72.30%
00 0100	62.60%	47.60%	01 0001	71.05%	56.05%	01 1110	79.50%	64.50%	10 1011	87.95%	72.95%
00 0101	63.25%	48.25%	01 0010	71.70%	56.70%	01 1111	80.15%	65.15%	10 1100	88.60%	73.60%
00 0110	63.90%	48.90%	01 0011	72.35%	57.35%	10 0000	80.80%	65.80%	10 1101	89.25%	74.25%
00 0111	64.55%	49.55%	01 0100	73.00%	58.00%	10 0001	81.45%	66.45%	10 1110	89.90%	74.90%
00 1000	65.20%	50.20%	01 0101	73.65%	58.65%	10 0010	82.10%	67.10%	10 1111	90.55%	75.55%
00 1001	65.85%	50.85%	01 0110	74.30%	59.30%	10 0011	82.75%	67.75%	11 0000	91.20%	76.20%
00 1010	66.50%	51.50%	01 0111	74.95%	59.95%	10 0100	83.40%	68.40%	11 0001	91.85%	76.85%
00 1011	67.15%	52.15%	01 1000	75.60%	60.60%	10 0101	84.05%	69.05%	11 0010	92.50%	77.50%
00 1100	67.80%	52.80%	01 1001	76.25%	61.25%	10 0110	84.70%	69.70%	11 0011 to 111111	Reserved	Reserved

NOTE 1 Please refer to addressing table. If the address is available, it must be programmed to 0 during MRS
NOTE 2 Reserved for Register control word setting. DRAM ignores MR command with BG0,BA[1:0]=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.
NOTE 3 tCCD_L should be programmed according to the value defined in AC parameter table per operating frequency.
NOTE 4 It's not finalized. Might be changed.

tCCD_L Programming

The DRAM Controller must program the correct tCCD_L value. tCCD_L will be programmed according to the value defined in the AC parameter table per operating frequency.

VREFDQ Training Enable

VREFDQ Training is where the DRAM internally generates it's own VREFDQ used by the DQ input receivers. The DRAM controller must use a MRS protocol (adjust up, adjust down, etc.) for setting and calibrating the internal VREFDQ level. The procedure is a series of Writes and Reads in conduction with VREFDQ adjustments to optimize and verify the data eye. Enabling VREFDQ Training should be used whenever MR6[6:0] register values are being written to.

VREFDQ Training Range

DDR4 defines two VREFDQ training ranges - Range 1 and Range 2. Range 1 supports VREFDQ between 60% and 92% of VDDQ while Range 2 supports VREFDQ between 45% and 77% of VDDQ. Range 1 is targeted for module based designs and Range 2 is added targeting point-to point designs.

VREFDQ Training Value

Fifty settings provided 0.65% of granularity steps sizes for both Range 1 and Range 2 of VREFDQ.

DRAM MR7 Ignore

The DDR4 SDRAM shall ignore any access to MR7 for all DDR4 SDRAM.Any bit setting within MR7 may not take any effect in the DDR4 SDRAM.

DDR4 SDRAM Command Description and Operation

Command Truth Table

(a) Note 1,2,3 and 4 apply to the entire Command truth table

(b) Note 5 applies to all Read/Write commands

[BG=Bank Group Address, BA=Bank Address, RA=Row Address, CA=Column Address, $\overline{BC}$=Burst Chop, X=Don't Care, V=Valid].

Function	Abbre-viation	CKE		$\overline{CS}$	$\overline{ACT}$	$\overline{RAS}$/A14	$\overline{CAS}$/A15	$\overline{WE}$/A14	BG0-BG1	BA0-BA1	C2-C0	A12/$\overline{BC}$	A17, A13, A11	A10/AP	A0-A9	NOTE
		Previous Cycle	Current Cycle													
Mode Register Set	MRS	H	H	L	H	L	L	L	BG	BA	V	OP Code				12
Refresh	REF	H	H	L	H	L	L	H	V	V	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	H	L	L	H	V	V	V	V	V	V	V	7,9
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	7,8,9,10
				L	H	H	H	H	V	V	V	V	V	V	V	
Single Bank Pre-charge	PRE	H	H	L	H	L	H	L	BG	BA	V	V	V	L	V	
Precharge all Banks	PREA	H	H	L	H	L	H	L	V	V	V	V	V	H	V	
RFU	RFU	H	H	L	H	L	H	H	RFU							
Bank Activate	ACT	H	H	L	L	Row Address (RA)			BG	BA	V	Row Address (RA)				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	H	L	L	BG	BA	V	V	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	H	L	L	BG	BA	V	L	V	L	CA	
Write (BL8, on the Fly)t	WRS8	H	H	L	H	H	L	L	BG	BA	V	H	V	L	CA	
Write with Auto Pre-charge(Fixed BL8 or BC4)	WRA	H	H	L	H	H	L	L	BG	BA	V	V	V	H	CA	
Write with Auto Pre-charge(BC4, on the Fly)	WRAS4	H	H	L	H	H	L	L	BG	BA	V	L	V	H	CA	
Write with Auto Pre-charge(BL8, on the Fly)	WRAS8	H	H	L	H	H	L	L	BG	BA	V	H	V	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	H	L	H	BG	BA	V	V	V	L	CA	
Read (BC4, on the Fly)	RDS4	H	H	L	H	H	L	H	BG	BA	V	L	V	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	H	L	H	BG	BA	V	H	V	L	CA	
Read with Auto Pre-charge(Fixed BL8 or BC4)	RDA	H	H	L	H	H	L	H	BG	BA	V	V	V	H	CA	

Function	Abbre-viation	CKE		CS	ACT	RAS/ A14	CAS/ A15	WE/ A14	BG0-BG1	BA0-BA1	C2-C0	A12/ BC	A17, A13, A11	A10/ AP	A0-A9	NOTE
		Previous Cycle	Current Cycle													
Read with Auto Pre-charge(BC4, on the Fly)	RDAS4	H	H	L	H	H	L	H	BG	BA	V	L	V	H	CA	
Read with Auto Pre-charge(BL8, on the Fly)	RDAS8	H	H	L	H	H	L	H	BG	BA	V	H	V	H	CA	
No Operation	NOP	H	H	L	H	H	H	H	V	V	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	X	X	X	
Power Down Entry	PDE	H	L	H	X	X	X	X	X	X	X	X	X	X	X	6
Power Down Exit	PDX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	6
ZQ calibration Long	ZQCL	H	H	L	H	H	H	L	V	V	V	V	V	H	V	
ZQ calibration Short	ZQCS	H	H	L	H	H	H	L	V	V	V	V	V	L	V	

NOTE 1 All DDR4 SDRAM commands are defined by states of $\overline{CS}$, $\overline{ACT}$, $\overline{RAS}$/A16, $\overline{CAS}$/A15, $\overline{WE}$/A14 and CKE at the rising edge of the clock. The MSB of BG, BA, RA and CA are device density and conuration dependant. When $\overline{ACT}$ = H; pins $\overline{RAS}$/A16, $\overline{CAS}$/A15, and $\overline{WE}$/A14 are used as command pins $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ respectively. When $\overline{ACT}$= L; pins $\overline{RAS}$/A16, $\overline{CAS}$/A15, and $\overline{WE}$/A14 are used as address pins A16, A15, and A14 respectively.

NOTE 2 $\overline{RESET}$ is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.

NOTE 3 Bank Group addresses (BG) and Bank addresses (BA) determine which bank within a bank group to be operated upon. For MRS commands the BG and BA selects the specific Mode Register location.

NOTE 4 “V” means “H or L (but a defined logic level)” and “X” means either “defined or undefined (like floating) logic level”.

NOTE 5 Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-Fly BL will be defined by MRS.

NOTE 6 The Power Down Mode does not perform any refresh operation.

NOTE 7 The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.

NOTE 8 Controller guarantees self refresh exit to be synchronous.

NOTE 9 VPP and VREF(VREFCA) must be maintained during Self Refresh operation.

NOTE 10 The No Operation command should be used in cases when the DDR4 SDRAM is in Gear Down Mode and Max Power Saving Mode Exit.

NOTE 11 Refer to the CKE Truth Table for more detail with CKE transition.

NOTE 12 During a MRS command A17 is Reserved for Future Use and is device density and configuration dependent.

CKE Truth Table

Current State[2]	CKE		Command (N)[3]	Action (N)[3]	NOTE
	Previous Cycle[1](N-1)	Current Cycle[1](N)	RAS, CAS, WE, CS		
Power Down	L	L	X	Maintain Power-Down	14,15
	L	H	DESELECT	Power Down Exit	11,14
Self Refresh	L	L	X	Maintain Self Refresh	15,16
	L	H	DESELECT	Self Refresh Exit	8,12,16
Bank(s) Active	H	L	DESELECT	Active Power Down Entry	11, 13, 14
Reading	H	L	DESELECT	Power Down Entry	11, 13, 14, 17
Writing	H	L	DESELECT	Power Down Entry	11, 13, 14, 17
Precharging	H	L	DESELECT	Power Down Entry	11, 13, 14, 17
Refreshing	H	L	DESELECT	Precharge Power Down Entry	11
All Banks Idle	H	L	DESELECT	Precharge Power Down Entry	11,13, 14, 18
	H	L	DESELECT	Self Refresh Entry	9,13,18
For more details with all signals See “Command Truth Table”.					10

NOTE 1 CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.
NOTE 2 Current state is defined as the state of the DDR4 SDRAM immediately prior to clock edge N.

NOTE 3 COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N),ODT is not included here.

NOTE 4 All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.

NOTE 5 The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.

NOTE 6 During any CKE transition (registration of CKE H->L or CKE L->H), the CKE level must be maintained until 1nCK prior to tCKEmin being satisfied (at which time CKE may transition again).

NOTE 7 DESELECT and NOP are defined in the Command Truth Table.

NOTE 8 On Self-Refresh Exit DESELECT commands must be issued on every clock edge occurring during the tXS period. Read or ODT commands may be issued only after tXSDLL is satisfied.

NOTE 9 Self-Refresh mode can only be entered from the All Banks Idle state.

NOTE 10 Must be a legal command as defined in the Command Truth Table.

NOTE 11 Valid commands for Power-Down Entry and Exit are DESELECT only.

NOTE 12 Valid commands for Self-Refresh Exit are DESELECT only except for Gear Down mode and Max Power Saving exit. NOP is allowed for these 2 modes.

NOTE 13 Self-Refresh can not be entered during Read or Write operations. For a detailed list of restrictions, see “Self-Refresh Operation” and “Power-Down Modes”.

NOTE 14 The Power-Down does not perform any refresh operations.

NOTE 15 “X” means “don’t care” (including floating around VREF) in Self-Refresh and Power-Down. It also applies to Address pins.

NOTE 16 VPP and VREF(VREFCA) must be maintained during Self-Refresh operation.

NOTE 17 If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power-

Down is entered, otherwise Active Power-Down is entered.

NOTE 18 'Idle state' is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, etc.) as well as all Self-Refresh exit and Power-Down Exit parameters are satisfied (tXS, tXP,etc).

NOP Command

The NO OPERATION (NOP) command was originally used to instruct the selected DDR4 SDRAM to perform a NOP ($\overline{CS}$ = LOW and $\overline{AST}$, $\overline{RAS}$/A16, $\overline{CAS}$/A15, and $\overline{WE}$/A14 = HIGH). This prevented unwanted commands from being registered during idle or wait states. The NOP command general support has been removed and should not be used unless specifically allowed; which is when exiting Max Power Saving Mode or when entering Gear-down Mode.

DESELECT Command

The DESELECT function ($\overline{CS}$ HIGH) prevents new commands from being executed by the DDR4 SDRAM. The DDR4 SDRAM is effectively deselected. Operations already in progress are not affected.

DLL on/off switching procedure

DDR4 SDRAM DLL-off mode is entered by setting MR1 bit A0 to “0”; this will disable the DLL for subsequent operations until A0 bit is set back to “1”.

DLL on to DLL off Procedure

To switch from DLL on to DLL off requires the frequency to be changed during Self-Refresh, as outlined in the following procedure:

1. Starting from Idle state (All banks pre-charged, all timings fulfilled, and DRAMs On-die Terminationresistors, RTT_NOM, must be in high impedance state before MRS to MR1 to disable the DLL.)

2. Set MR1 bit A0 to “0” to disable the DLL.

3. Wait tMOD.

4. Enter Self Refresh Mode; wait until (tCKSRE) is satisfied.

5. Change frequency, in guidance with “Input clock frequency change”.

6. Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs.

7. Starting with the Self Refresh Exit command, CKE must continuously be registered HIGH until alltMOD timings from any MRS command are satisfied. In addition, if any ODT features were enabled inthe mode registers when Self Refresh mode was entered, the ODT signal must continuously be registered LOW until all tMOD timings from any MRS command are satisfied. If RTT_NOM features were disabled in the mode registers when Self Refresh mode was entered, ODT signal is Don’t Care.

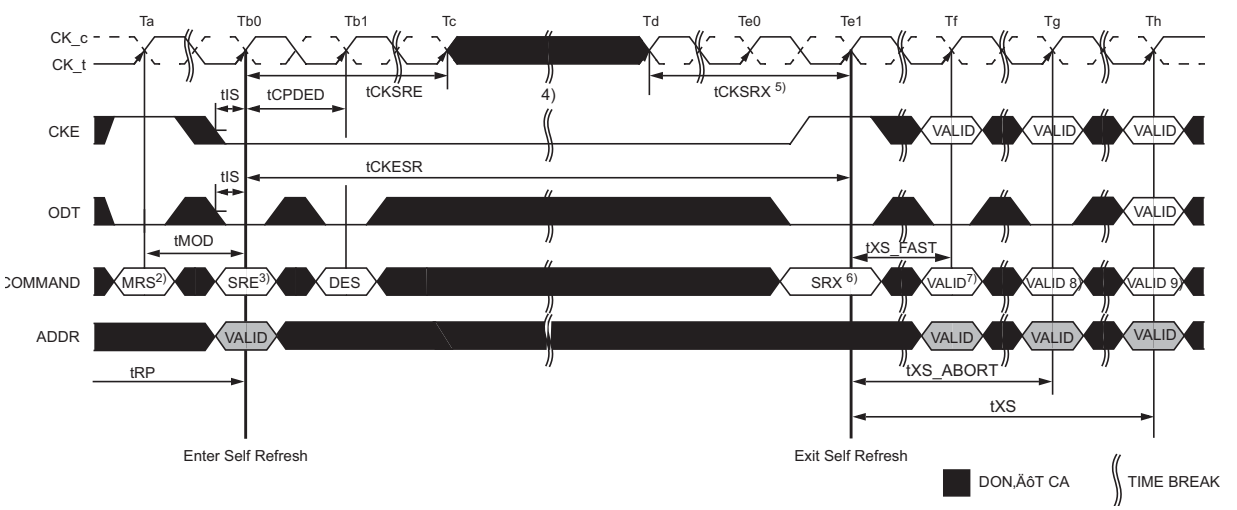
8. Wait tXS_Fast or tXS_Abort or tXS, then set Mode Registers with appropriate values (especially an update of CL, CWL and WR may be necessary. A ZQCL command may also be issued after tXS_Fast).

- tXS - ACT, PRE, PREA, REF, SRE, PDE, WR, WRS4, WRS8, WRA, WRAS4, WRAS8, RD, RDS4, RDS8, RDA, RDAS4, RDAS8

- tXS_Fast - ZQCL, ZQCS, MRS commands. For MRS command, only DRAM CL and WR/RTP register in MR0, CWL register in MR2 and geardown mode in MR3 are allowed to be accessed provided DRAM is not in per DRAM addressibility mode. Access to other DRAM mode registers must satisfy tXS timing.

- tXS_Abort - If the MR4 bit A9 is enabled then the DRAM aborts any ongoing refresh and does not increment the refresh counter. The controller can issue a valid command after a delay of tXS_abort. Upon exit from Self-Refresh, the DDR4 SDRAM requires a minimum of one extra refresh command before it is put back into Self-Refresh Mode. This requirement remains the same irrespective of the setting of the MRS bit for self refresh abort.

9. Wait for tMOD, then DRAM is ready for next command.



NOTE 1 Starting in the idle state. RTT in stable state.

NOTE 2 Disable DLL by setting MR1 bit A0 to 0.

NOTE 3 Enter SR.

NOTE 4 Change frequency.

NOTE 5 Clock must be stable tCKSRX.

NOTE 6 Exit SR.

NOTE 7,8,9 Update mode registers allowed with DLL_off settings met.

DLL off to DLL on Procedure

To switch from DLL off to DLL on (with required frequency change) during Self-Refresh:

1. Starting from Idle state (All banks pre-charged, all timings fulfilled and DRAMs On-die Termination resistors (RTT_NOM) must be in high impedance state before Self-Refresh mode is entered.)

2. Enter Self Refresh Mode, wait until tCKSRE satisfied.

3. Change frequency, in guidance with "Input clock frequency change".

4. Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs.

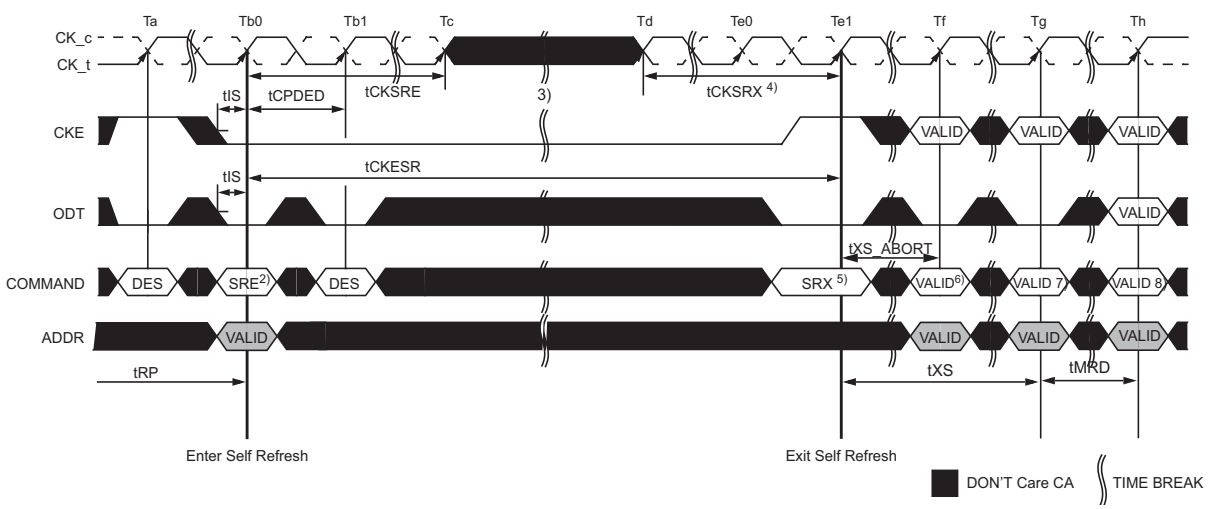
5. Starting with the Self Refresh Exit command, CKE must continuously be registered HIGH until tDLLK timing from subsequent DLL Reset command is satisfied. In addition, if any ODT features were enabled in the mode registers when Self Refresh mode was entered, the ODT signal must continuously be registered LOW until tDLLK timings from subsequent DLL Reset command is satisfied. If RTT_NOM were disabled in the mode registers when Self Refresh mode was entered, ODT signal is Don't care.

6. Wait tXS or tXS_ABORT depending on Bit A9 in MR4, then set MR1 bit A0 to "1" to enable the DLL.

7. Wait tMRD, then set MR0 bit A8 to "1" to start DLL Reset.

8. Wait tMRD, then set Mode Registers with appropriate values (especially an update of CL, CWL and WR may be necessary. After tMOD satisfied from any proceeding MRS command, a ZQCL command may also be issued during or after tDLLK.)

9. Wait for tMOD, then DRAM is ready for next command (Remember to wait tDLLK after DLL Reset before applying command requiring a locked DLL!). In addition, wait also for tZQoper in case a ZQCL command was issued.



NOTE 1 Starting in the idle state.

NOTE 2 Enter SR.

NOTE 3 Change frequency.

NOTE 4 Clock must be stable tCKSRX.

NOTE 5 Exit SR.

NOTE 6,7 Set DLL to on by setting MR1 ro A0 = 1.

NOTE 8 Start DLLReset.

NOTE 9 Update rest MR register values after tDLLK (not shown in the diagram).

NOTE 10 Ready for valid command after tDLLK (not shown in the diagram).

DLL-off Mode

DDR4 SDRAM DLL-off mode is entered by setting MR1 bit A0 to “0”; this will disable the DLL for subsequent operations until A0 bit is set back to “1”. The MR1 A0 bit for DLL control can be switched either during initialization or later. Refer to “Input clock frequency change”.

The DLL-off Mode operations listed below are an optional feature for DDR4 SDRAM. The maximum clock frequency for DLL-off Mode is specified by the parameter tCKDLL_OFF. There is no minimum frequency limit besides the need to satisfy the refresh interval, tREFI.

Due to latency counter and timing restrictions, only one value of CAS Latency (CL) in MR0 and CAS Write Latency (CWL) in MR2 are supported. The DLL-off mode is only required to support setting of both CL=10 and CWL=9. When DLL-off Mode is enabled, use of CA Parity Mode is not allowed.

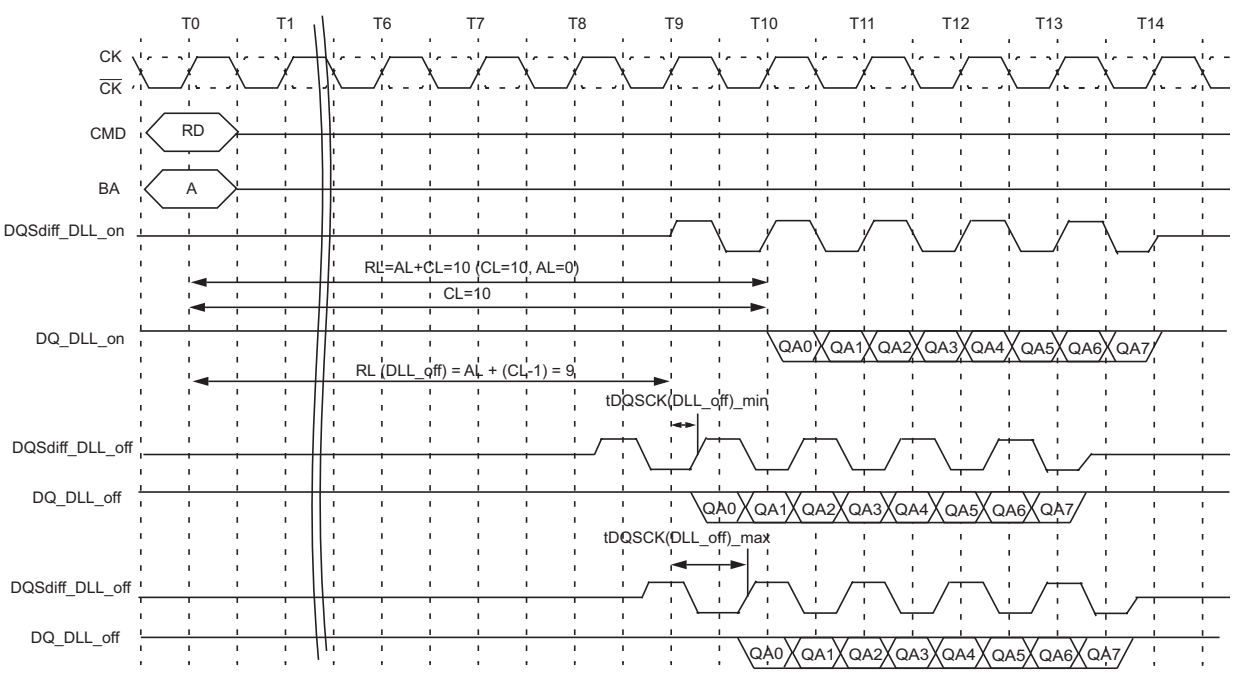
DLL-off mode will affect the Read data Clock to Data Strobe relationship (tDQSCK), but not the Data Strobe to Data relationship (tDQSQ, tQH). Special attention is needed to line up Read data to controller time domain.

Comparing with DLL-on mode, where tDQSCK starts from the rising clock edge (AL+CL) cycles after the Read command, the DLL-off mode tDQSCK starts (AL+CL - 1) cycles after the read command.

Another difference is that tDQSCK may not be small compared to tCK (it might even be larger than tCK) and the difference between tDQSCKmin and tDQSCKmax is significantly larger than in DLL-on mode.

tDQSCK(DLL_off) values are vendor specific.

The timing relations on DLL-off mode READ operation are shown in the following Timing Diagram(CL=10, BL=8, PL=0):



Input Clock Frequency Change

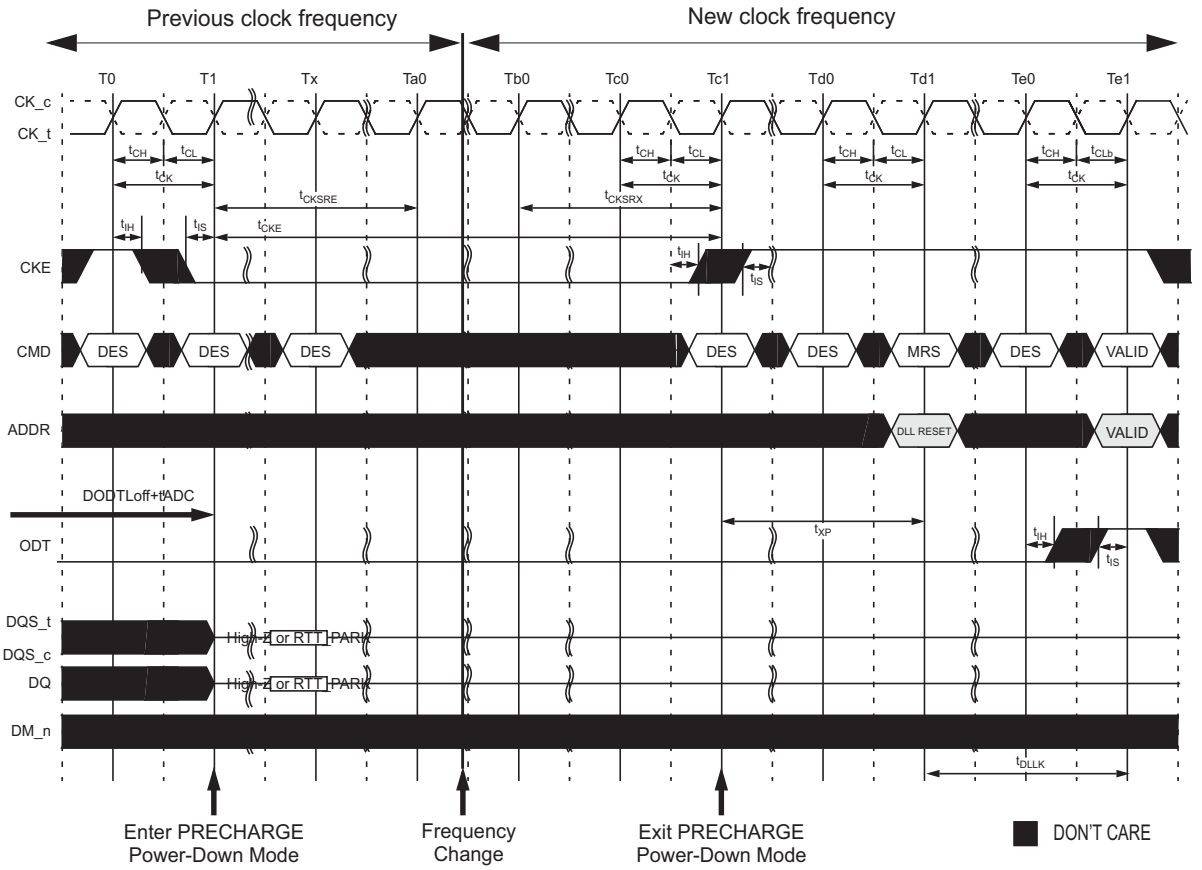
Once the DDR4 SDRAM is initialized, the DDR4 SDRAM requires the clock to be “stable” during almost all states of normal operation. This means that, once the clock frequency has been set and is to be in the °ßstable state°®, the clock period is not allowed to deviate except for what is allowed for by the clock jitter and SSC (spread spectrum clocking) specifications.

The input clock frequency can be changed from one stable clock rate to another stable clock rate under two conditions: (1) Self-Refresh mode and (2) Precharge Power-down mode. Outside of these two modes, it is illegal to change the clock frequency.For the first condition, once the DDR4 SDRAM has been successfully placed in to Self-Refresh mode and tCKSRE has been satisfied, the state of the clock becomes a don’t care. Once a don’t care, changing the clock frequency is permissible, provided the new clock frequency is stable prior to tCKSRX. When entering and exiting Self-Refresh mode for the sole purpose of changing the clock frequency, the Self-Refresh entry and exit specifications must still be met as outlined in “Self-Refresh Operation”.However, because DDR4 DLL lock time ranges from 597nCK at 1333MT/s to 1024nCK at 3200MT/s, additional MRS commands need to be issued for the new clock frequency. If DLL is enabled, tDLLK must be programmed according to the value defined in AC parameter tables, and the DLL must be RESET by an explicit MRS command (MR0 bit A8=’1’b) when the input clock frequency is different before and after self refresh.The DDR4 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade. Any frequency change below the minimum operating frequency would require the use of DLL_on- mode -> DLL_off -mode transition sequence, refer to “DLL on/off switching procedure”.

The second condition is when the DDR4 SDRAM is in Precharge Power-down mode. If the RTT_NOM feature was enabled in the mode register prior to entering Precharge power down mode, the ODT signal must continuously be registered LOW during this sequence until DLL re-lock to complete.

If the RTT_NOM feature was disabled in the mode register prior to entering Precharge power down mode, ODT signal is allowed to be floating and DRAM does not provide RTT_NOM termination. A minimum of tCKSRE must occur after CKE goes LOW before the clock frequency may change.

The DDR4 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade. During the input clock frequency change, CKE must be held at stable LOW levels. Once the input clock frequency is changed, stable new clocks must be provided to the DRAM tCKSRX before Precharge Power-down may be exited; after Precharge Power-down is exited and tXP has expired, tDLLK MRS command followed by DLL reset must be issued. Depending on the new clock frequency, additional MRS commands may need to be issued to appropriately set the WR/RTP, CL, and CWL with CKE continuously registered high. During DLL re-lock period, CKE must remain HIGH. After the DLL lock time, the DRAM is ready to operate with new clock frequency.



NOTE 1 tCKSRE and tCKSRX are Self-Refresh mode specifications but the value they represent are applicable here.

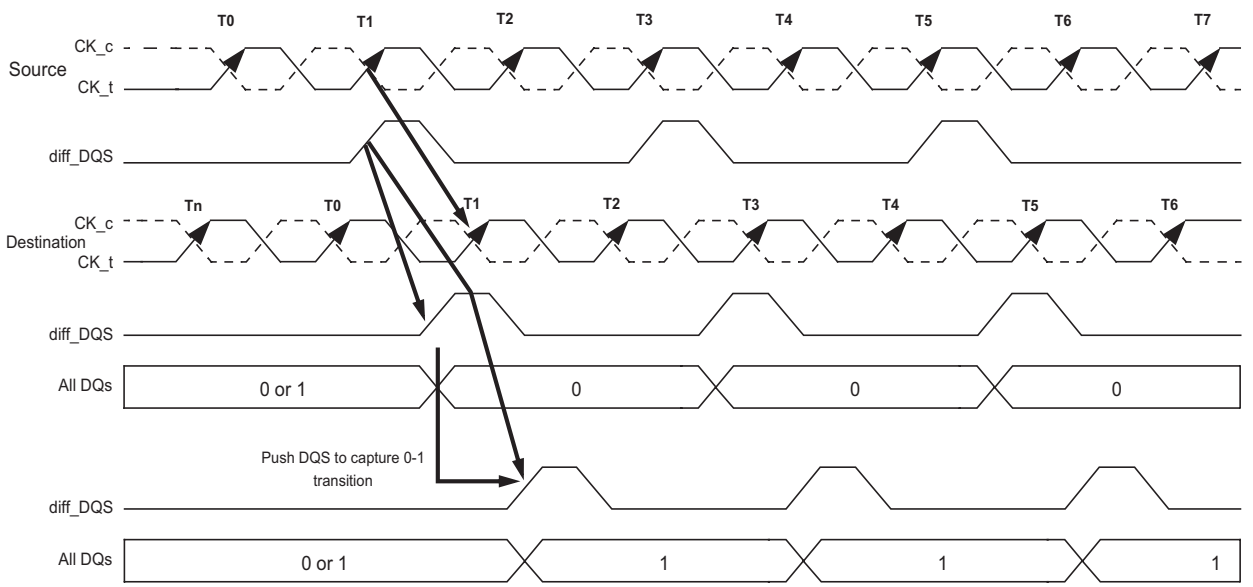
NOTE 2 If the RTT_NOM feature was enabled in the mode register prior to entering Precharge power down mode, the ODT signal must continuously be registered LOW ensuring RTT is in an off state. If the RTT_NOM feature was disabled in the mode register prior to entering Precharge power down mode or DRAM ODT input deactivation is enabled, RTT will remain in the off state. The ODT signal can be registered either LOW or HIGH in this case.

NOTE 3 If RTT_PARK is disabled and ODT input buffer is not deactivated.

Write Leveling

For better signal integrity, the DDR4 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has benefits from reducing number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the DDR4 SDRAM supports a 'write leveling' feature to allow the controller to compensate for skew. This feature may not be required under some system conditions provided the host can maintain the tDQSS, tDSS and tDSH specifications.

The memory controller can use the 'write leveling' feature and feedback from the DDR4 SDRAM to adjust the DQS - $\overline{\text{DQS}}$ to CK - $\overline{\text{CK}}$ relationship. The memory controller involved in the leveling must have adjustable delay setting on DQS - $\overline{\text{DQS}}$ to align the rising edge of DQS - $\overline{\text{DQS}}$ with that of the clock at the DRAM pin. The DRAM asynchronously feeds back CK - $\overline{\text{CK}}$, sampled with the rising edge of DQS - $\overline{\text{DQS}}$, through the DQ bus. The controller repeatedly delays DQS - $\overline{\text{DQS}}$ until a transition from 0 to 1 is detected. The DQS - $\overline{\text{DQS}}$ delay established through this exercise would ensure tDQSS specification. Besides tDQSS, tDSS and tDSH specification also needs to be fulfilled. One way to achieve this is to combine the actual tDQSS in the application with an appropriate duty cycle and jitter on the DQS - $\overline{\text{DQS}}$ signals. Depending on the actual tDQSS in the application, the actual values for tDQSL and tDQSH may have to be better than the absolute limits provided in the chapter "AC Timing Parameters" in order to satisfy tDSS and tDSH specification. A conceptual timing of this scheme is shown below.



DQS - $\overline{\text{DQS}}$ driven by the controller during leveling mode must be terminated by the DRAM based on ranks populated. Similarly, the DQ bus driven by the DRAM must also be terminated at the controller.

All data bits should carry the leveling feedback to the controller across the DRAM configurations X4, X8, and X16. On a X16 device, both byte lanes should be leveled independently. Therefore, a separate feedback mechanism should be available for each byte lane. The upper data bits should provide the feedback of the upper diff_DQS(diff_UDQS) to clock relationship whereas the lower data bits would indicate the lower diff_DQS(diff_LDQS) to clock relationship.

RAM setting for write leveling & DRAM termination function in that mode

DRAM enters into Write leveling mode if A7 in MR1 set 'High' and after finishing leveling, DRAM exits from write leveling mode if A7 in MR1 set 'Low'. Note that in write leveling mode, only DQS/$\overline{\text{DQS}}$ terminations are activated and deactivated via ODT pin, unlike normal operation.

MR setting involved in the leveling procedure

Function	MR1	Enable	Disable
Write leveling enable	A7	1	0
Output buffer mode (Qoff)	A12	0	1

MR setting involved in the leveling procedure

ODT pin @DRAM if RTT_NOM/PARK Value is set via MRS	DQS/$\overline{DQS}$ termination	DQs termination
RTT_NOM with ODT High	On	Off
RTT_PARK with ODT LOW	On	Off

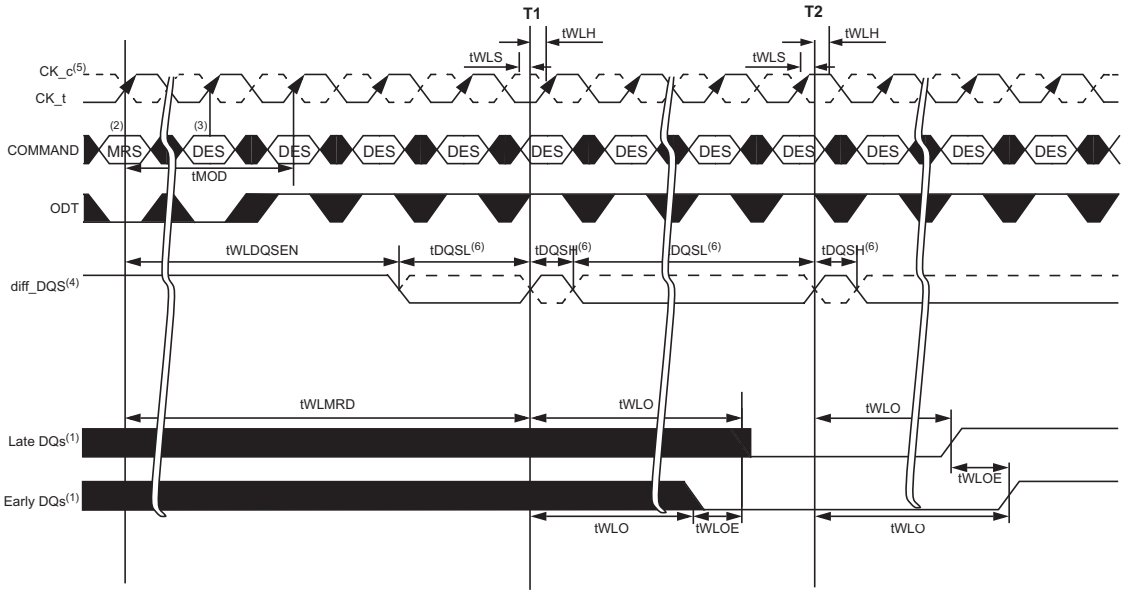
NOTE 1 In Write Leveling Mode with its output buffer disabled (MR1[bit A7] = 1 with MR1[bit A12] = 1) all RTT_NOM and RTT_PARK settings are allowed; in Write Leveling Mode with its output buffer enabled (MR1[bit A7] = 1 with MR1[bit A12] = 0) only RTT_NOM and RTT_PARK settings of TBD are allowed.

Procedure Description

The Memory controller initiates Leveling mode of all DRAMs by setting bit A7 of MR1 to 1. When entering write leveling mode, the DQ pins are in undefined driving mode. During write leveling mode, only DESELECT commands are allowed, as well as an MRS command to change Qoff bit (MR1[A12]) and an MRS command to exit write leveling (MR1[A7]). Upon exiting write leveling mode, the MRS command performing the exit (MR1[A7]=0) may also change MR1 bits of A12-A8 ,A2-A1. Since the controller levels one rank at a time, the output of other ranks must be disabled by setting MR1 bit A12 to 1. The Controller may assert ODT after tMOD, at which time the DRAM is ready to accept the ODT signal.

The Controller may drive DQS low and $\overline{DQS}$ high after a delay of tWLDQSEN, at which time the DRAM has applied on-die termination on these signals. After tDQSL and tWLMRD, the controller provides a single DQS, $\overline{DQS}$ edge which is used by the DRAM to sample CK - $\overline{CK}$ driven from controller. tWLMRD(max) timing is controller dependent.

DRAM samples CK - $\overline{CK}$ status with rising edge of DQS - $\overline{DQS}$ and provides feedback on all the DQ bits asynchronously after tWLO timing. There is a DQ output uncertainty of tWLOE defined to allow mismatch on DQ bits. The tWLOE period is defined from the transition of the earliest DQ bit to the corresponding transition of the latest DQ bit. There are no read strobes (DQS/$\overline{DQS}$) needed for these DQs. Controller samples incoming DQs and decides to increment or decrement DQS - $\overline{DQS}$ delay setting and launches the next DQS/$\overline{DQS}$ pulse after some time, which is controller dependent. Once a 0 to 1 transition is detected, the controller locks DQS - $\overline{DQS}$ delay setting and write leveling is achieved for the device. The following figure describes the timing diagram and parameters for the overall Write Leveling procedure.



NOTE 1 DDR4 SDRAM drives leveling feedback on all DQs

NOTE 2 MRS : Load MR1 to enter write leveling mode

NOTE 3 DES : Deselect

NOTE 4 diff_DQS is the differential data strobe (DQS-$\overline{DQS}$). Timing reference points are the zero crossings. DQS is shown with solid line, $\overline{DQS}$ is shown with dotted line

NOTE 5 CK/$\overline{CK}$: CK is shown with solid dark line, where as $\overline{CK}$ is drawn with dotted line.

NOTE 6 DQS, $\overline{DQS}$ needs to fulfill minimum pulse width requirements tDQSH(min) and tDQSL(min) as defined for regular Writes; the max pulse width is system dependent

Write Leveling Mode Exit

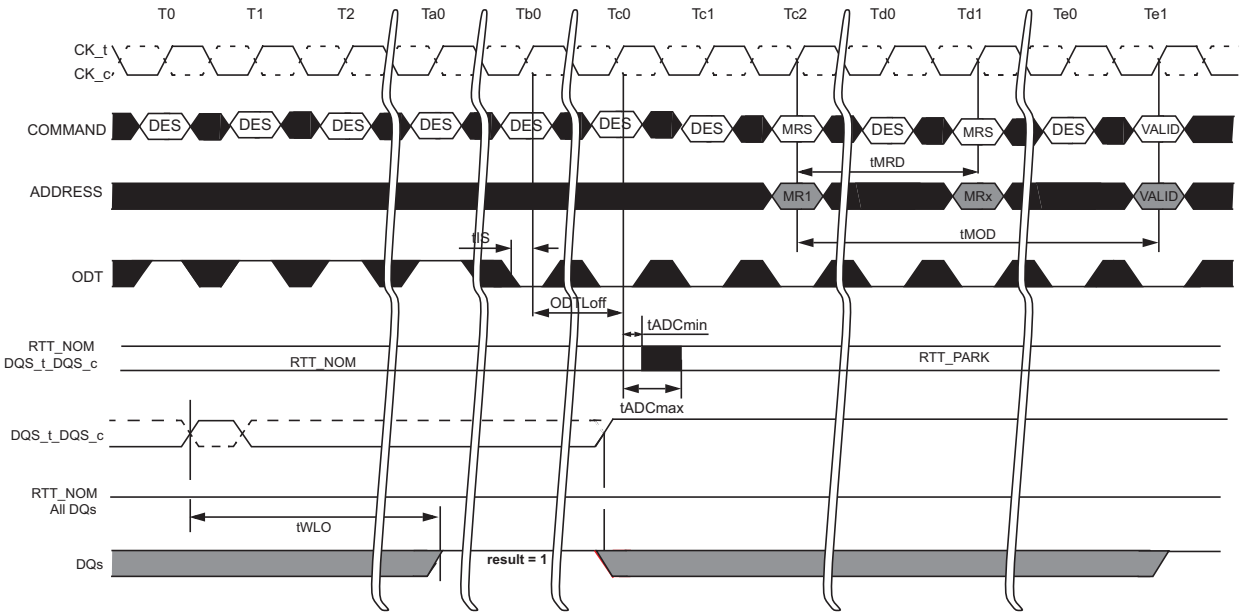
The following sequence describes how the Write Leveling Mode should be exited:

1.After the last rising strobe edge (see ~T0), stop driving the strobe signals (see ~Tc0). Note: From now on, DQ pins are in undefined driving mode, and will remain undefined, until tMOD after the respective MRS command (Te1).

2.Drive ODT pin low (tIS must be satisfied) and continue registering low. (see Tb0).

3.After the RTT is switched off, disable Write Level Mode via MRS command (see Tc2).

4.After tMOD is satisfied (Te1), any valid command may be registered. (MRS commands may be issued after tMRD (Td1)).

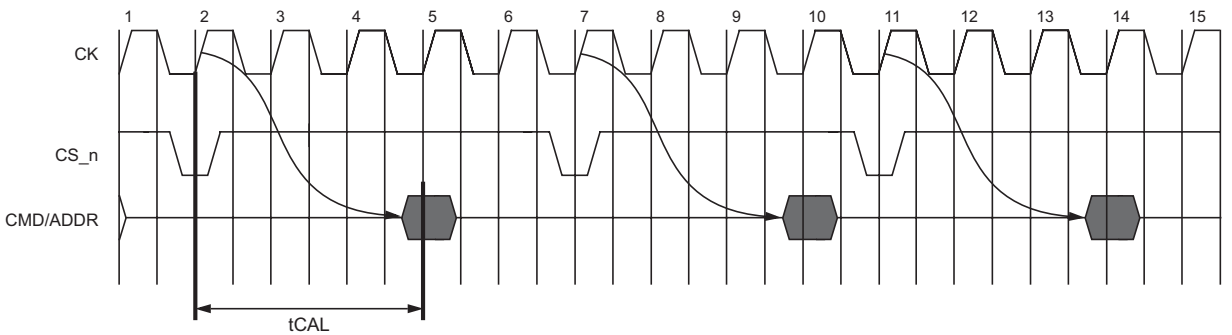

T0
T1
T2
Ta0
Tb0
Tc0
Tc1
Tc2
Td0
Td1
Te0
Te1
CK_t
CK_c
COMMAND
DES
MRS
VALID
tMRD
ADDRESS
MR1
MRx
VALID
tMOD
tIS
ODT
ODTLoff
tADCmin
RTT_NOM
DQS_t_DQS_c
RTT_NOM
RTT_PARK
tADCmax
DQS_t_DQS_c
RTT_NOM
All DQs
tWLO
DQs
result = 1

CAL Mode ($\overline{CS}$ to Command Address Latency)

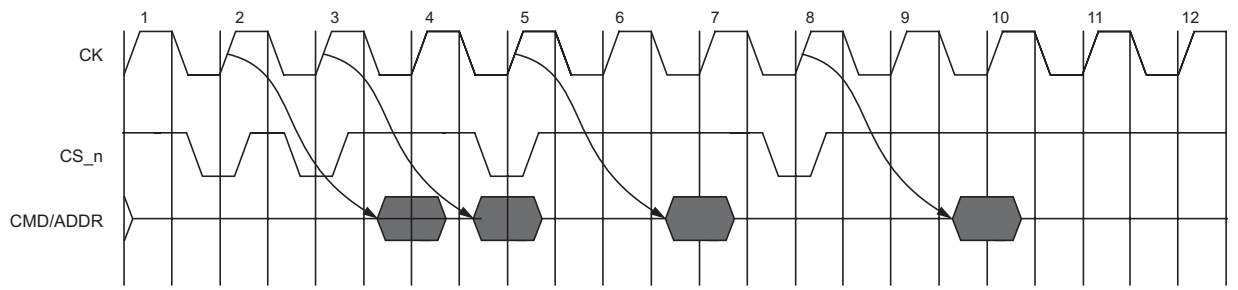
DDR4 supports Command Address Latency, CAL, function as a power savings feature. CAL is the delay in clock cycles between $\overline{CS}$ and CMD/ADDR defined by MR4[A8:A6] .

CAL gives the DRAM time to enable the CMD/ADDR receivers before a command is issued. Once the command and the address are latched, the receivers can be disabled. For consecutive commands, the DRAM will keep the receivers enabled for the duration of the command sequence.

Definition of CAL



CAL operational timing for consecutive command issues



The following tables show the timing requirements for tCAL and MRS settings at different data rates.

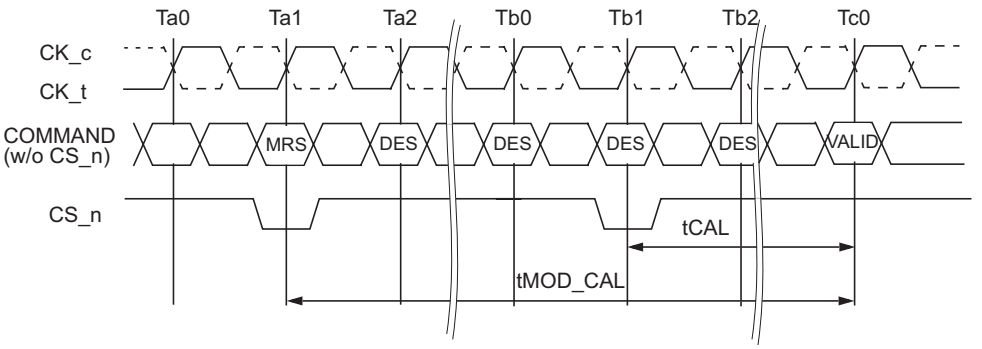
Parameter	Symbol	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	Units
$\overline{CS}$ to Command Address Latency	tCAL	max(3 nCK, 3.748 ns)	max(3 nCK, 3.748 ns)	max(3 nCK, 3.748 ns)	max(3 nCK, 3.748 ns)	nCK

Parameter	Symbol	DDR4-2666				Units
$\overline{CS}$ to Command Address Latency (Gear down mode even CK)	tCAL	max(3 nCK, 3.748 ns)				nCK

MRS Timings with Command/Address Latency enabled

When Command/Address latency mode is enabled, users must allow more time for MRS commands to take effect. When CAL modeis enabled, or being enabled by an MRS command, the earliest the next valid command can be issued is tMOD_CAL, wheretMOD_CAL=tMOD+tCAL.

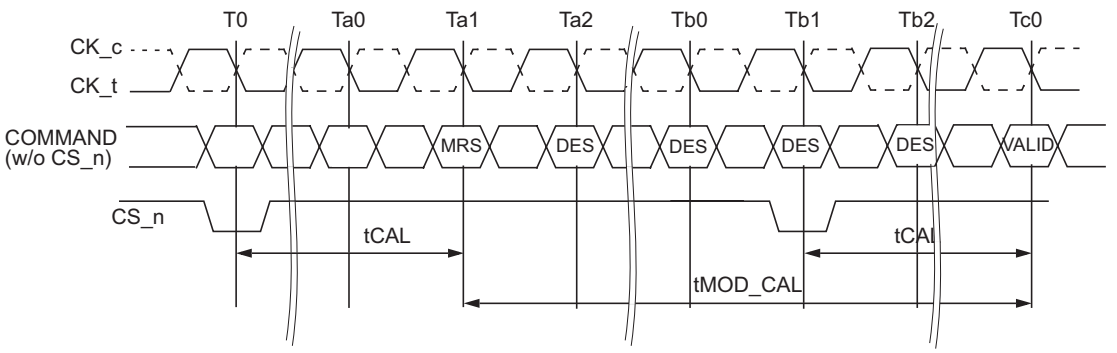
CAL enable timing - tMOD_CAL



NOTE 1 MRS command at Ta1 enables CAL mode

NOTE 2 tMOD_CAL=tMOD+tCAL

tMOD_CAL, MRS to valid command timing with CAL enabled

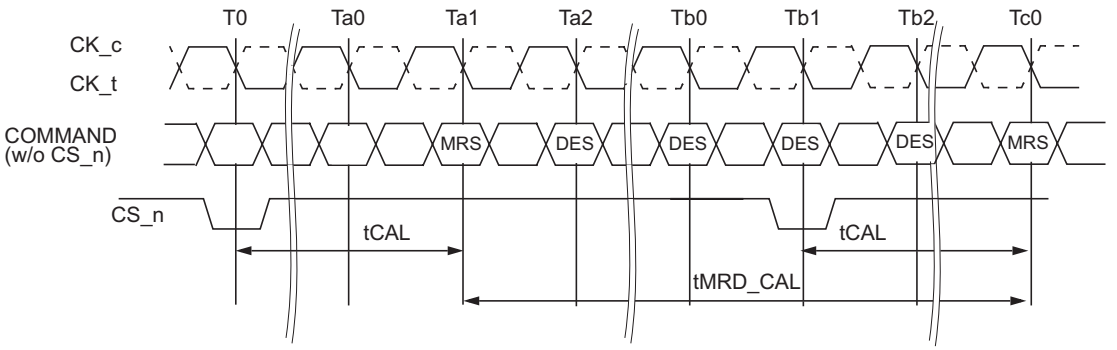


NOTE 1 MRS at Ta1 may or may not modify CAL, tMOD_CAL is computed based on new tCAL setting.

NOTE 2 tMOD_CAL=tMOD+tCAL.

When Command/Address latency is enabled or being entered, users must wait tMRD_CAL until the next MRS command can be issued. tMRD_CAL=tMOD+tCAL.

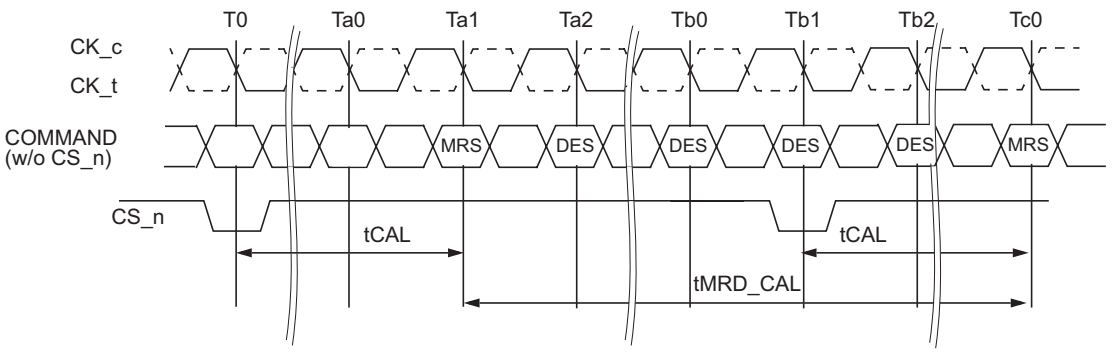
CAL enabling MRS to next MRS command, tMRD_CAL



NOTE 1 MRS command at Ta1 enables CAL mode.

NOTE 2 tMOD_CAL=tMOD+tCAL.

tMRD_CAL, mode register cycle time with CAL enabled



NOTE 1 MRS at Ta1 may or may not modify CAL, tMRD_CAL is computed based on new tCAL setting.

NOTE 2 tMOD_CAL=tMOD+tCAL.

Multi Purpose Register

DQ Training with MPR

The DDR4 DRAM contains four 8bit programmable MPR registers used for DQ bit pattern storage. These registers once programmed are activated with MRS read commands to drive the MPR bits on to the DQ bus during link training.

And DDR4 SDRAM only supports following command, MRS, RD, RDA WR, WRA, DES, REF and Reset during MPR enable Mode: MR3 [A2 = 1].

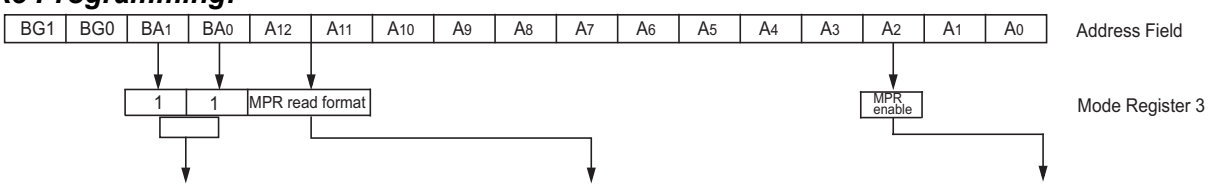
Note that in MPR mode RDA/WRA has the same functionality as a READ/WRITE command which means the auto pre-charge part of RDA/WRA is ignored. Power-Down mode and Self-Refresh command also is not allowed during MPR enable Mode. No other command can be issued within tRFC after REF command and 1x Refresh is only allowed when MPR mode is Enable. During MPR operations, MPR read or write sequence must be complete prior to a refresh command.

MR3 definition

Mode register MR3 controls the Multi-Purpose Registers (MPR) used for training. MR3 is written by asserting $\overline{CS}$, $\overline{RAS}$/A16,$\overline{CAS}$/A15 and $\overline{WE}$/A14 low, $\overline{ACT}$, BA0 and BA1 high and BG1[1] and BG0 low while controlling the states of the address pinsaccording to the table below.

NOTE 1. x4/x8 only

MR3 Programming:



BA1	BA0	MR select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

A12	A11	MPR read format
0	0	Serial
0	1	Parallel
1	0	Staggered
1	1	RFU

A2	MPR Operation
0	Normal operation
1	Dataflow from/to MPR

Read or Write with MPR LOCATION :

BA1	BA0	MPR Location
0	0	MPR location 0
0	1	MPR location 1
1	0	MPR location 2
1	1	MPR location 3

Default value for MPR0 = 01010101
Default value for MPR1 = 00110011
Default value for MPR2 = 00001111
Default value for MPR3 = 00000000

MPR Reads

MPR reads are supported using BL8 and BC4(Fixed) modes. BC4 on the fly is not supported for MPR reads.

MPR reads using BC4:

BA1 and BA0 indicate the MPR location within the selected page in MPR Mode.

A10 and other address pins are don't care including BG1 and BG0.Read commands for BC4 are supported with starting column address of A2:A0 of '000' and '100'.

Data Bus Inversion (DBI) is not allowed during MPR Read operation.

DDR4 MPR mode is enabled by programming bit A2=1 and then reads are done from a specific MPR location.

MPR location is specified with the Read command using Bank address bits BA1 and BA0.

Each MPR location is 8 bit wide.

STEPS:

DLL must be locked prior to MPR Reads. If DLL is Enabled : MR1[A0 = 1]

Precharge all

Wait until tRP is satisfied

MRS MR3, Opcode A2=’1’b

- Redirect all subsequent read and writes to MPR locations

Wait until tMRD and tMOD satisfied.

Read command

- A[1:0] = ‘00’b (data burst order is fixed starting at nibble, always 00b here)
- A[2]= ‘0’b (For BL=8, burst order is fixed at 0,1,2,3,4,5,6,7)
  (For BC=4, burst order is fixed at 0,1,2,3,T,T,T,T)

or

- A[2]= 1 (For BL=8 : Not Support)
  (For BC=4, burst order is fixed at 4,5,6,7,T,T,T,T)
- A12/BC= 0 or 1 : Burst length supports only BL8(Fixed) and BC4(Fixed), not supports BC4(OTF).

When MR0 A[1:0] is set ‘01’, A12/BC must be always ‘1’b in MPR read commands (BL8 only).

- BA1 and BA0 indicate the MPR location
- A10 and other address pins are don’t care including BG1and BG0

After RL= AL + CL, DRAM bursts out the data from MPR location. The format of data on return is described in a later section andcontrolled by MR3 bits A0,A1, A11 and A12.

Memory controller repeats these calibration reads until read data capture at memory controller is optimized. Read MPR location canbe a different location as specified by the Read command

After end of last MPR read burst, wait until tMPRR is satisfied

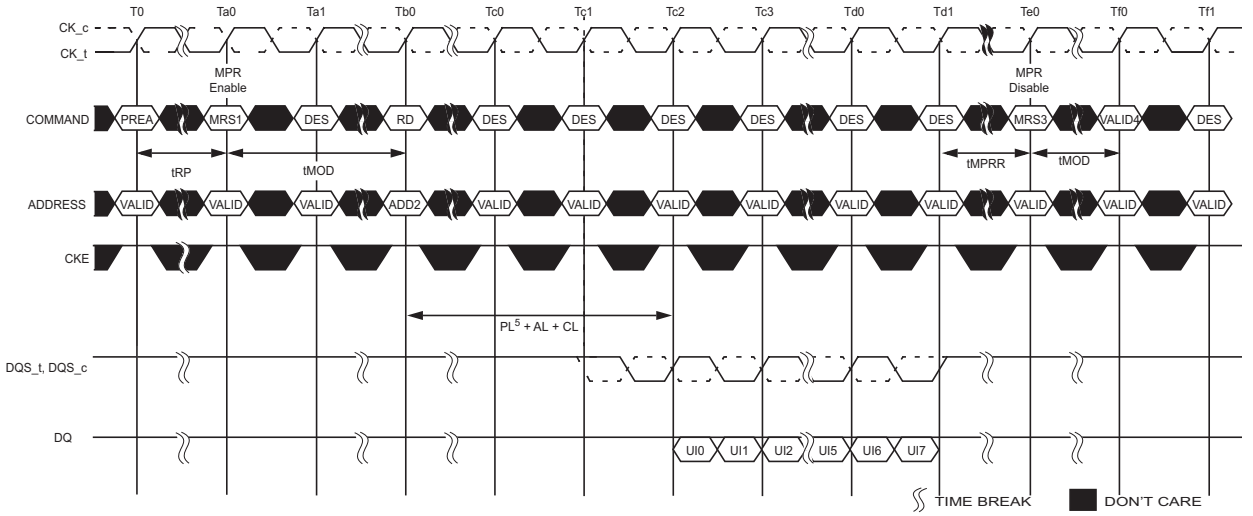
MRS MR3, Opcode A2= ‘0b’

All subsequent reads and writes from DRAM array

Wait until tMRD and tMOD are satisfied

Continue with regular DRAM commands like Activate.

MPR Read Timing



NOTE 1 Multi-Purpose Registers Read/Write Enable (MR3 A2 = 1)

NOTE 2 Address setting

- A[1:0] = ‘00’b (data burst order is fixed starting at nibble, always 00b here)

- A[2]= ‘0’b (For BL=8, burst order is fixed at 0,1,2,3,4,5,6,7)

- BA1 and BA0 indicate the MPR location

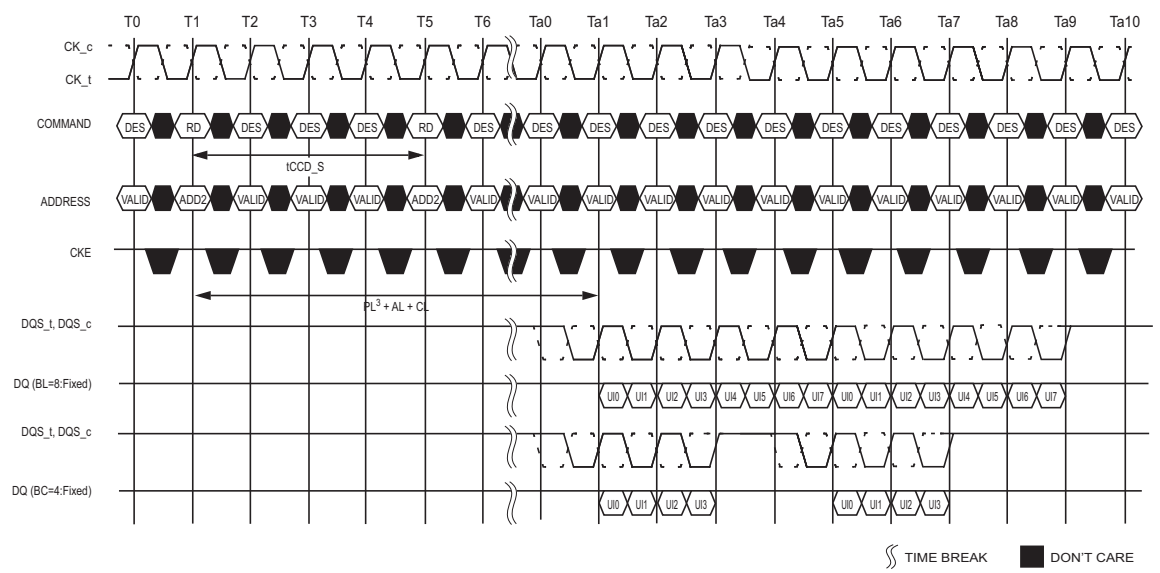
- A10 and other address pins are don’t care including BG1 and BG0. A12 is don’t care when MR0 A[1:0] = ‘00’ or ‘10’ and must be ‘1’b when MR0 A[1:0] = ‘01’

NOTE 3 Multi-Purpose Registers Read/Write Disable (MR3 A2 = 0)

NOTE 4 Continue with regular DRAM command.

NOTE 5 PL (Parity latency) is added to Data output delay when C/A parity latency mode is enabled.

MPR Back to Back Read Timing



NOTE 1 tCCD_S = 4, Read Preamble = 1tCK

NOTE 2 Address setting

- A[1:0] = ‘00’b (data burst order is fixed starting at nibble, always 00b here)

- A[2]= ‘0’b (For BL=8, burst order is fixed at 0,1,2,3,4,5,6,7)

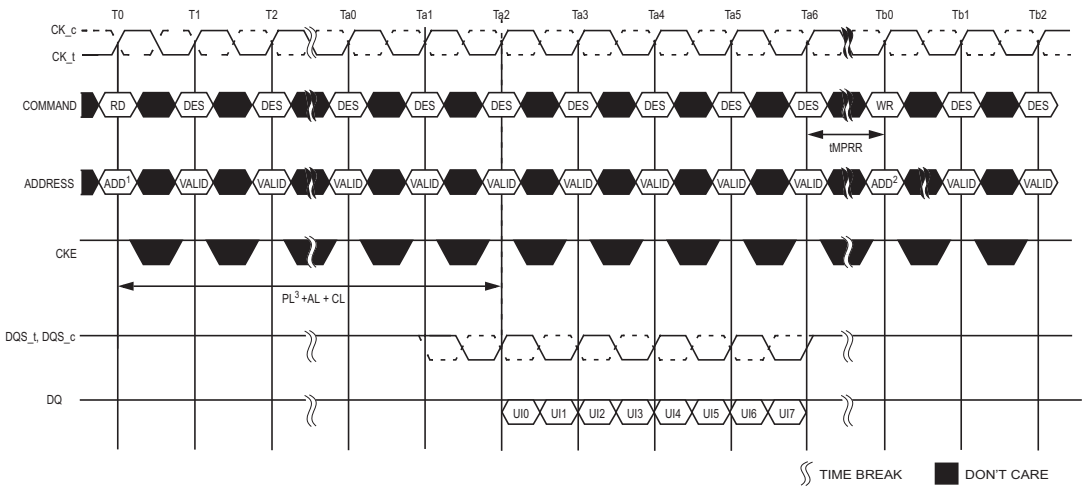
(For BC=4, burst order is fixed at 0,1,2,3,T,T,T,T)

- BA1 and BA0 indicate the MPR location

- A10 and other address pins are don’t care including BG1 and BG0. A12 is don’t care when MR0 A[1:0] = ‘00’ or ‘10’ and must be ‘1’b when MR0 A[1:0] = ‘01’

NOTE 3 PL (Parity latency) is added to Data output delay when C/A parity latency mode is enabled.

MPR Read to Write Timing



NOTE 1 Address setting

- A[1:0] = ‘00’b (data burst order is fixed starting at nibble, always 00b here)

- A[2]= ‘0’b (For BL=8, burst order is fixed at 0,1,2,3,4,5,6,7)

- BA1 and BA0 indicate the MPR location

- A10 and other address pins are don’t care including BG1 and BG0. A12 is don’t care when MR0 A[1:0] = ‘00’ or ‘10’ and must be ‘1’b when MR0 A[1:0] = ‘01’

NOTE 2 Address setting

- BA1 and BA0 indicate the MPR location

- A [7:0] = data for MPR

- A10 and other address pins are don’t care

NOTE 3 PL (Parity latency) is added to Data output delay when C/A parity latency mode is enabled.

MPR Writes

DDR4 allows 8 bit writes to the MPR location using the address bus A7:A0.

UI and Address Mapping for MPR Location

MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
SDRAM Address	A7	A6	A5	A4	A3	A2	A1	A0
UI	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7

STEPS:

DLL must be locked prior to MPR Writes. If DLL is Enabled : MR1[A0 = 1]

Precharge all

Wait until tRP is satisfied

MRS MR3, Opcode A2='1'b

Redirect all subsequent read and writes to MPR locations

Wait until tMRD and tMOD satisfied.

Write command

BA1 and BA0 indicate the MPR location

A [7:0] = data for MPR

Wait until tWR_MPR satisfied, so that DRAM to complete MPR write transaction.

Memory controller repeats these calibration writes and reads until data capture at memory controller is optimized.

After end of last MPR read burst, wait until tMPRR is satisfied

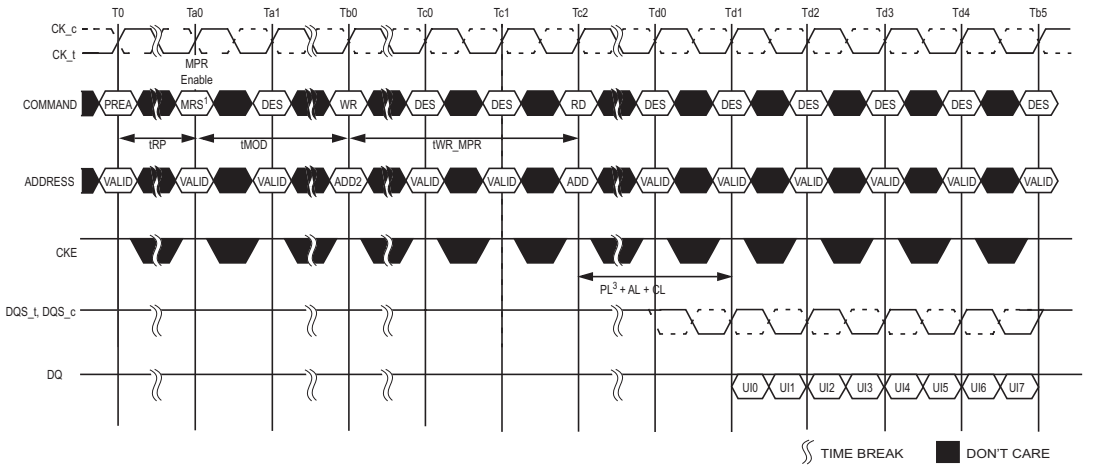
MRS MR3, Opcode A2= '0b'

All subsequent reads and writes from DRAM array

Wait until tMRD and tMOD are satisfied

Continue with regular DRAM commands like Activate.

MPR Write Timing and Write to Read Timing



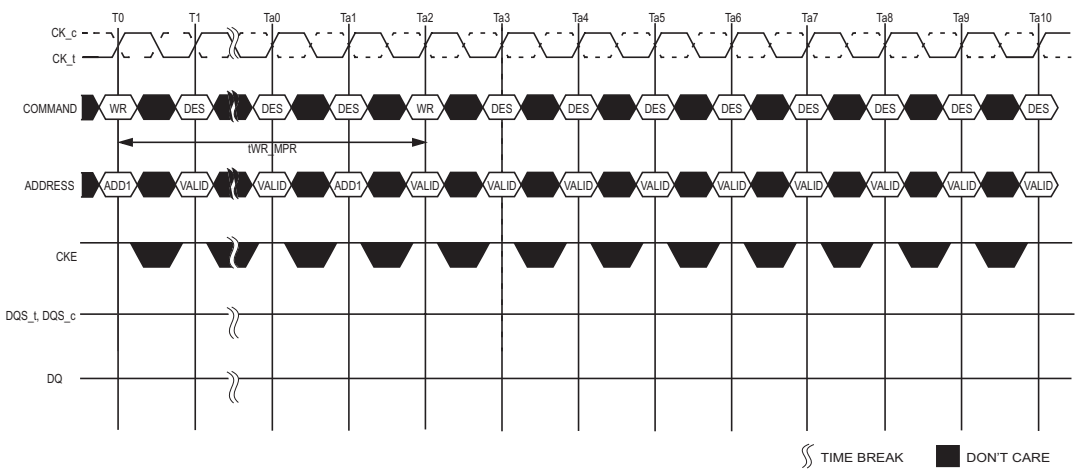
NOTE 1 Multi-Purpose Registers Read/Write Enable (MR3 A2 = 1)

NOTE 2 Address setting

- BA1 and BA0 indicate the MPR location
- A [7:0] = data for MPR
- A10 and other address pins are don't care.

NOTE 3 PL (Parity latency) is added to Data output delay when C/A parity latency mode is enabled.

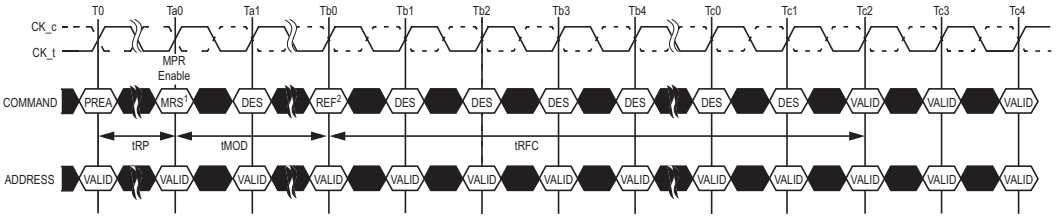
MPR Back to Back Write Timing



NOTE 1 Address setting

- BA1 and BA0 indicate the MPR location
- A [7:0] = data for MPR
- A10 and other address pins are don't care.

Refresh Command Timing

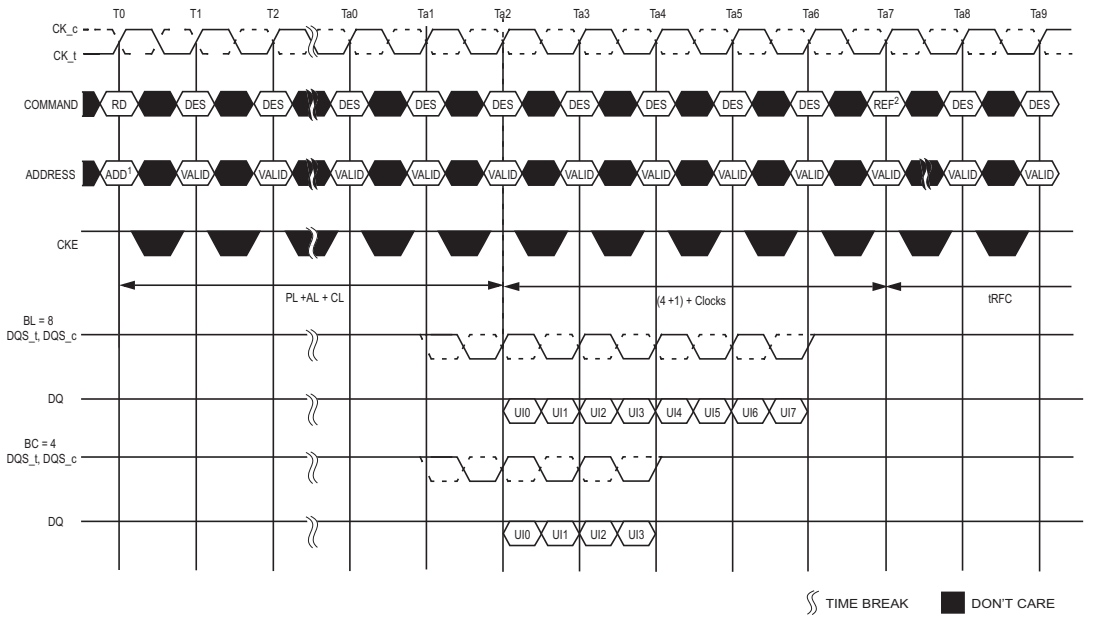


NOTE 1 Multi-Purpose Registers Read/Write Enable (MR3 A2 = 1)

- Redirect all subsequent read and writes to MPR locations

NOTE 2 1x Refresh is only allowed when MPR mode is Enable.

Read to Refresh Command Timing



NOTE 1 Address setting

- A[1:0] = ‘00’b (data burst order is fixed starting at nibble, always 00b here)

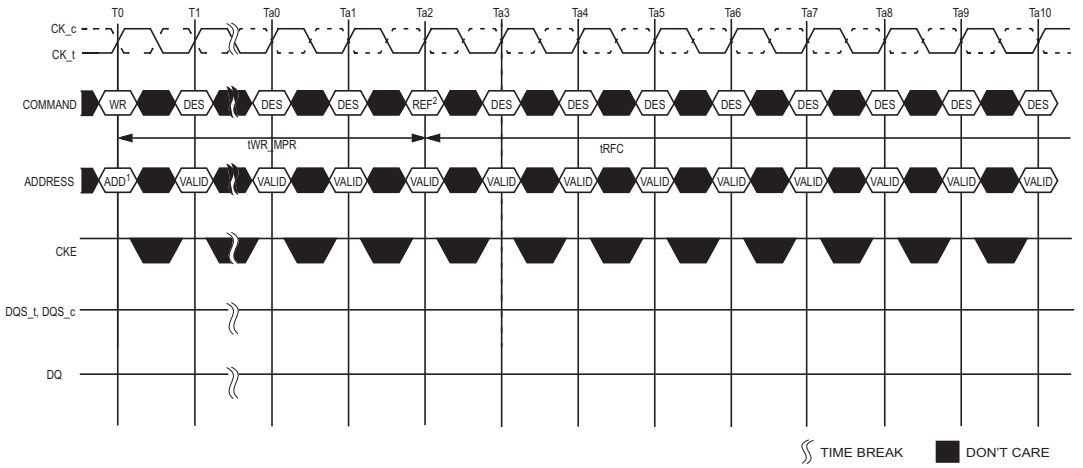
- A[2]= ‘0’b (For BL=8, burst order is fixed at 0,1,2,3,4,5,6,7)

- BA1 and BA0 indicate the MPR location

- A10 and other address pins are don’t care including BG1 and BG0. A12 is don’t care when MR0 A[1:0] = ‘00’ or ‘10’ and must be ‘1’b when MR0 A[1:0] = ‘01’

NOTE 2 1x Refresh is only allowed when MPR mode is Enable.

Write to Refresh Command Timing



NOTE 1 Address setting

- BA1 and BA0 indicate the MPR location
- A [7:0] = data for MPR
- A10 and other address pins are don't care.

NOTE 2 1x Refresh is only allowed when MPR mode is Enable.

MPR Read Data format

Mode bits in MR3: (A12, A11) are used to select the data return format for MPR reads. The DRAM is required to drive associated strobes with the read data returned for all read data formats.

Serial return implies that the same pattern is returned on all DQ lanes as shown in figure below. Data from the MPR is used on all DQ lanes for the serial return case. Reads from MPR page0, MPR page1 and MPR page3 are allowed with serial data return mode.In this example the pattern programmed in the MPR register is 0111 111: MPR Location [7:0].

x4 Device

Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	1	1	1	1	1	1	1
DQ1	0	1	1	1	1	1	1	1
DQ2	0	1	1	1	1	1	1	1
DQ3	0	1	1	1	1	1	1	1

x8 Device

Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	1	1	1	1	1	1	1
DQ1	0	1	1	1	1	1	1	1
DQ2	0	1	1	1	1	1	1	1

Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ3	0	1	1	1	1	1	1	1
DQ4	0	1	1	1	1	1	1	1
DQ5	0	1	1	1	1	1	1	1
DQ6	0	1	1	1	1	1	1	1
DQ7	0	1	1	1	1	1	1	1

x16 Device

Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	1	1	1	1	1	1	1
DQ1	0	1	1	1	1	1	1	1
DQ2	0	1	1	1	1	1	1	1
DQ3	0	1	1	1	1	1	1	1
DQ4	0	1	1	1	1	1	1	1
DQ5	0	1	1	1	1	1	1	1
DQ6	0	1	1	1	1	1	1	1
DQ7	0	1	1	1	1	1	1	1
DQ8	0	1	1	1	1	1	1	1
DQ9	0	1	1	1	1	1	1	1
DQ10	0	1	1	1	1	1	1	1
DQ11	0	1	1	1	1	1	1	1
DQ12	0	1	1	1	1	1	1	1
DQ13	0	1	1	1	1	1	1	1
DQ14	0	1	1	1	1	1	1	1
DQ15	0	1	1	1	1	1	1	1

Parallel return implies that the MPR data is retuned in the first UI and then repeated in the remaining UI's of the burst as shown in the figure below. Data from Page0 MPR registers can be used for the parallel return case as well. Read from MPR page1, MPR page2 and MPR page3 are not allowed with parallel data return mode. In this example the pattern programmed in the Page 0 MPR registeris 0111 1111:MPR Location [7:0]. For the case of x4, only the first four bits are used (0111:MPR Location [7:4] in this example). For thecase of x16, the same pattern is repeated on upper and lower bytes.

x4 Device

Parallel	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	0	0	0	0	0	0	0
DQ1	1	1	1	1	1	1	1	1
DQ2	1	1	1	1	1	1	1	1

Parallel	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ3	1	1	1	1	1	1	1	1

x8 Device

Parallel	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	0	0	0	0	0	0	0
DQ1	1	1	1	1	1	1	1	1
DQ2	1	1	1	1	1	1	1	1
DQ3	1	1	1	1	1	1	1	1
DQ4	1	1	1	1	1	1	1	1
DQ5	1	1	1	1	1	1	1	1
DQ6	1	1	1	1	1	1	1	1
DQ7	1	1	1	1	1	1	1	1

x16 Device

Parallel	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	0	0	0	0	0	0	0
DQ1	1	1	1	1	1	1	1	1
DQ2	1	1	1	1	1	1	1	1
DQ3	1	1	1	1	1	1	1	1
DQ4	1	1	1	1	1	1	1	1
DQ5	1	1	1	1	1	1	1	1
DQ6	1	1	1	1	1	1	1	1
DQ7	1	1	1	1	1	1	1	1
DQ8	1	1	1	1	1	1	1	1
DQ9	1	1	1	1	1	1	1	1
DQ10	1	1	1	1	1	1	1	1
DQ11	1	1	1	1	1	1	1	1
DQ12	1	1	1	1	1	1	1	1
DQ13	1	1	1	1	1	1	1	1
DQ14	1	1	1	1	1	1	1	1
DQ15	1	1	1	1	1	1	1	1

The third mode of data return is the staggering of the MPR data across the lanes. In this mode a read command is issued to a specific MPR and then the data is returned on the DQ from different MPR registers. Read from MPR page1, MPR page2, and MPR page3 are not allowed with staggered data return mode.

For a x4 device, a read to MPR0 will result in data from MPR0 being driven on DQ0, data from MPR1 on DQ1 and so forth as shown below.

A read command to MPR1 will result in data from MPR1 being driven on DQ0, data from MPR2 on DQ1 and so forth as shown below. Reads from MPR2 and MPR3 are also shown below.

MPR Readout Staggered Format, x4

MPR0(BA[1:0]="00')		MPR1(BA[1:0]="01')		MPR2(BA[1:0]="10')		MPR3(BA[1:0]="11')	
Stagger	**UI0-7**	**Stagger**	**UI0-7**	**Stagger**	**UI0-7**	**Stagger**	**UI0-7**
DQ0	MPR0	DQ0	MPR1	DQ0	MPR2	DQ0	MPR3
DQ1	MPR1	DQ1	MPR2	DQ1	MPR3	DQ1	MPR0
DQ2	MPR2	DQ2	MPR3	DQ2	MPR0	DQ2	MPR1
DQ3	MPR3	DQ3	MPR0	DQ3	MPR1	DQ3	MPR2

It is expected that the DRAM can respond to back to back read commands to MPR for all DDR4 frequencies so that a stream as follows can be created on the data bus with no bubbles or clocks between read data. In this case controller issues a sequence of RD MPR0, RD MPR1, RD MPR2, RD MPR3, RD MPR0, RD MPR1, RD MPR2 and RD MPR3.

MPR Readout Staggered Format, x4 (Back to Back read commands)

Stagger	UI0-7	UI8-15	UI16-23	UI23-31	UI32-39	UI40-47	UI48-55	UI56-63
DQ0	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3
DQ1	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0
DQ2	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1
DQ3	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2

The following figure shows a read command to MPR0 for a x8 device.The same pattern is repeated on the lower nibble as on the upper nibble. Reads to other MPR location follows the same format as for x4 case.

A read example to MPR0 for x8 and x16 device is shown below.

MPR Readout Staggered Format, x8 and x16

x8		x16			
Stagger	**UI0-7**	**Stagger**	**UI0-7**	**Stagger**	**UI0-7**
DQ0	MPR0	DQ0	MPR0	DQ8	MPR0
DQ1	MPR1	DQ1	MPR1	DQ9	MPR1
DQ2	MPR2	DQ2	MPR2	DQ10	MPR2
DQ3	MPR3	DQ3	MPR3	DQ12	MPR3
DQ4	MPR0	DQ4	MPR0	DQ13	MPR0
DQ5	MPR1	DQ5	MPR1	DQ14	MPR1
DQ6	MPR2	DQ6	MPR2	DQ15	MPR2
DQ7	MPR3	DQ7	MPR3	DQ16	MPR3

Four MPR pages are provided in DDR4 SDRAM. Page 0 is for both read and write, and pages 1,2 and 3 are read-only. Any MPR location (MPR0-3) in page 0 can be readable through any of three readout modes (serial, parallel or staggered), but pages 1, 2 and 3 support only the serial readout mode.

After power up, the content of MPR page 0 should have the default value as defined in the table. MPR page 0 can be writeable only when MPR write command is issued by controller. Unless MPR write command is issued, DRAM must keep the default value permanently, and should never change the content on its own for any purpose.

MPR page0 (Training pattern)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	note
BA1:BA0	00 = MPR0	0	1	0	1	0	1	0	1	Read/Write (default value)
	01= MPR1	0	0	1	1	0	0	1	1	
	10 = MPR2	0	0	0	0	1	1	1	1	
	11 = MPR3	0	0	0	0	0	0	0	0	

NOTE 1 MPRx using A7:A0 that A7 is mapped to location [7] and A0 is mapped to location [0].

MPR page1 (CA parity error log)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	note
BA1:BA0	00 = MPR0	A7	A6	A5	A4	A3	A2	A1	A0	Read-only
	01= MPR1	$\overline{CAS}$/A15	$\overline{WE}$/A14	A13	A12	A11	A10	A9	A8	
	10 = MPR2	PAR	$\overline{ACT}$	BG1	BG0	BA1	BA0	A17	$\overline{RAS}$/A16	
	11 = MPR3	CRC Error Status	CA Parity Error Status	CA Parity Latency[4]			C2	C1	C0	
				MR5.A[2]	MR5.A[1]	MR5.A[0]				

NOTE 1 MPR used for C/A parity error log readout is enabled by setting A[2] in MR3

NOTE 2 For higher density of DRAM, where A[17] is not used, MPR2[1] should be treated as don't care.

NOTE 3 If a device is used in monolithic application, where C[2:0] are not used, then MPR3[2:0] should be treated as don't care.

MPR page2 (MRS Readout)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	note
BA1:BA0	00 = MPR0	RFU	RFU	RFU	Temperature Sen-sor Status[1]		CRC Write En-able	Rtt_WR		read-only
		-	-	-	-	-	MR2	MR2		
		-	-	-	-	-	A12	A10	A9	
	01= MPR1	Vref DQ Trng range	Vref DQ training Value						Gear-down En-able	
		MR6	MR6							
		A6	A5	A4	A3	A2	A1	A0	A3	
	10 = MPR2	CAS Latency				RFU	CAS Write Latency			
		MR0				-	MR2			
		A6	A5	A4	A2	-	A5	A4	A3	
	11 = MPR3	Rtt_Nom			Rtt_Park			Driver Impedance		
		MR1			MR5			MR2		
		A10	A9	A6	A8	A7	A6	A2	A1	

NOTE 1 Temperature Sen-sor Status Readout

MPR0 bit A4	MPR0 bit A3	Refresh Rate Range	MR3[5]
0	0	Sub 1x refresh (>tREFI)	**MR3 bit A5=1 (Temperature sensor readout = Enabled)** DRAM updates the temperature sensor status to MPR Page 2 (MPR0 bits A[4:3]). Temperature data is guaranteed by the DRAM to be no more than 32ms old at the time of MPR Read of the Temperature Sensor Status bits. **MR3 bit A5=0 (Temperature sensor readout = Disabled)** DRAM disables updates to the temperature sensor status in MPR Page 2(MPR0-bit A[4:3])
0	1	1x refresh rate (= tREFI)	
1	0	2x refresh rate (1/2 x tREFI)	
1	1	RFU	

MPR page3 (Vendor purpose only)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	note
BA1:BA0	00 = MPR0	don't care	don't care	don't care	don't care	don't care	don't care	don't care	1	read-only
	01= MPR1	don't care	don't care	don't care	don't care	don't care	don't care	don't care	1	
	10 = MPR2	don't care	don't care	don't care	don't care	don't care	don't care	don't care	1	
	11 = MPR3	don't care	don't care	don't care	don't care	don't care	don't care	don't care	0	

Gear Down Mode

The following ballot represents the sequence for the gear down mode. The DRAM defaults in 1/2 rate(1N) clock mode and utilizes a low frequency MRS command followed by a sync pulse to align the proper clock edge for operating the control lines $\overline{CS}$, CKE and ODT in 1/4rate(2N) mode. For operation in 1/2 rate mode no MRS command for geardown or sync pulse is required. DRAM defaults in 1/2 rate mode.

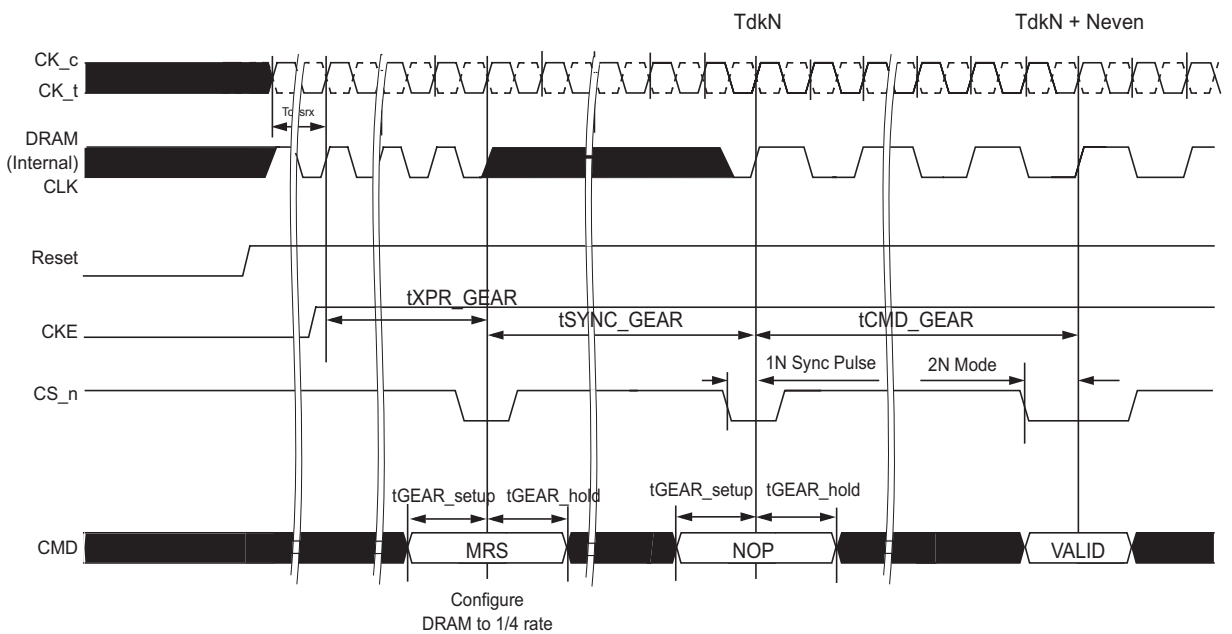
General sequence for operation in geardown during initialization

- DRAM defaults to a 1/2 rate(1N mode) internal clock at power up/reset
- Assertion of reset
- Assertion of CKE enables the rank
- MRS is accessed with a low frequency N*tck MRS geardown CMD.(Ntck static MRS command qualified by 1N $\overline{CS}$).
- MC sends 1N sync pulse with a low frequency N*tck NOP CMD; CK tSYCN_GEAR is an even number of clocks; Sync pulse on even edge from MRS CMD.
- Normal operation in 2N starts tCMD_GEAR clocks later

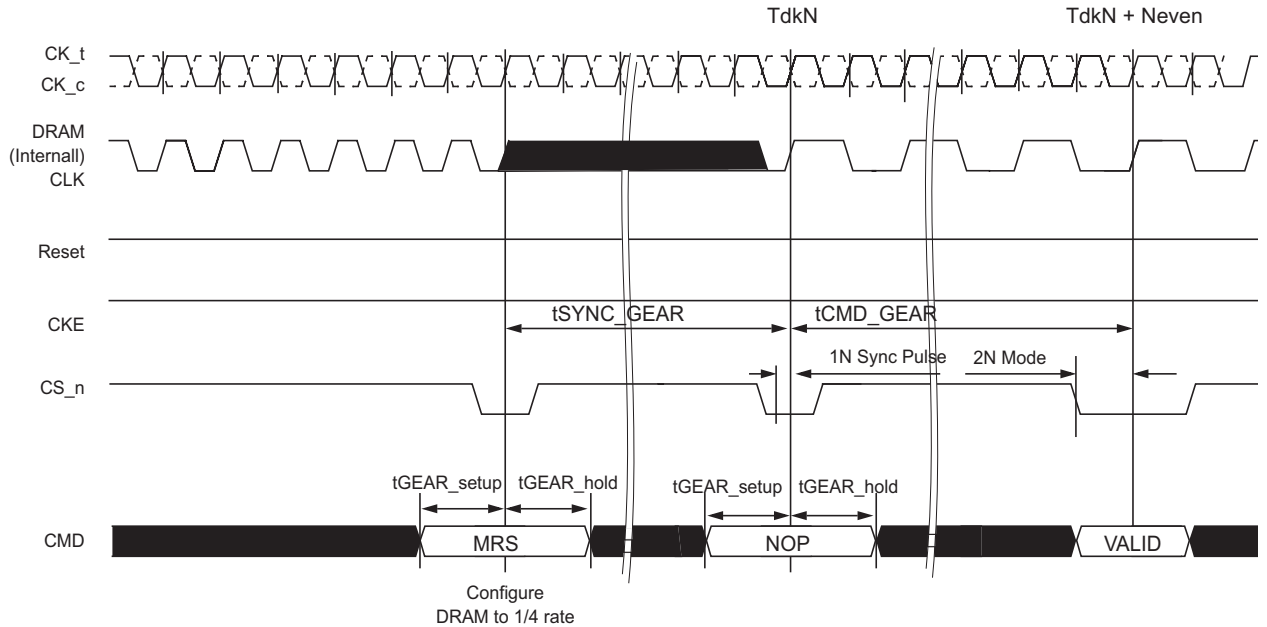
For the operation of geardown mode in 1/4 rate, the following MR settings should be applied.

- CAS Latency (MR0 A[6:4,2]) : Even numbers
- Write Recovery and Read to Precharge (MR0 A[11:9]) : Even numbers
- Additive Latency (MR1 A[4:3]) : 0, CL -2
- CAS Write Latency (MR2 A[5:3]) : Even numbers
- $\overline{CS}$ to Command/Address Latency Mode (MR4 A[8:6]) : Even numbers
- CA Parity Latency Mode (MR5 A[2:0]) : Even numbers

Gear down (2N) mode entry sequence during initialization



Gear down (2N) mode entry sequence during normal operation

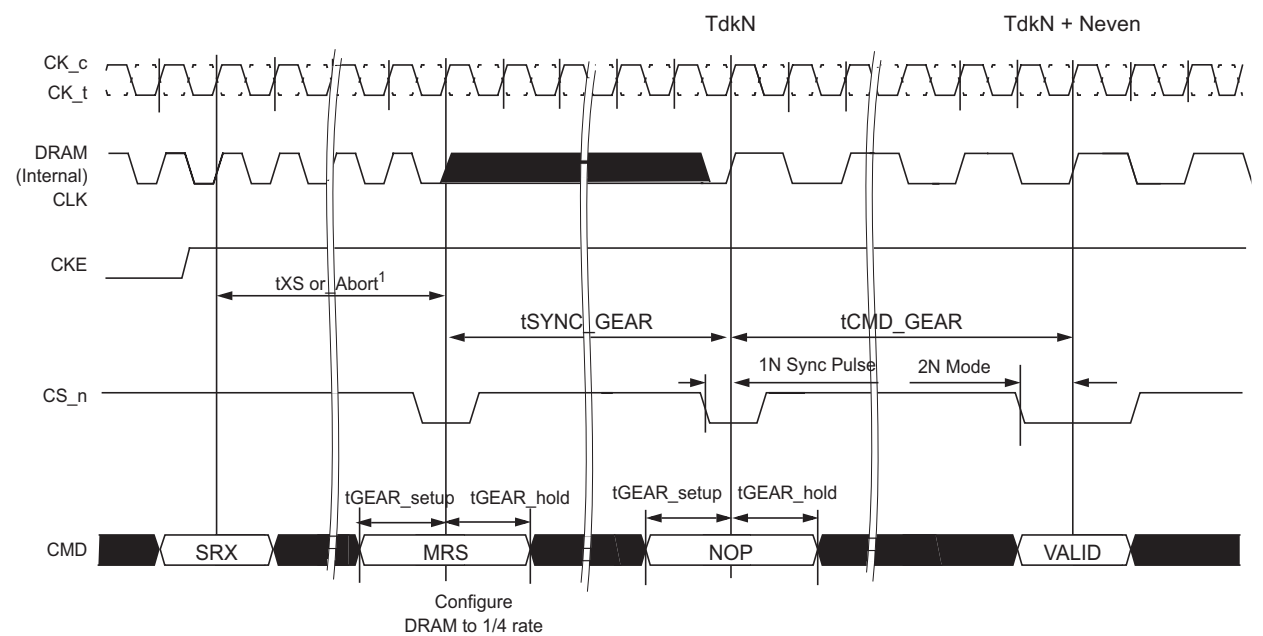


If operation is 1/2 rate(1N) mode before and after self refresh, no MRS command or sync pulse is required during self refresh exit. The min exit delay is tXS, or tXS_Abort to the first valid command.

If operation is in 1/4 rate mode after self refresh exit, the DRAM requires a MRS command and sync pulse as illustrated in the figure below.

DRAM must internally reset to 1N mode from 2N mode during self Refresh and Max Power Saving Mode to properly align internal clock edge with the sync pulse.Illustration below for the DRAM operating in 1/4 rate mode before and after self refresh entry and exit.

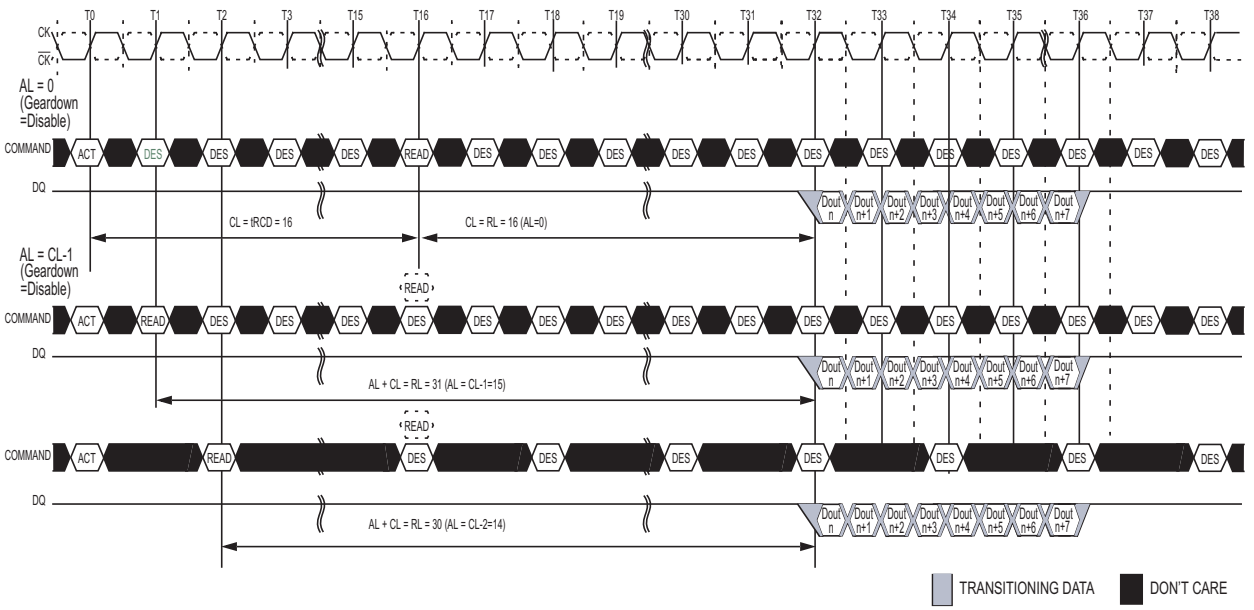
Gear down (2N) mode entry sequence after self refresh exit (SRX)



NOTE 1 CKE High Assert to Gear Down Enable Time (tXS, tXS_Abort) depend on MR setting. A correspondence of tXS/tXS_Abort and MR Setting isas follows.

- MR4[A9] = 0 : tXS
- MR4[A9] = 1 : tXS_Abort

Comparison Timing Diagram Between Geardown Disable and Enable



NOTE 1 BL=8, tRCD=CL=16

NOTE 2 DOUT n = data-out from column n.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read $\overline{DBI}$ = Disable.

Maximum Power Saving Mode

This mode provides lowest power consuming mode which could be similar to the Self-Refresh status with no internal refresh activity.When DDR4 SDRAM is in the maximum power saving mode, it does not need to guarantee data retention nor respond to any external command (except maximum power saving mode exit and asserting $\overline{\text{RESET}}$ signal LOW) to minimize the power consumption.

Mode entry

Max power saving mode is entered through an MRS command. For devices with shared control/address signals, a single DRAM device can be entered into the max power saving mode using the per DRAM Addressability MRS command.

Note that large $\overline{\text{CS}}$ hold time to CKE upon the mode exit may cause DRAM malfunction, thus it is required that the CA parity, CAL and Gear Down modes are disabled prior to the max power saving mode entry MRS command.

Maximum Power Saving mode Entry

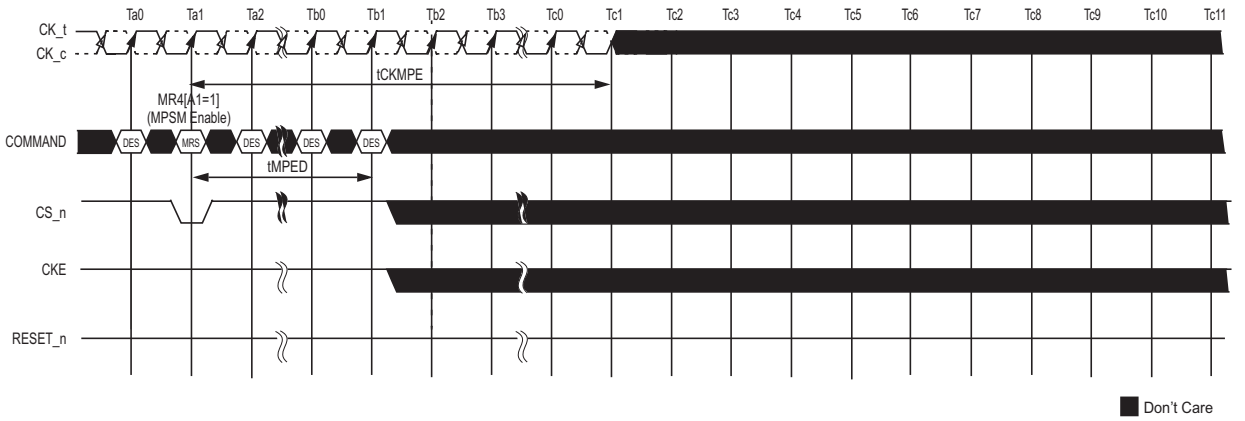
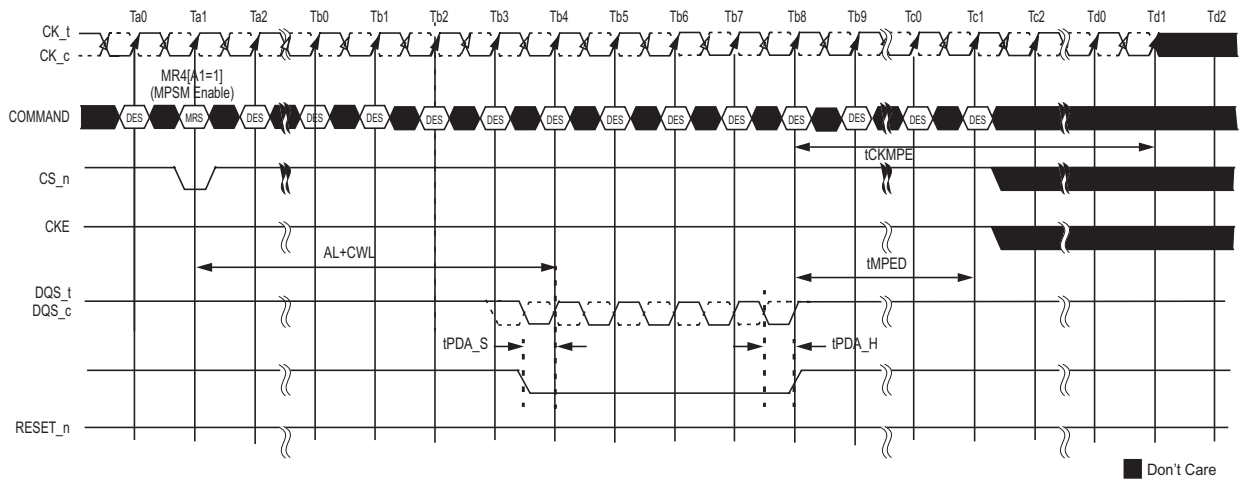


Figure below illustrates the sequence and timing parameters required for the maximum power saving mode with the per DRAM addressability (PDA).

Maximum Power Saving mode Entry with PDA

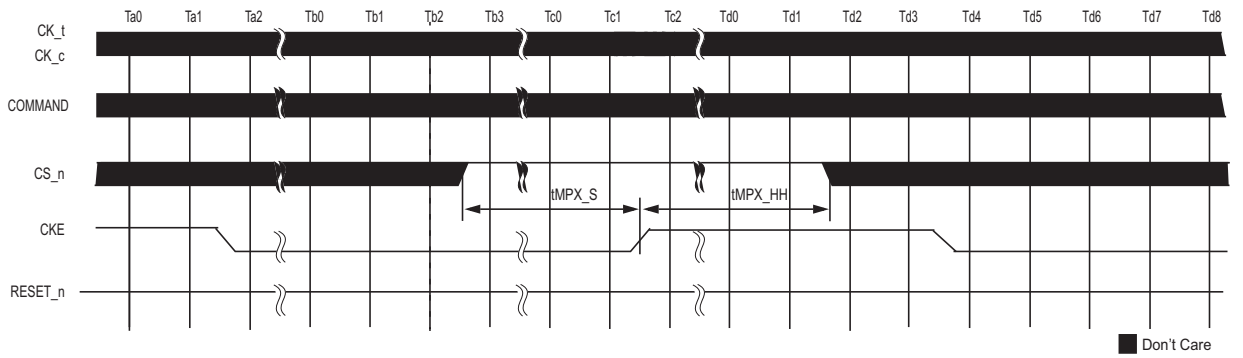


When entering Maximum Power Saving mode, only DES commands are allowed until tMPED is satisfied. After tMPED period from the mode entry command, DRAM is not responsive to any input signals except CS, CKE and RESET signals, and all other input signals can be High-Z. CLK should be valid for tCKMPE period and then can be High-Z.

CKE transition during the mode

CKE toggle is allowed when DRAM is in the maximum power saving mode. To prevent the device from exiting the mode, CS should be issued 'High' at CKE 'L' to 'H' edge with appropriate setup tMPX_S and hold tMPX_HH timings.

CKE Transition Limitation to hold Maximum Power Saving Mode

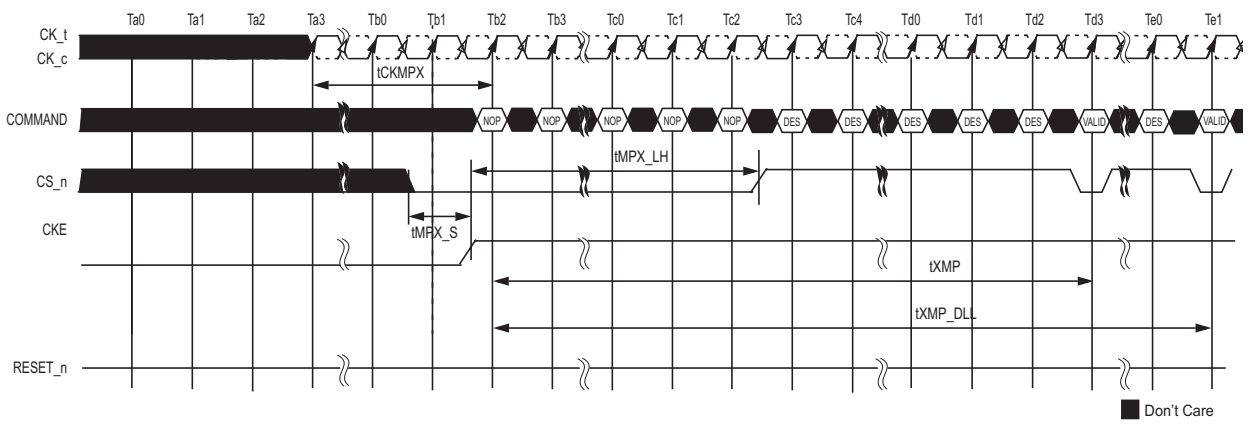


Mode exit

DRAM monitors CS signal level and when it detects CKE 'L' to 'H' transition, and either exits from the power saving mode or stay in the mode depending on the CS signal level at the CKE transition. Because CK receivers are shut down during this mode, CS = 'L' is captured by rising edge of the CKE signal. If CS signal level is detected 'L', then the DRAM initiates internal exit procedure from the power saving mode. CK must be restarted and stable tCKMPX period before the device can exit the maximum power saving mode. During the exit time tXMP, any valid commands except DES command is not allowed to DDR4 SDRAM and also tXMP_DLL, any valid commands requiring a locked DLL is not allowed to DDR4 SDRAM.

When recovering from this mode, the DRAM clears the MRS bits of this mode. It means that the setting of MR4 [A1] is move to '0' automatically.

Maximum Power Saving Mode Exit Sequence



Command Address Parity (CA Parity)

[A2:A0] of MR5 are defined to enable or disable C/A Parity in the DRAM. The default state of the C/A Parity bits is disabled. If C/A parity is enabled by programming a non-zero value to C/A Parity Latency in the mode register (the Parity Error bit must be set to zero when enabling C/A any Parity mode), then the DRAM has to ensure that there is no parity error before executing the command. The additional delay for executing the commands versus a parity disabled mode is programmed in the mode register when C/A Parity is enabled (Parity Latency) and is applied to all commands.When C/A Parity is enabled, only DES is allowed between valid commands to prevent DRAM from any malfunctioning. CA Parity Mode is supported when DLL-on Mode is enabled, use of CA Parity Mode when DLL-off Mode is enabled is not allowed.

C/A Parity signal (PAR) covers $\overline{ACT}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and the address bus including bank address and bank group bits. The control signals CKE, ODT and $\overline{CS}$ are not included. (e.g. for a 4 Gbit x4 monolithic device, parity is computed across BG0, BG1,BA1, BA0, A16/$\overline{RAS}$, A15/$\overline{CAS}$, A14/$\overline{WE}$, A13-A0 and $\overline{ACT}$). (DRAM should internally treat any unused address pins as 0's, e.g., if a common die has stacked pins but the device is used in a monolithic application then the address pins used for stacking should internally be treated as 0's)

The convention of parity is even parity i.e. valid parity is defined as an even number of ones across the inputs used for parity computation combined with the parity signal. In other words the parity bit is chosen so that the total number of 1's in the transmitted signal, including the parity bit is even.

If a DRAM detects a C/A parity error in any command as qualified by $\overline{CS}$ then it must perform the following steps:

- Ignore the erroneous command. Commands in max NnCK window (tPAR_UNKNOWN) prior to the erroneous command are not guaranteed to be executed. When a READ command in this NnCK window is not executed, the DRAM does not activate DQS outputs.

- Log the error by storing the erroneous command and address bits in the error log. (MPR page1)

- Set the Parity Error Status bit in the mode register to '1'. The Parity Error Status bit must be set before the $\overline{ALERT}$ signal is released by the DRAM (i.e. tPAR_ALERT_ON + tPAR_ALERT_PW(min)).

- Assert the $\overline{ALERT}$ signal to the host ($\overline{ALERT}$ is active low) within tPAR_ALERT_ON time.

- Wait for all in-progress commands to complete. These commands were received tPAR_UNKOWN before the erroneous command. If a parity error occurs on a command issued between the tXS_Fast and tXS window after self-refresh exit then the DRAM maydelay the de-assertion of $\overline{ALERT}$ signal as a result of any internal on going refresh.

- Wait for tRAS_min before closing all the open pages. The DRAM is not executing any commands during the window defined by(tPAR_ALERT_ON + tPAR_ALERT_PW).

- After tPAR_ALERT_PW_min has been satisfied, the DRAM may de-assert $\overline{ALERT}$.

- After the DRAM has returned to a known pre-charged state it may de-assert $\overline{ALERT}$.

- After (tPAR_ALERT_ON + tPAR_ALERT_PW), the DRAM is ready to accept commands for normal operation. Parity latency will be in effect, however, parity checking will not resume until the memory controller has cleared the Parity Error Status bit by writing a '0'(the DRAM will execute any erroneous commands until the bit is cleared).

- It is possible that the DRAM might have ignored a refresh command during the (tPAR_ALERT_ON + tPAR_ALERT_PW) window or the refresh command is the first erroneous frame so it is recommended that the controller issues extra refresh cycles as needed.

- The Parity Error Status bit may be read anytime after (tPAR_ALERT_ON + tPAR_ALERT_PW) to determine which DRAM had theerror. The DRAM maintains the Error Log for the first erroneous command until the Parity Error Status bit is reset to '0'.

Mode Register for C/A Parity Error is defined as follows. C/A Parity Latency bits are write only, Parity Error Status bit is read/write and error logs are read only bits. The controller can only program the Parity Error Status bit to '0'. If the controller illegally attempts to write a '1' to the Parity Error Status bit the DRAM does not guarantee that parity will be checked. The DRAM may opt to block the controller from writing a '1' to the Parity Error Status bit.

Mode Registers for C/A Parity

C/A Parity Latency MR5[2:0]*	Speed bins	C/A Parity Error Status MR5[4]	Errant C/A Frame
000 = Disabled	-	0=clear	C2-C0, $\overline{ACT}$, BG1, $\overline{BG0}$, BA0, $\overline{BA1}$, PAR, A17, A16/ $\overline{RAS}$, A15/$\overline{CAS}$, A14/$\overline{WE}$, A13:A0
001= 4 Clocks	1600,1866,2133		
010= 5 Clocks	2400	1=Error	
011= 6 Clocks	RFU		
100= 8 Clocks	RFU		

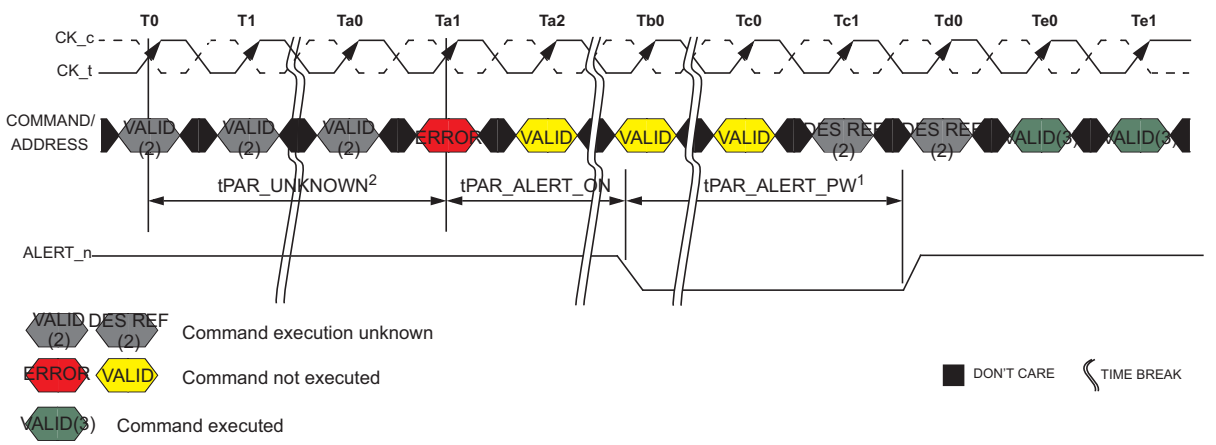
NOTE 1 Parity Latency is applied to all commands.

NOTE 2 Parity Latency can be changed only from a C/A Parity disabled state, i.e. a direct change from PL=3 -> PL=4 is not allowed. Correct sequenceis PL=3 -> Disabled -> PL=4

NOTE 3 Parity Latency is applied to write and read latency. Write Latency = AL+CWL+PL. Read Latency = AL+CL+PL.

DDR4 SDRAM supports MR bit for 'Persistent Parity Error Mode'. This mode is enabled by setting MR5 A9=High and when it is enabled, DRAM resumes checking CA Parity after the $\overline{ALERT}$ is deasserted, even if Parity Error Status bit is set as High. If multiple errors occur before the Error Status bit is cleared the Error log in MPR page 1 should be treated as 'Don't Care'. In 'Persistent Parity Error Mode' the $\overline{ALERT}$ pulse will be asserted and deasserted by the DRAM as defined with the min. and max. value for tPAR_ALERT_PW. The controller must issue DESELECT commands once it detects the $\overline{ALERT}$ signal, this response time is definedas tPAR_ALERT_RSP. The following figure captures the flow of events on the C/A bus and the $\overline{ALERT}$ signal.

Normal CA Parity Error Checking Operation

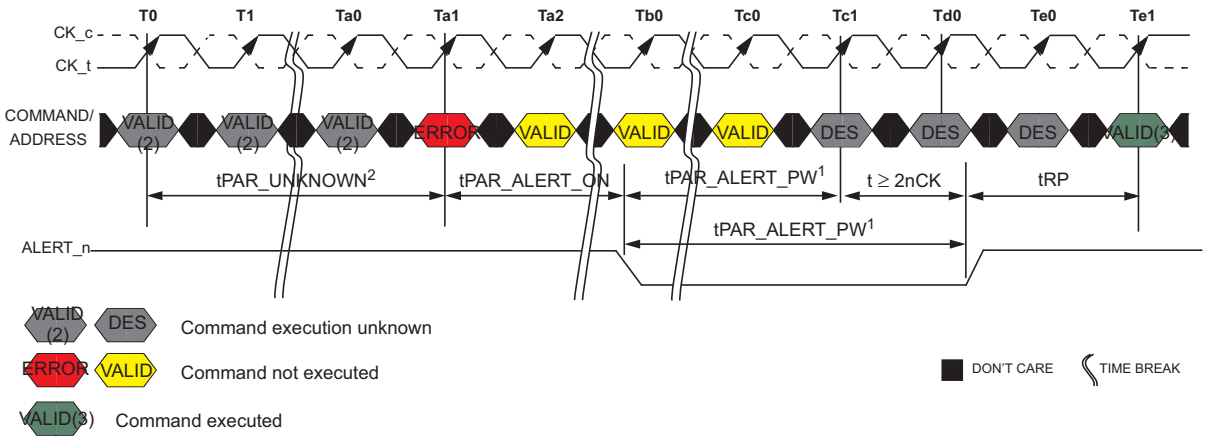


NOTE 1 DRAM is emptying queues, Precharge All and parity checking off until Parity Error Status bit cleared.

NOTE 2 Command execution is unknown the corresponding DRAM internal state change may or may not occur. The DRAM Controller should consider both cases and make sure that the command sequence meets the specifications.

NOTE 3 Normal operation with parity latency (CA Parity Persistent Error Mode disabled). Parity checking off until Parity Error Status bit cleared.

Persistent CA Parity Error Checking Operation

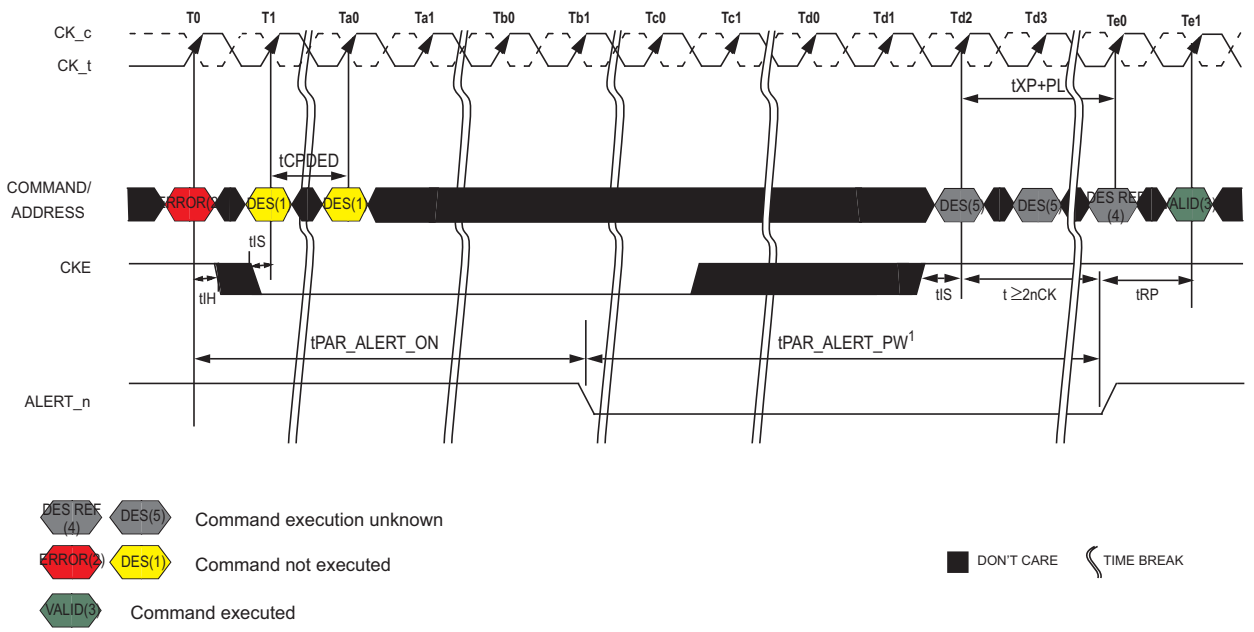


NOTE 1 DRAM is emptying queues, Precharge All and parity check re-enable finished by tPAR_ALERT_PW.

NOTE 2 Command execution is unknown the corresponding DRAM internal state change may or may not occur. The DRAM Controller should consider both cases and make sure that the command sequence meets the specifications.

NOTE 3 Normal operation with parity latency and parity checking (CA Parity Persistent Error Mode enabled).

CA Parity Error Checking - PDE/PDX



NOTE 1 Deselect command only allowed.

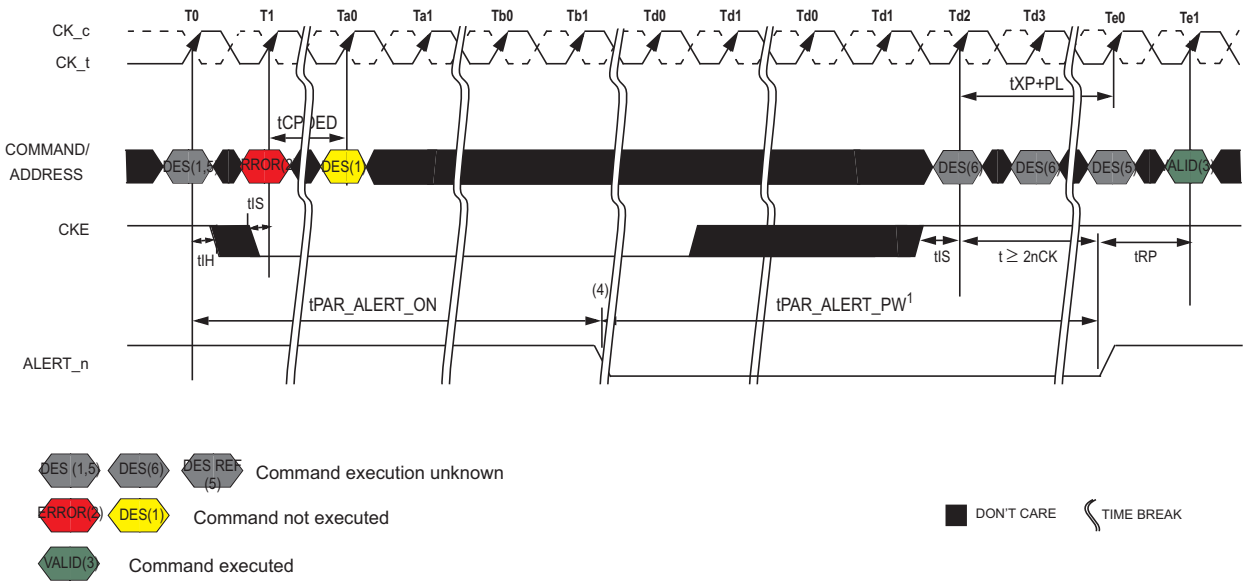
NOTE 2 Error could be Precharge or Activate.

NOTE 3 Normal operation with parity latency (CA Parity Persistent Error Mode disable). Parity checking is off until Parity Error Status bit cleared.

NOTE 4 Command execution is unknown the corresponding DRAM internal state change may or may not occur. The DRAM Controller should consider both cases and make sure that the command sequence meets the specifications.

NOTE 5 Deselect command only allowed CKE may go high prior to Td2 as long as DES commands are issued.

CA Parity Error Checking - SRE Attempt



NOTE 1 Deselect command only allowed.

NOTE 2 Self Refresh command error. DRAM masks the intended SRE command enters Precharge Down.

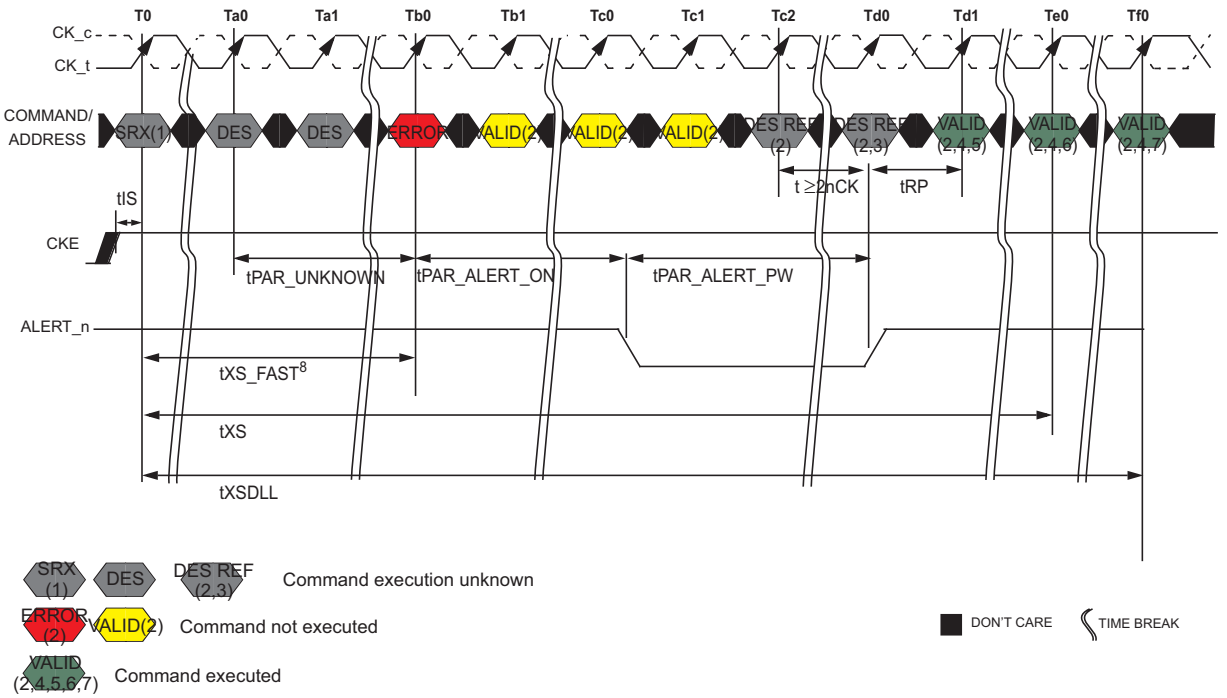
NOTE 3 Normal operation with parity latency (CA Parity Persistent Error Mode disable). Parity checking is off until Parity Error Status bit cleared.

NOTE 4 Controller can not disable dock until it has been able to have detected a possible C/A Parity error.

NOTE 5 Command execution is unknown the corresponding DRAM internal state change may or may not occur. The DRAM Controller should consider both cases and make sure that the command sequence meets the specifications.

NOTE 6 Deselect command only allowed CKE may go high prior to Tc2 as long as DES commands are issued.

CA Parity Error Checking - SRX



NOTE 1 Self Refresh Abort = Disable : MR4 [A9=0].

NOTE 2 Input commands are bounded by tXSDLL, tXS, tXS_ABORT and tXS_FAST timing.

NOTE 3 Command execution is unknown the corresponding DRAM internal state change may or may not occur. The DRAM Controller should consider both cases and make sure that the command sequence meets the specifications.

NOTE 4 Normal operation with parity latency (CA Parity Persistent Error Mode disabled). Parity checking off until Parity Error Status bit cleared.

NOTE 5 Only MRS (limited to those described in the Self-Refresh Operation section), ZQCS or ZQCL command allowed.

NOTE 6 Valid commands not requiring a locked DLL

NOTE 7 Valid commands requiring a locked DLL

NOTE 8 This figure shows the case from which the error occurred after tXS FAST. An error also occur after tXS_ABORT and tXS.

Command/Address parity entry and exit timings

When entering and exiting Parity mode, users must wait tMRD_PAR before issuing another MRS command, and wait tMOD_PAR before any other commands.

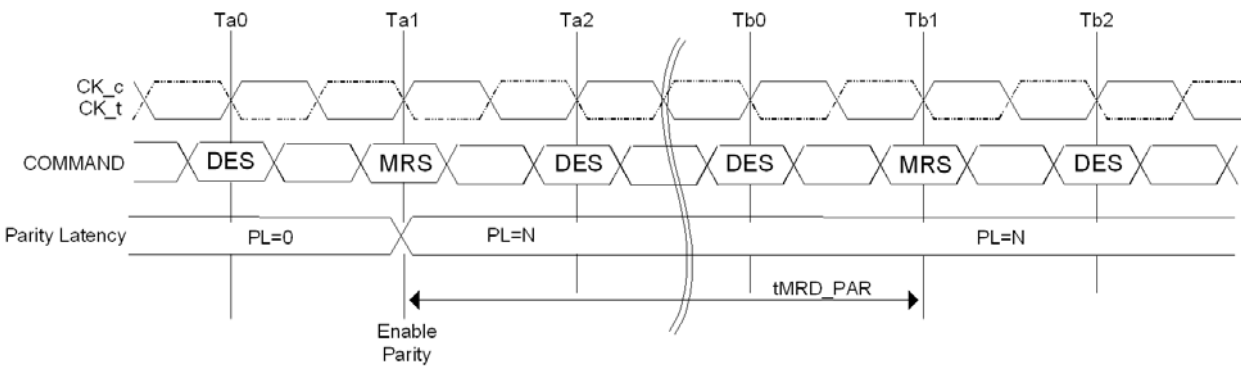
tMOD_PAR = tMOD + PL

tMRD_PAR = tMOD + PL

For CA parity entry, PL in the equations above is the parity latency programmed with the MRS command entering CA parity mode.

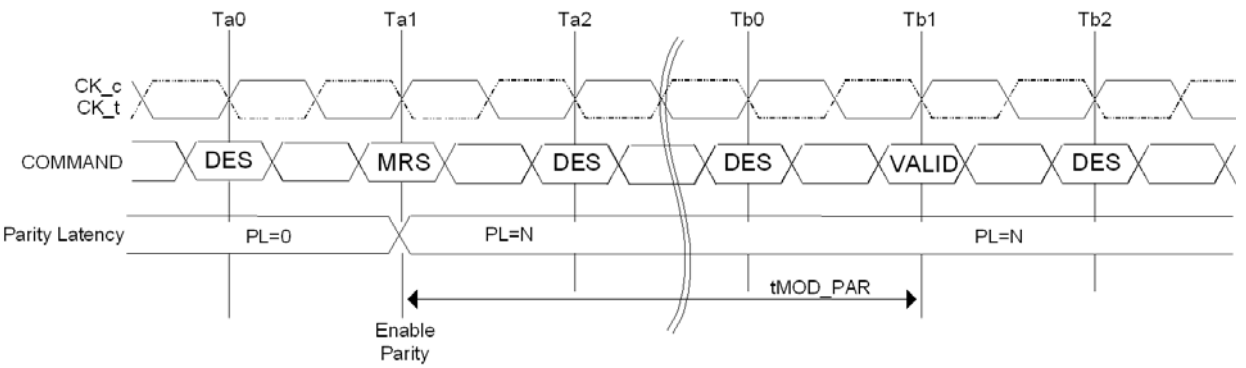
For CA parity exit, PL in the equations above is the programmed parity latency prior to the MRS command exiting CA parity mode.

Parity entry timing example - tMRD_PAR



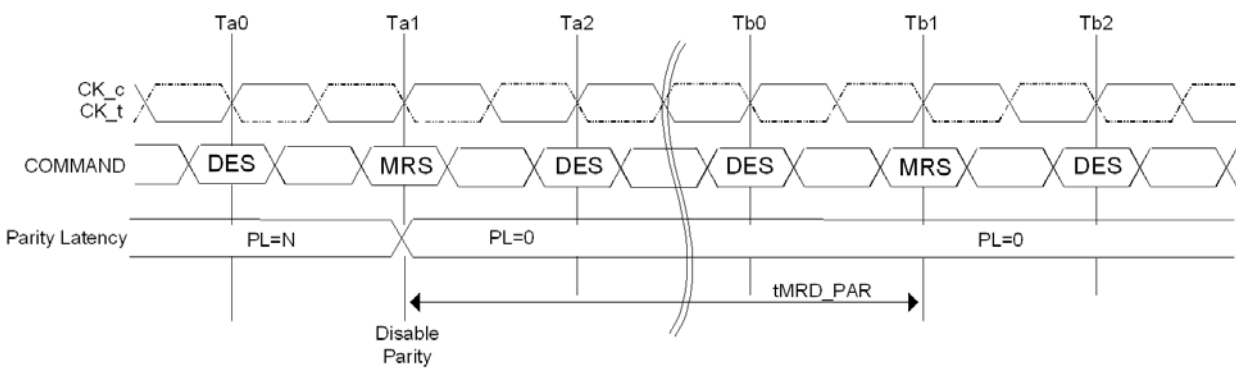
NOTE 1 tMRD_PAR = tMOD + N; where N is the programmed parity latency.

Parity entry timing example - tMOD_PAR



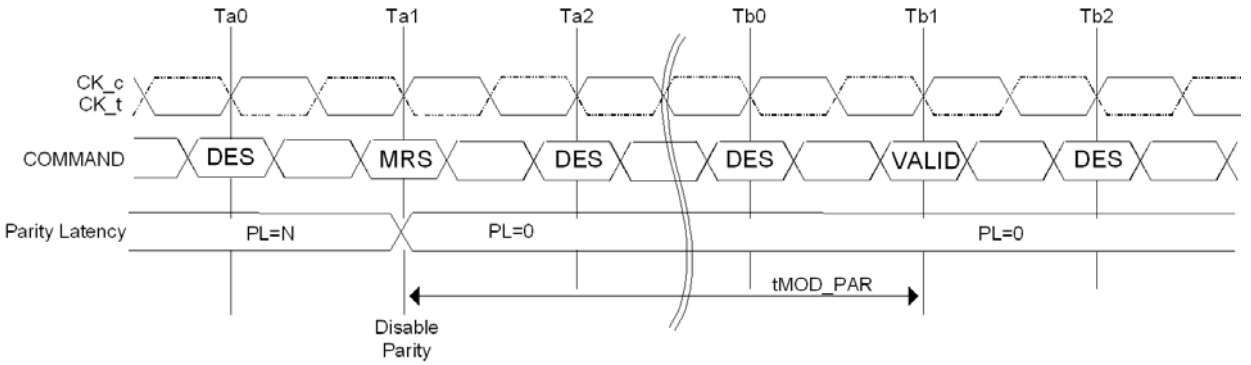
NOTE 1 tMOD_PAR = tMOD + N; where N is the programmed parity latency.

Parity exit timing example - tMRD_PAR



NOTE 1 tMRD_PAR = tMOD + N; where N is the programmed parity latency.

Parity exit timing example - tMOD_PAR



NOTE 1 tMOD_PAR = tMOD + N; where N is the programmed parity latency.

CA Parity Error Log Readout

MPR Mapping of CA Parity Error Log[1](Page1)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BA1:BA0 = 0:1	00=MPR0	A7	A6	A5	A4	A3	A2	A1	A0
	01=MPR1	$\overline{\text{CAS}}$/A15	$\overline{\text{WE}}$/A14	A13	A12	A11	A10	A9	A8
	10=MPR2	PAR	$\overline{\text{ACT}}$	BG1	BG0	BA1	BA0	A17	$\overline{\text{RAS}}$/A16
	11=MPR3	CRC Error Status	CA Parity Error Status	CA Parity Latency			C2	C1	C0

NOTE 1 MPR used for CA parity error log readout is enabled by setting A[2] in MR3

NOTE 2 For higher density of DRAM, where A[17] is not used, MPR2[1] should be treated as don't care.

NOTE 3 If a device is used in monolithic application, where C[2:0] are not used, then MPR3[2:0] should be treated as don't care.

Per DRAM Addressability

DDR4 allows programmability of a given device on a rank. As an example, this feature can be used to program different ODT or Vref values on DRAM devices on a given rank.

1. Before entering 'per DRAM addressability (PDA)' mode, the write leveling is required.

2. Before entering 'per DRAM addressability (PDA)' mode, the following Mode Register setting is possible.

- RTT_PARK MR5 {A8:A6} = Enable

- RTT_NOM MR1 {A10:A9:A8} = Enable

3. Enable 'per DRAM addressability (PDA)' mode using MR3 bit "A4=1".

4. In the 'per DRAM addressability' mode, all MRS command is qualified with DQ0. DRAM captures DQ0 by using $\overline{DQS}$ and $\overline{DQS}$ signals. If the value on DQ0 is 0 then the DRAM executes the MRS command. If the value on DQ0 is 1, then-the DRAM ignores the MRS command. The controller can choose to drive all the DQ bits.

5. Program the desired devices and mode registers using MRS command and DQ0.

6. In the 'per DRAM addressability' mode, only MRS commands are allowed.

7. The mode register set command cycle time at PDA mode, AL + CWL + 3.5nCK + tMRD_PDA is required to complete the write operation to the mode register and is the minimum time required between two MRS commands.

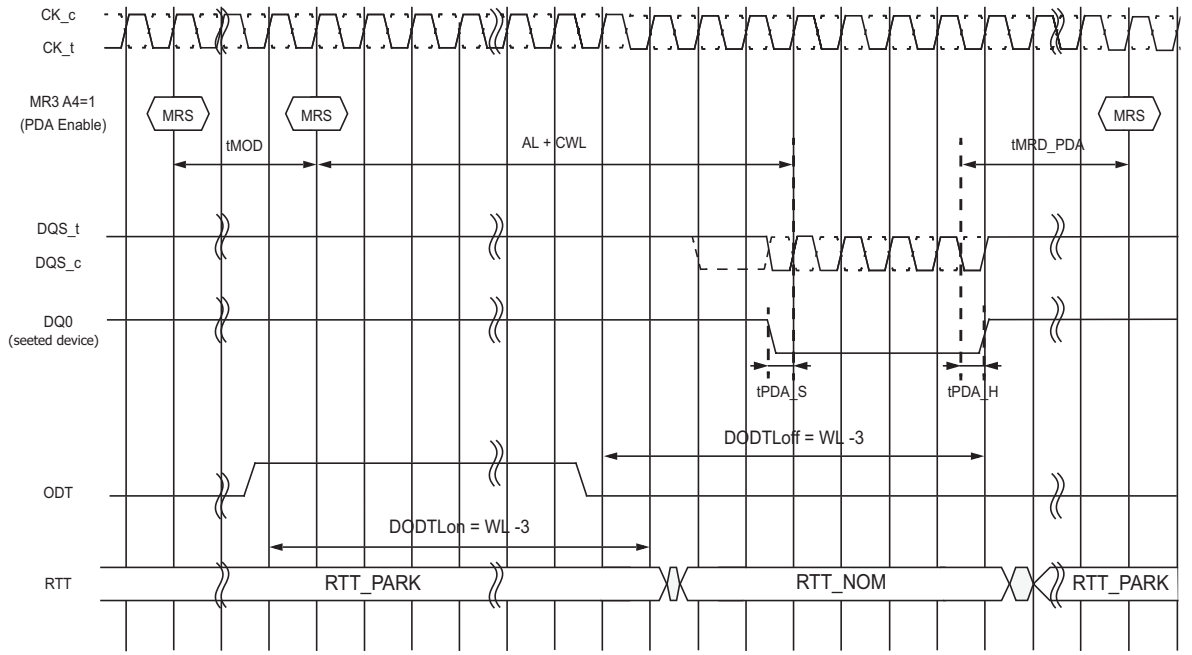
8. Remove the DRAM from 'per DRAM addressability' mode by setting MR3 bit "A4=0". (This command will require DQ0=0.)

Note: Removing a DRAM from per DRAM addressability mode will require programming the entire MR3 when the MRS commandis issued. This may impact some per DRAM values programmed within a rank as the exit command is sent to the rank. In order to avoid such a case the PDA Enable/Disable Control bit is located in a mode register that does not have any 'per DRAM addressability' mode controls. In per DRAM addressability mode, DRAM captures DQ0 using DQS and $\overline{DQS}$ like normal write operation. However, Dynamic ODT is not supported. So extra care required for the ODT setting. If RTT_NOM MR1 {A10:A9:A8} =Enable, DDR4 SDRAM data termination need to be controlled by ODT pin and apply the same timing parameters as defined in Direct ODT function that shown in below.

Applied ODT Timing Parameter to PDA Mode

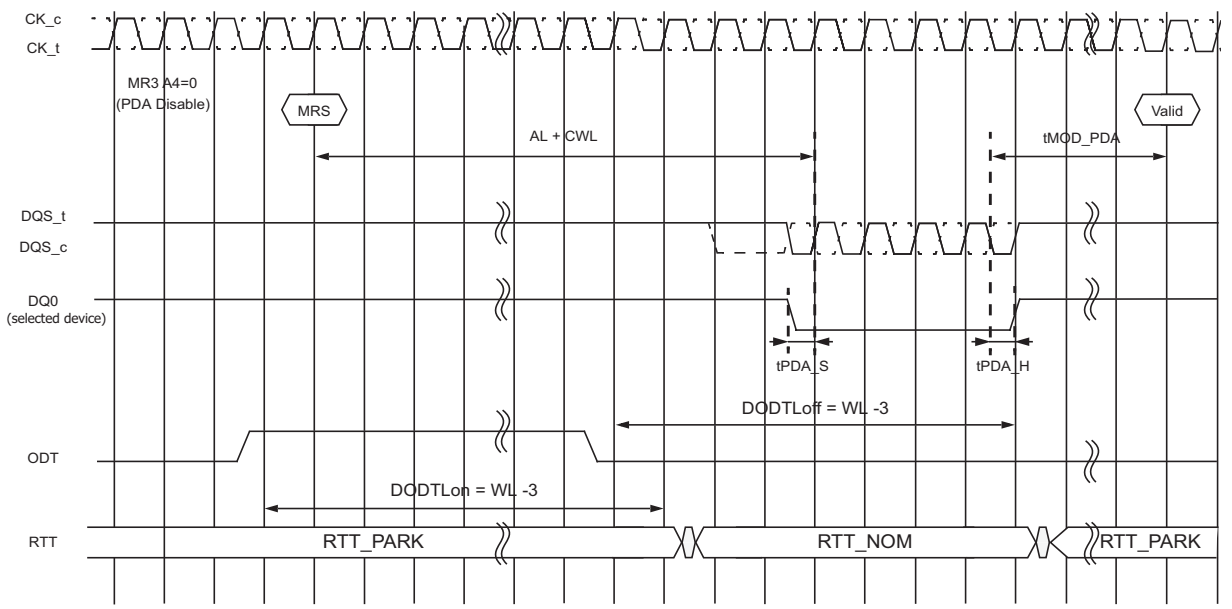
Symbol	Parameter
DODTLon	Direct ODT turn on latency
DODTLoff	Direct ODT turn off latency
tADC	RTT change timing skew
tAONAS	Asynchronous RTT_NOM turn-on delay
tAOFAS	Asynchronous RTT_NOM turn-off delay

MRS w/ per DRAM addressability (PDA) issuing before MRS



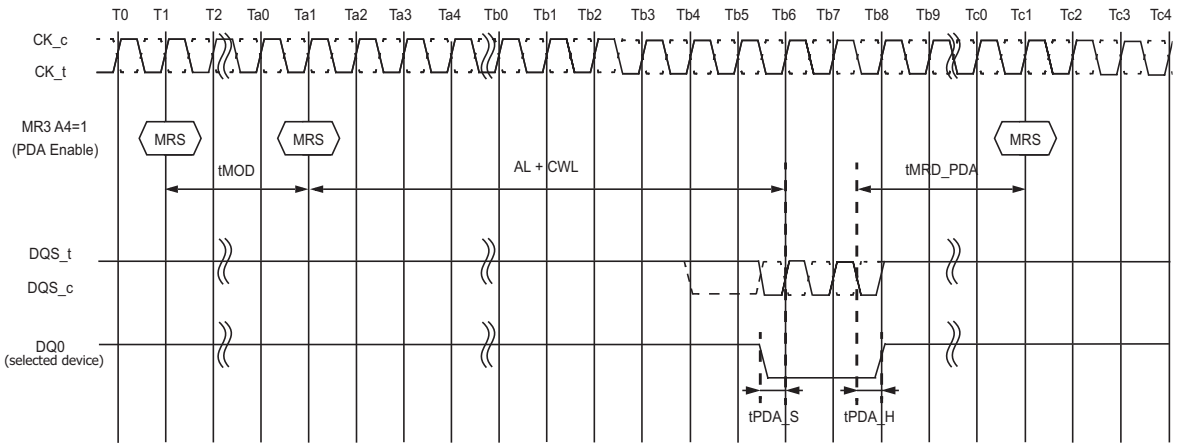
NOTE RTT_PARK = Enable, RTT_NOM = Enable, Write Preamble Set = 2tCK and DLL = ON.

MRS w/ per DRAM addressability (PDA) Exit



NOTE RTT_PARK = Enable, RTT_NOM = Enable, Write Preamble Set = 2tCK and DLL = ON.

PDA using Burst Chop 4



tPDA_S = tDS and tPDA_H = tDH for all DDR4 speed bins.

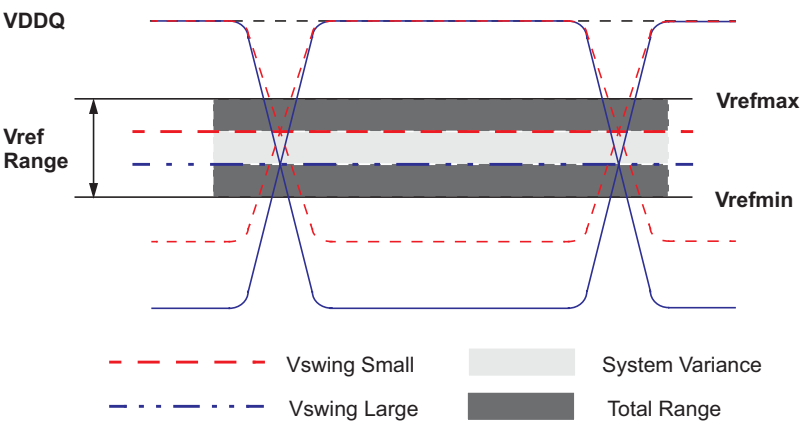
Since PDA mode may be used to program optimal Vref for the DRAM, the DRAM may incorrectly read DQ level at the first DQS edge and the last falling DQS edge. It is recommended that DRAM samples DQ0 on either the first falling or second rising DQS edges. This will enable a common implementation between BC4 and BL8 modes on the DRAM. Controller is required to drive DQ0 to a 'Stable Low or High' during the length of the data transfer for BC4 and BL8 cases.

DQ Vref Training

The DRAM internal DQ Vref specification parameters are operating voltage range, stepsize, Vref step time, Vref full step time and Vref valid level.

The voltage operating range specifies the minimum required Vref setting range for DDR4 DRAM devices. The minimum range isdefined by Vrefmax and Vrefmin as depicted in figure below.

Vref operating range(Vrefmin, Vrefmax)

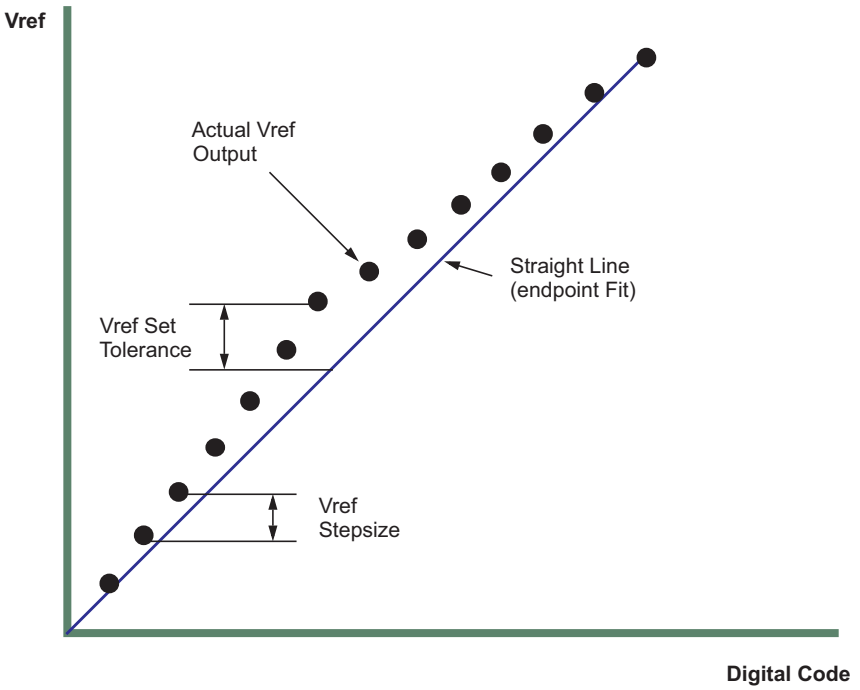


The Vref stepsize is defined as the stepsize between adjacent steps. Vref stepsize ranges from 0.5% VDDQ to 0.8% VDDQ.However, for a given design, DRAM has one value for Vref step size that falls within the range.

The Vref set tolerance is the variation in the Vref voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for Vref set tolerance uncertainty. The range of Vref set tolerance uncertainty is a function of number of steps n.

The Vref set tolerance is measured with respect to the ideal line which is based on the two endpoints. Where the end-points are at themin and max Vref values for a specified range. An illustration depicting an example of the stepsize and Vref set tolerance is below.

Example of Vref set tolerance (max case only shown) and stepsize



The Vref increment/decrement step times are define by Vref_time-short and long. The Vref_time-short and long is defined from t0 to t1, where t1 is referenced to when the vref voltage is at the final DC level within the Vref valid tolerance (Vref_val_tol).

The Vref valid level is defined by Vref_val tolerance to qualify the step time t1. This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any Vref increment/decrement adjustment. This parameter is only applicable for DRAM component level validation/characterization.

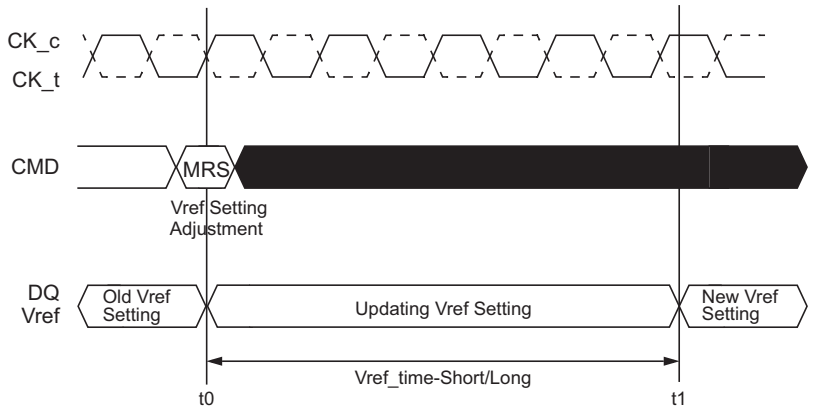
Vref_time-Short is for a single stepsize increment/decrement change in Vref voltage.

Vref_time-Long is the time including up to Vrefmin to Vrefmax or Vrefmax to Vrefmin change in Vref voltage.

t0 - is referenced to MRS command clock

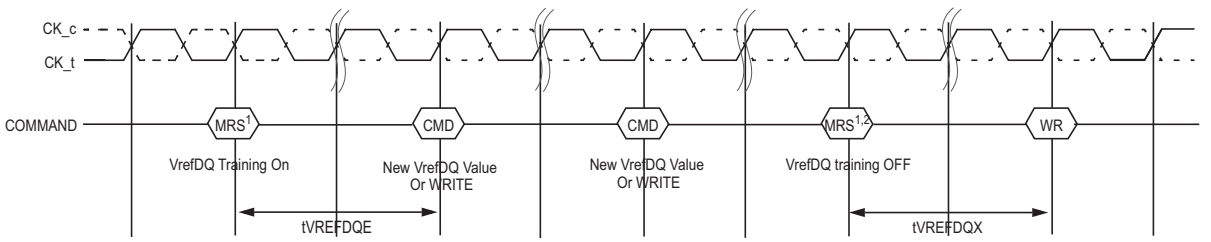
t1 - is referenced to the Vref_val_tol

Vref_time for short and long timing diagram



A MRS command to the mode register bits 5:0 of MR6 are used to program the vref value. VrefDQ training mode is enabled/disabledby A7 of MR6 and training range can be selected by A6 of MR6. When VrefDQ training mode is entered/exited, the following parameter needs to be satisfied to prevent current consumption and also stable operation.

VrefDQ training mode entry and exit timing diagram



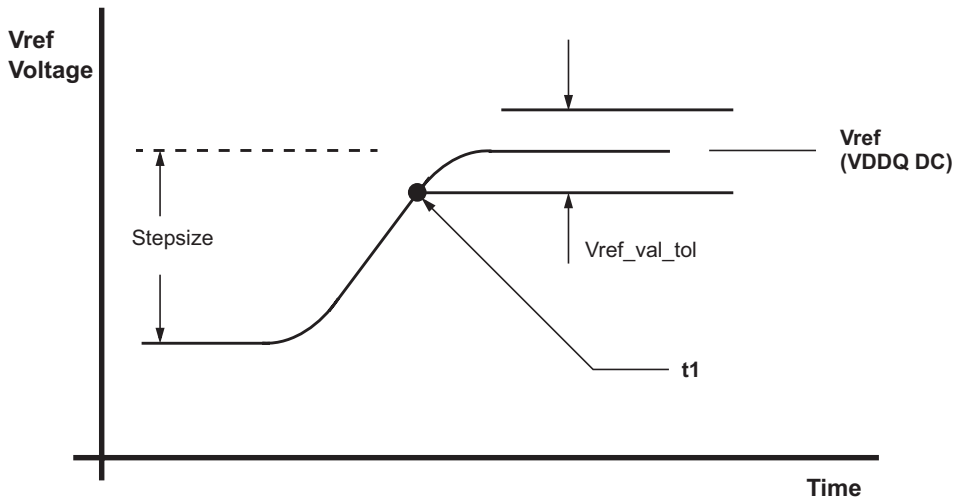
NOTE 1 New VrefDQ value is not allowed with MRS commands for training mode exit.

NOTE 2 Depending on the step size of the latest programmed VREF value, Vref_time_short or Vref_time_long must be satisfied before disabling VrefDQ training mode.

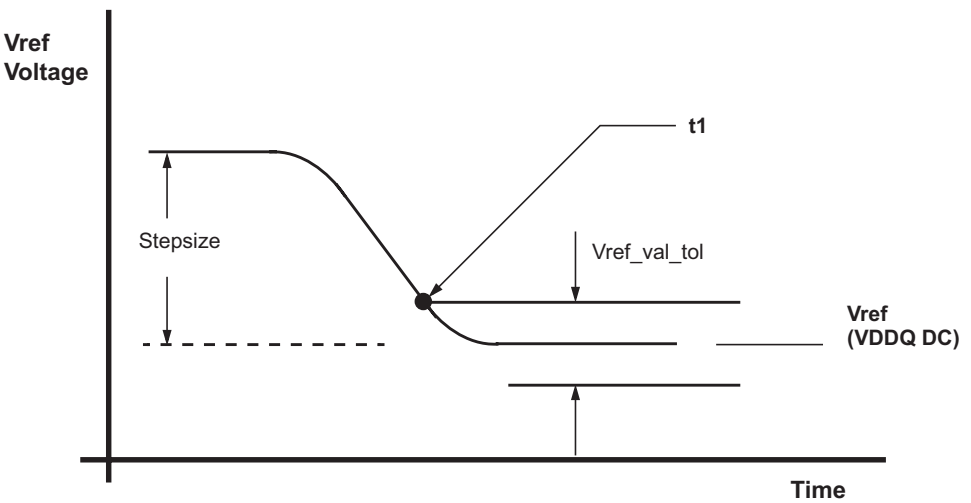
AC parameters of DDR4 VrefDQ training

Speed		DDR4-1600,1866,2133,2400,2666,3200		Unit	NOTE
Parameter	Symbol	MIN	MAX		
VrefDQ training					
Enter VrefDQ training mode to the first write or VREFDQ MRS command delay	tVREFDQE	150	-	ns	
Exit VrefDQ training mode to the first write command delay	tVREFDQX	150	-	ns	

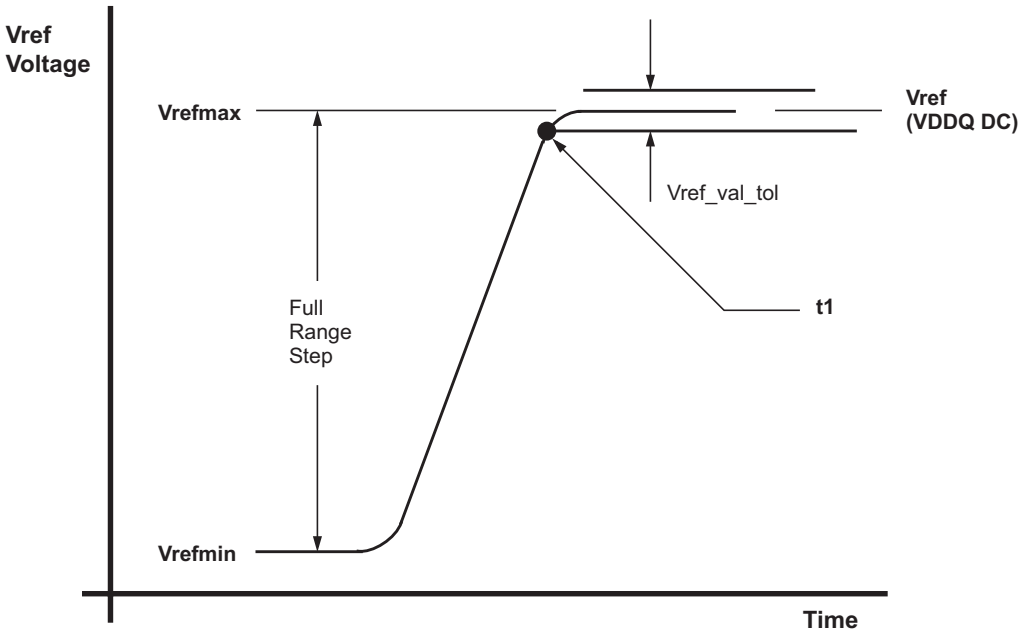
Vref step single stepsize increment case



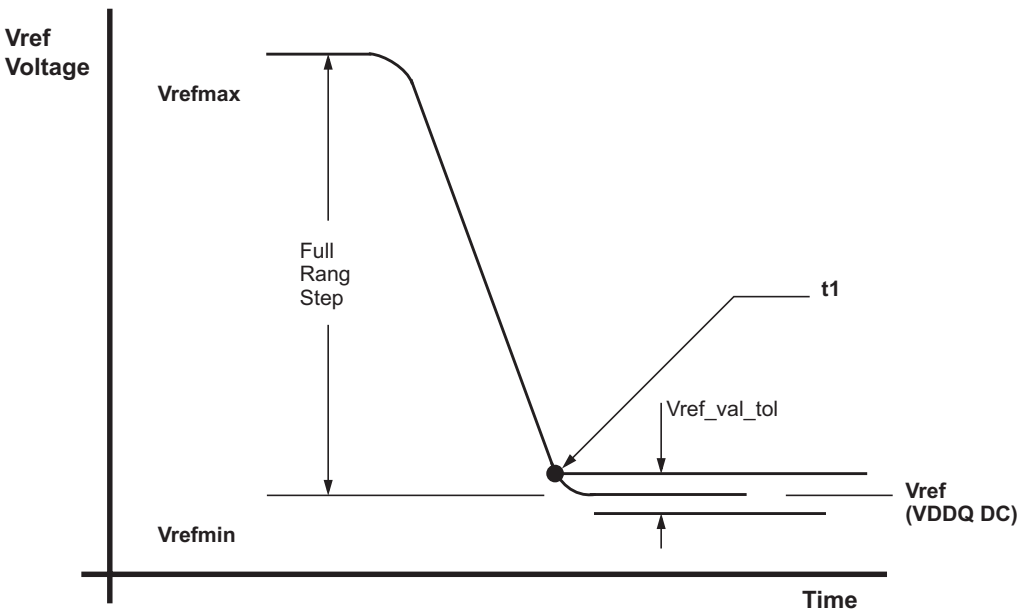
Vref step single stepsize decrement case



Vref full step from Vrefmin to Vrefmax case



Vref full step from Vrefmax to Vrefmin case



DQ Internal Vref Specifications

Prarmeter	Symbol	Min	Typ	Max	Unit	NOTE
Vref Max operating point Range1	Vref_max_R1	60%	-	92%	VDDQ	1,11
Vref Max operating point Range2	Vref_max_R2	45%	-	77%	VDDQ	1,11
Vref Stepsize	Vref step	0.50%	0.65%	0.80%	VDDQ	2
Vref Set Tolerance	Vref_set_tol	-1.625%	0.00%	1.625%	VDDQ	3,4,6
		-0.15%	0.00%	0.15%	VDDQ	3,4,7
Vref Step Time	Vref_time-Short	-	-	60	ns	8,12
	Vref_time-Long	-	-	150	ns	9,12
Vref Valid tolerance	Vref_val_tol	-0.15%	0.00%	0.15%	VDDQ	10

NOTE 1 Vref DC voltage referenced to VDDQ_DC. VDDQ_DC is 1.2V

NOTE 2 Vref stepsize increment/decrement range. Vref at DC level.

NOTE 3 Vref_new = Vref_old+n*Vref_step; n=number of step; if increment use “+”; If decrement use “-”

NOTE 4 The minimum value of Vref setting tolerance=Vref_new-1.625%*VDDQ. The maximum value of Vref setting tolerance=Vref_new+1.625%*VDDQ. For n>4

NOTE 5 The minimum value of Vref setting tolerance=Vref_new-0.15%*VDDQ. The maximum value of Vref setting tolerance=Vref_new+0.15%*VDDQ. For n<=4

NOTE 6 Measured by recording the min and max values of the Vref output over the range, drawing a straight line between those points and comparing all other Vref output settings to that line

NOTE 7 Measured by recording the min and max values of the Vref output across 4 consecutive steps(n=4), drawing a straight line between those points and comparing all other Vref output settings to that line

NOTE 8 Time from MRS command to increment or decrement one step size for Vref

NOTE 9 Time from MRS command to increment or decrement more than one step size up to full range of Vref

NOTE 10 Only applicable for DRAM component level test/characterization purpose. Not applicable for normal mode of operation. Vref valid is to qualify the step times which will be characterized at the component level.

NOTE 11 DRAM range1 or 2 set by MRS bit MR6,A6.

NOTE 12 If the Vref monitor is enabled, Vref_time-long and Vref_time-short must be derated by: +10ns if DQ load is 0pF and an additional +15ns/pF of DQ loading.

Connectivity Test Mode

The DDR4 memory device supports a connectivity test (CT) mode, which is designed to greatly speed up testing of electrical continuity of pin interconnection on the PC boards between the DDR4 memory devices and the memory controller on the SoC. Designed to work seamlessly with any boundary scan devices, the CT mode is required for all x16 width devices independent of density and optional for all x8 and x4 width devices with densities greater than or equal to 8Gb.

Contrary to other conventional shift register based test mode, where test patterns are shifted in and out of the memory devices serially in each clock, DDR4's CT mode allows test patterns to be entered in parallel into the test input pins and the test results extracted in parallel from the test output pins of the DDR4 memory device at the same time, significantly enhancing the speed of the connectivity check. $\overline{\text{RESET}}$ is registered to High and VREFCA must be stable prior to entering CT mode. Once put in the CT mode,the DDR4 memory device effectively appears as an asynchronous device to the external controlling agent; after the input test pattern is applied, the connectivity check test results are available for extraction in parallel at the test output pins after a fixed propagation delay. During CT mode, any ODT is turned off.

A reset of the DDR4 memory device is required after exiting the CT mode.

Pin Mapping

Only digital pins can be tested via the CT mode. For the purpose of connectivity check, all pins that are used for the digital logic in the DDR4 memory device are classified as one of the following types:

1. Test Enable (TEN) pin: when asserted high, this pin causes the DDR4 memory device to enter the CT mode. In this mode, the normal memory function inside the DDR4 memory device is bypassed and the IO pins appear as a set of test input and output pins to the external controlling agent. The TEN pin is dedicated to the connectivity check function and will not be used during normal memory operation.

2. Chip Select ($\overline{\text{CS}}$) pin: when asserted low, this pin enables the test output pins in the DDR4 memory device. When deasserted, the output pins in the DDR4 memory device will be tri-stated. The $\overline{\text{CS}}$ pin in the DDR4 memory device serves as the $\overline{\text{CS}}$ pin when in CT mode.

3. Test Input: a group of pins that are used during normal DDR4 DRAM operation are designated test input pins. These pins are used to enter the test pattern in CT mode.

4. Test Output: a group of pins that are used during normal DDR4 DRAM operation are designated test output pins. These pins are used for extraction of the connectivity test results in CT mode.

5. $\overline{\text{RESET}}$: Fixed high level is required during CT mode same as normal function.

Pin Classification of DDR4 Memory Device in Connectivity Test(CT) Mode

Pin Type in CT Mode	Pin Names during Normal Memory Operation
Test Enable	TEN
Chip Select	CS
Test Input	BA0-1, BG0-1, A0-A9, A10/AP, A11, A12/$\overline{\text{BC}}$, A13, $\overline{\text{WE}}$/A14, $\overline{\text{CAS}}$/A15, $\overline{\text{RAS}}$/A16,$\overline{\text{RESET}}$, CKE, $\overline{\text{ACT}}$, ODT, CLK, $\overline{\text{CLK}}$, $\overline{\text{LDM}}$, $\overline{\text{LDBI}}$, $\overline{\text{UDM}}$, $\overline{\text{UDBI}}$, Parity, $\overline{\text{ALERT}}$
Test Output	DQ0-DQ15, DQSU, $\overline{\text{DQSU}}$, DQSL, $\overline{\text{DQSL}}$

Logic Equations

Min Term Equations

MTx is an internal signal to be used to generate the signal to drive the output signals. x16 and x8 signals are internal signal indicating the density of the device.

MT0 = XOR (A1, A6, PAR)

MT1 = XOR (A8, ALERT, A9)

MT2 = XOR (A2, A5, A15)

MT3 = XOR (A0 A7, A11)

MT4 = XOR ($\overline{CK}$, ODT, $\overline{CAS}$)

MT5 = XOR (CKE, $\overline{RAS}$,/A16, A10/AP)

MT6 = XOR ($\overline{ACT}$, A4, BA1)

MT7 = XOR (((x16 and $\overline{UDM}$ / $\overline{UDBI}$) or (!x16 and BG1)), ((x8 or x16) and $\overline{LDM}$ / $\overline{LDBI}$), CK))

MT8 = XOR ($\overline{WE}$ / A14, A12 / BC, BA0)

MT9 = XOR (BG0, A3, ($\overline{RESET}$ and TEN))

Output equations for x16 devices

DQ0 = MT0

DQ1 = !DQ0

DQ2 = MT1

DQ3 = !DQ2

DQ4 = MT2

DQ5 = !DQ4

DQ6 = MT3

DQ7 = !DQ6

DQ8 = MT4

DQ9 = !DQ8

DQ10 = MT5

DQ11 = ! DQ10

DQ12 = MT6

DQ13 = MT7

DQ14 = MT8

DQ15 = !DQ14

DQSL = MT9

$\overline{DQSL}$ = !DQ12

DQSU = !DQSL

$\overline{DQSU}$ = !DQ13

Output equations for x8 devices

DQ0 = MT0

DQ1 = MT1

DQ2 = MT2

DQ3 = MT3

DQ4 = MT4

DQ5 = MT5

DQ6 = MT6

DQ7 = MT7

DQS = MT8

$\overline{DQS}$ = MT9

Output equations for x4 devices

DQ0 = XOR(MT0, MT1)

DQ1 = XOR(MT2, MT3)

DQ2 = XOR(MT4, MT5)

DQ3 = XOR(MT6, MT7)

DQS = MT8

$\overline{DQS}$ = MT9

Timing Requirement

Prior to the assertion of the TEN pin, all voltage supplies must be valid and stable.

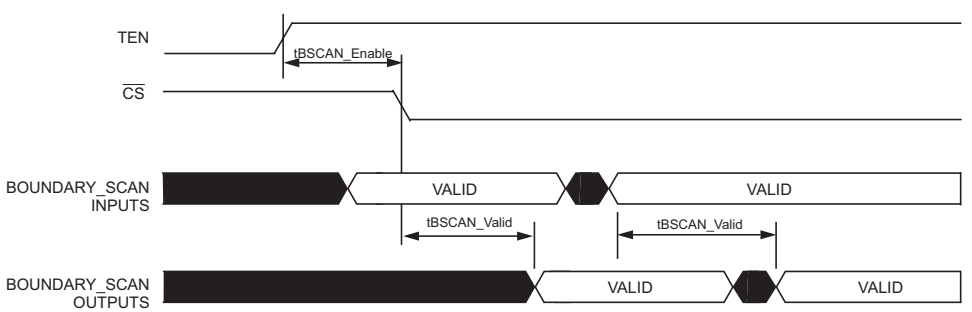
Upon the assertion of the TEN pin, the CK and $\overline{CK}$ signals will be ignored and the DDR4 memory device enter into the CT mode after tBSCAN_Enable. In the CT mode, no refresh activities in the memory arrays, initiated either externally (i.e., auto-refresh) or internally (i.e., self-refresh), will be maintained.

The TEN pin may be asserted at anytime during normal memory operation including when the DDR4 memory device is in low power (or self refreshed) mode. During CT Mode, the signaling of all test input pins is CMOS rail-to-rail with DC high and low at 80% and 20% of VDD.

The TEN pin may be de-asserted at any time in the CT mode. Upon exiting the CT mode, the states of the DDR4 memory device are unknown and the integrity of the original content of the memory array is not guaranteed and therefore the reset initialization sequence is required.

All output signals at the test output pins will be stable within tBSCAN_valid after the test inputs have been applied to the test input pins with TEN input and $\overline{CS}$ input maintained High and Low respectively.

Timing Diagram for Boundary Scan mode



AC parameters for Boundary scan mode

Symbol	Min	Mix	Unit
tBSCAN_Enable	200	-	ns
tBSCAN_Valid	-	200	ns

ACTIVATE Command

The ACTIVATE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BG0-BG1 in X4/8 and BG0 in X16 select the bankgroup; BA0-BA1 inputs selects the bank within the bankgroup, and the address provided on inputs A0-A17 selects the row. This row remains active (or open) for accesses until a precharge command is issued to that bank or a precharge all command is issued. A bank must be precharged before opening a different row in the same bank.

Precharge Command

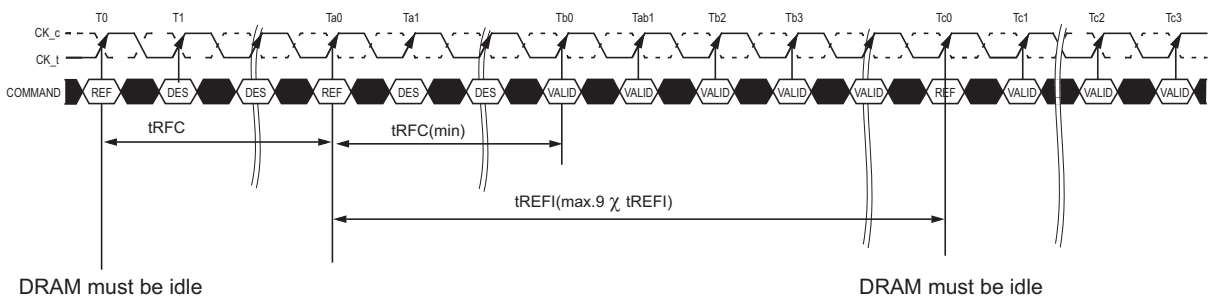
The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row activation a specified time (tRP) after the PRECHARGE command is issued, except in the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command is allowed if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. However, the precharge period will be determined by the last PRECHARGE command issued to the bank.

Refresh Command

The Refresh command (REF) is used during normal operation of the DDR4 SDRAMs. This command is non persistent, so it must be issued each time a refresh is required. The DDR4 SDRAM requires Refresh cycles at an average periodic interval of tREFI. When $\overline{CS}$, $\overline{RAS}$/A16 and $\overline{CAS}$/A15 are held Low and $\overline{WE}$/A14 and $\overline{ACT}$ are held High at the rising edge of the clock, the chip enters a Refresh cycle. All banks of the SDRAM must be precharged and idle for a minimum of the precharge time tRP(min) before the Refresh Command can be applied. The refresh addressing is generated by the internal refresh controller. This makes the address bits “Don’t Care” during a Refresh command. An internal address counter supplies the addresses during the refresh cycle. No control of the external address bus is required once this cycle has started. When the refresh cycle has completed, all banks of the SDRAM will be in the precharged (idle) state. A delay between the Refresh Command and the next valid command, except DES, must be greater than or equal to the minimum Refresh cycle time tRFC(min) as shown in below figure. Note that the tRFC timing parameter depends on memory density.

In general, a Refresh command needs to be issued to the DDR4 SDRAM regularly every tREFI interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided for postponing and pulling-in refresh command. A maximum of 8 Refresh commands can be postponed when DRAM is in 1X refresh mode and for 2X/4X refresh mode, 16/32 Refresh commands can be postponed respectively during operation of the DDR4 SDRAM, meaning that at no point in time more than a total of 8,16,32 Refresh commands are allowed to be postponed for 1X,2X,4X Refresh mode respectively. In case that 8 Refresh commands are postponed in a row, the resulting maximum interval between the surrounding Refresh commands is limited to 9 x tREFI (see the below figure). In 2X and 4X Refresh mode, it’s limited to 17 x tREFI2 and 33 x tREFI4. A maximum of 8 additional Refresh commands can be issued in advance (“pulled in”) in 1X refresh mode and for 2X/4X refresh mode, 16/32 Refresh commands can be pulled in respectively, with each one reducing the number of regular Refresh commands required later by one. Note that pulling in more than 8/16/32, depending on Refresh mode, Refresh commands in advance does not further reduce the number of regular Refresh commands required later, so that the resulting maximum interval between two surrounding Refresh commands is limited to 9 x tREFI , 17 x tRFEI2 and 33 x tREFI4 respectively. At any given time, a maximum of 16 REF/32REF 2/64REF 4 commands can be issued within 2 x tREFI/ 4 x tREFI2/ 8 x tREFI4

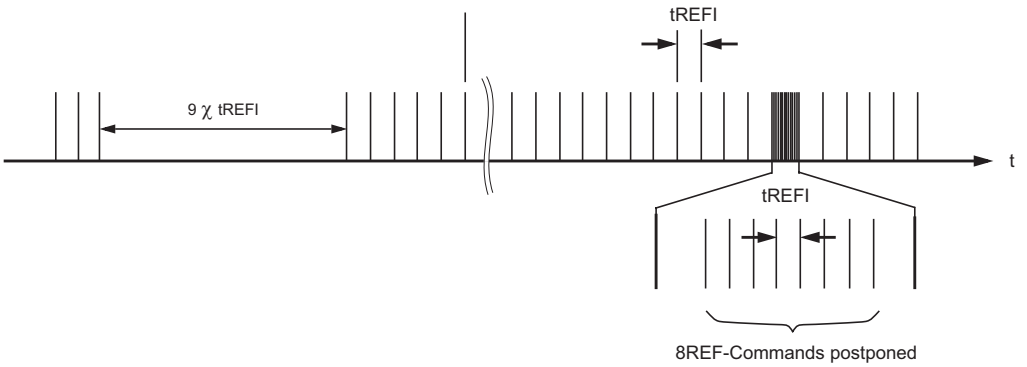
Refresh Command Timing



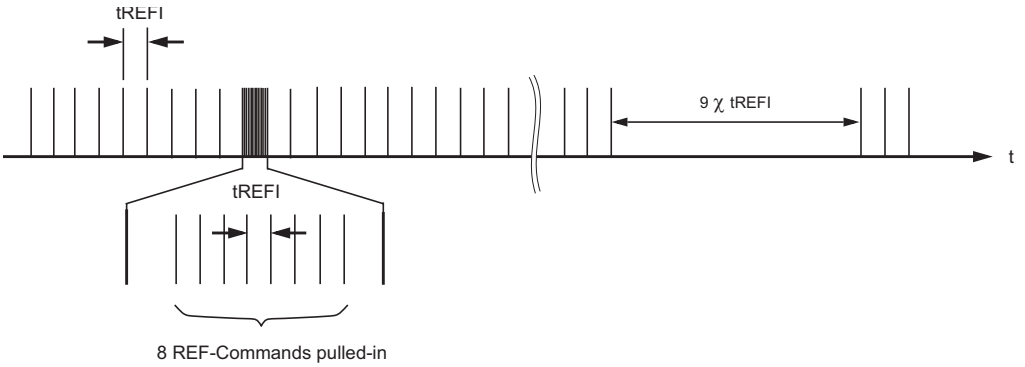
NOTE 1 Only DES commands allowed after Refresh command registered untill tRFC(min) expires.

NOTE 2 Time interval between two Refresh commands may be extended to a maximum of 9 X tREFI.

Postponing Refresh Commands



Pulling-in Refresh Commands



Self refresh Operation

The Self-Refresh command can be used to retain data in the DDR4 SDRAM, even if the rest of the system is powered down. When in the Self-Refresh mode, the DDR4 SDRAM retains data without external clocking.The DDR4 SDRAM device has a built-in timer to accommodate Self-Refresh operation. The Self-Refresh-Entry (SRE) Command is defined by having $\overline{CS}$, $\overline{RAS}$/A16, $\overline{CAS}$/A15, and CKE held low with $\overline{WE}$/A14 and $\overline{ACT}$ high at the rising edge of the clock.

Before issuing the Self-Refresh-Entry command, the DDR4 SDRAM must be idle with all bank precharge state with tRP satisfied. 'Idle state' is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD,tRFC, tZQinit, tZQoper, tZQCS, etc.). Deselect command must be registered on last positive clock edge before issuing Self Refresh Entry command. Once the Self Refresh Entry command is registered, Deselect command must also be registered at the next positive clock edge. Once the Self-Refresh Entry command is registered, CKE must be held low to keep the device in Self-Refresh mode. .DRAM automatically disables ODT termination and set Hi-Z as termination state regardless of ODT pin and RTT_PARK set when it enters in Self-Refresh mode. Upon exiting Self-Refresh, DRAM automatically enables ODT termination and set RTT_PARK asynchronously during tXSDLL when RTT_PARK is enabled. During normal operation (DLL on) the DLL is automatically disabled upon entering Self-Refresh and is automatically enabled (including a DLL-Reset) upon exiting Self-Refresh.

When the DDR4 SDRAM has entered Self-Refresh mode, all of the external control signals, except CKE and $\overline{RESET}$, are "don't care". For proper Self-Refresh operation, all power supply and reference pins (VDD, VDDQ, VSS, VSSQ, VPP, and VREFCA) must be at valid levels. DRAM internal VREFDQ generator circuitry may remain ON or turned OFF depending on DRAM design. If DRAM internal VREFDQ circuitry is turned OFF in self refresh, when DRAM exits from self refresh state, it ensures that VREFDQ generator circuitry is powered up and stable within tXS period. First Write operation or first Write Leveling Activity may not occur earlier than tXS after exit from Self Refresh. The DRAM initiates a minimum of one Refresh command internally within tCKE period once it enters Self-Refresh mode.

The clock is internally disabled during Self-Refresh Operation to save power. The minimum time that the DDR4 SDRAM must remain in Self-Refresh mode is tCKESR. The user may change the external clock frequency or halt the external clock tCKSRE after Self-Refresh entry is registered, however, the clock must be restarted and stable tCKSRX before the device can exit Self-Refresh operation.

The procedure for exiting Self-Refresh requires a sequence of events. First, the clock must be stable prior to CKE going back HIGH. Once a Self-Refresh Exit command (SRX, combination of CKE going high and Deselect on command bus) is registered, following timing delay must be satisfied:

1. Commands that do not require locked DLL:tXS - ACT, PRE, PREA, REF, SRE, PDE, WR, WRS4, WRS8, WRA, WRAS4, WRAS8, tXSFast - ZQCL, ZQCS, MRS commands. For MRS command, only DRAM CL and WR/RTP register in MR0, CWL register in MR2 and geardown mode in MR3 are allowed to be accessed provided DRAM is not in per DRAM addressability mode. Access to other DRAM mode registers must satisfy tXS timing.Note that synchronous ODT for write commands (WR, WRS4, WRS8, WRA, WRAS4 and WRAS8) and dynamic ODT controlled by write command require locked DLL.

2. Commands that require locked DLL:tXSDLL - RD, RDS4, RDS8, RDA, RDAS4, RDAS8

Depending on the system environment and the amount of time spent in Self-Refresh, ZQ calibration commands may be required to compensate for the voltage and temperature drift as described in "ZQ Calibration Commands". To issue ZQ calibration commands, applicable timing requirements must be satisfied.

CKE must remain HIGH for the entire Self-Refresh exit period tXSDLL for proper operation except for Self-Refresh re-entry. Upon exit from Self-Refresh, the DDR4 SDRAM can be put back into Self-Refresh mode or Power down mode after waiting at least tXS period and issuing one refresh command (refresh period of tRFC). Deselect commands must be registered on each positive clock edge during the Self-Refresh exit interval tXS. Low level of ODT pin must be registered on each positive clock edge during tXSDLL when normal mode (DLL-on) is set. Under DLL-off mode, asynchronous ODT function might be allowed.

The use of Self-Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self-Refresh mode. Upon exit from Self-Refresh, the DDR4 SDRAM requires a minimum of one extra refresh command before it is put back into Self-Refresh Mode.

The exit timing from self-refresh exit to first valid command not requiring a locked DLL is tXS.

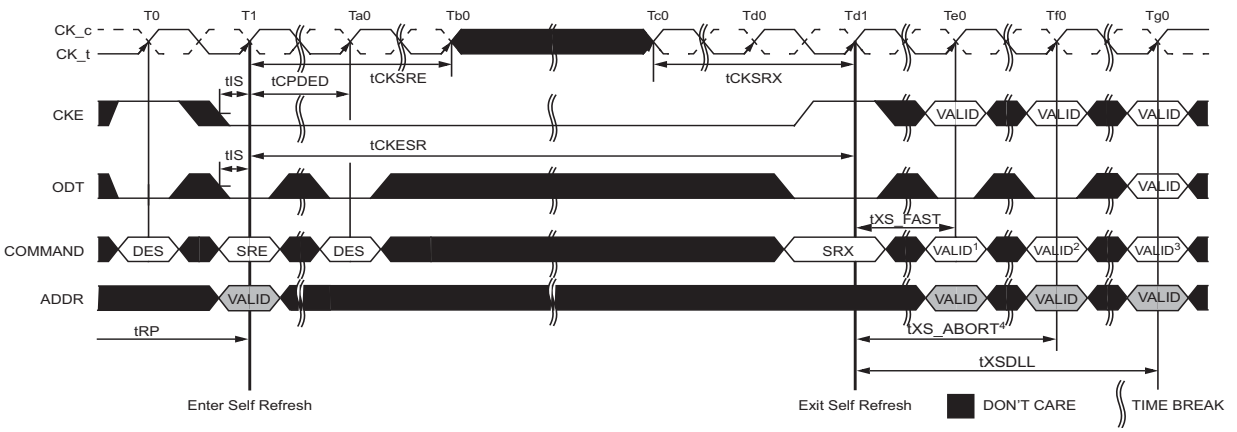
The value of tXS is (tRFC+10ns). This delay is to allow for any refreshes started by the DRAM to complete. tRFC continues to grow with higher density devices so tXS will grow as well.

A Bit A9 in MR4 is defined to enable the self refresh abort mode. If the bit is disabled then the controller uses tXS timings.

If the bit is enabled then the DRAM aborts any ongoing refresh and does not increment the refresh counter. The controller can issue a valid command not requiring a locked DLL after a delay of tXS_abort.

Upon exit from Self-Refresh, the DDR4 SDRAM requires a minimum of one extra refresh command before it is put back into Self-Refresh Mode. This requirement remains the same irrespective of the setting of the MRS bit for self refresh abort.

Self-Refresh Entry/Exit Timing



Low Power Auto Self Refresh

DDR4 devices support Low Power Auto Self-Refresh (LP ASR) operation at multiple temperatures ranges (See temperature tablebelow). Mode Register MR2 - descriptions

MR2 definitions for Low Power Auto Self-Refresh mode

A6	A7	Self-Refresh Operation Mode
0	0	Manual Mode - Normal operating temperature range
0	1	Manual Mode - Extended operating temperature range
1	0	Manual Mode - Lower power mode at a reduced operating temperature range
1	1	ASR Mode - automatically switching between all modes to optimize power for any of the temperature ranges listed above

Auto Self Refresh (ASR)

DDR4 DRAM provides an Auto Self-Refresh mode (ASR) for application ease. ASR mode is enabled by setting the above MR2 bitsA6=1 and A7=1. The DRAM will manage Self Refresh entry through the supported temperature range of the DRAM. In this mode, theDRAM will change self-refresh rate as the DRAM operating temperature changes, lower at low temperatures and higher at hightemperatures.

Manual Mode

If ASR mode is not enabled, the LP ASR Mode Register must be manually programmed to one the three self-refresh operating modes listed above. In this mode, the user has the flexibility to select a fixed self-refresh operating mode at the entry of the self-refresh according to their system memory temperature conditions. The user is responsible to maintain the required memorytemperature condition for the mode selected during the self-refresh operation. The user may change the selected mode after exitingfrom self refresh and before the next self-refresh entry. If the temperature condition is exceeded for the mode selected, there is risk todata retention resulting in loss of data.

Self Refresh Function table

MR2-A6	MR2-A7	LP ASR Mode	Self Refresh Operation	Allowed Operating Temperature Range for Self Refresh Mode(all reference to DRAM Tcase)
0	0	Normal	Fixed normal self-Refresh rate to maintain data retention for the normal operating temperature. User is required to ensure 85'C DRAM Tcasemax is not exceeded to avoid any risk ofdata loss.	(0'C - 85'C)
0	1	Extended Temperature range	Fixed high self-Refresh rate to optimize data retention to support the extended temperature range	(0'C - 95'C)
1	0	Reduced Temperature range	Variable or fixed self-Refresh rate or any other DRAM power consumption reduction control for the reduced temperature range. User is required to ensure 45'C DRAM Tcase max is not exceeded to avoid any risk of data loss .	(0'C - 45'C)
1	1	Auto Self Refresh	ASR Mode Enabled. Self-Refresh power consumption anddata retention are optimized for any given operating temperature conditions	All of the above

Temperature controlled Refresh modes

This mode is enabled and disabled by setting bit A3 in MR4. Two modes are supported that are selected by bit A2 setting in MR4.

Normal temperature mode

Once this mode is enabled by setting bit A3=1 and A2=0 in MR4, Refresh commands should be issued to DDR4 SDRAM with there fresh period equal to or shorter than tREFI of normal temperature range (0’C - 85’C). In this mode, the system guarantees that theDRAM temperature does not exceed 85’C.

Below 45’C, DDR4 SDRAM may adjust internal refresh period to be longer than tREFI of the normal temperature range by skipping external refresh commands with proper gear ratio. The internal refresh period adjustment is automatically done inside the DRAM and user does not need to provide any additional control.

Extended temperature mode

Once this mode is enabled by setting bit A3=1 and A2=1 in MR4, Refresh commands should be issued to DDR4 SDRAM with there fresh period equal to or shorter than tREFI of extended temperature range (85’C - 95’C).

In the normal temperature range (0’C - 85’C), DDR4 SDRAM adjusts its internal refresh period to tREFI of the normal temperature range by skipping external refresh commands with proper gear ratio. Below 45’C, DDR4 SDRAM may further adjust internal refresh period to be longer than tREFI of the normal temperature range. The internal refresh period adjustment is automatically done insidethe DRAM and user does not need to provide any additional control.

Fine Granularity Refresh Mode

Mode Register and Command Truth Table

The Refresh cycle time (tRFC) and the average Refresh interval (tREFI) of DDR4 SDRAM can be programmed by MRS command. The appropriate setting in the mode register will set a single set of Refresh cycle time and average Refresh interval for the DDR4 SDRAM device (fixed mode), or allow the dynamic selection of one of two sets of Refresh cycle time and average Refresh interval for the DDR4 SDRAM device (on-the-fly mode). The on-the-fly mode must be enabled by MRS before any on-the-fly- Refresh command can be issued.

MR3 definition for Fine Granularity Refresh Mode

A8	A7	A6	Fine Granularity Refresh
0	0	0	Normal mode (Fixed 1x)
0	0	1	Fixed 2x
0	1	0	Fixed 4x
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Enable on the fly 2x
1	1	0	Enable on the fly 4x
1	1	1	Reserved

There are two types of on-the-fly modes (1x/2x and 1x/4x modes) that are selectable by programming the appropriate values into the mode register. When either of the two on-the-fly modes is selected (‘A8=1’), DDR4 SDRAM evaluates BG0 bit when a Refresh command is issued, and depending on the status of BG0, it dynamically switches its internal Refresh configuration between 1x and 2x (or 1x and 4x) modes, and executes the corresponding Refresh operation.

Refresh command truth table

Function	CS	ACT	$\overline{\text{RAS}}$/ A15	$\overline{\text{CAS}}$/ A14	$\overline{\text{WE}}$/ A13	BG1	BG0	BA0-1	A10/AP	A0-9, A11-12, A16-20	MR3 Setting
Refresh (Fixed rate)	L	H	L	L	H	V	V	V	V	V	A8 = ‘0’
Refresh (on-the-fly 1x)	L	H	L	L	H	V	L	V	V	V	A8 = ‘1’
Refresh (on-the-fly 2x)	L	H	L	L	H	V	H	V	V	V	A8:A7:A6=’101’
Refresh (on-the-fly 4x)											A8:A7:A6=’110’

tREFI and tRFC parameters

The default Refresh rate mode is fixed 1x mode where Refresh commands should be issued with the normal rate, i.e., tREFI1 = tREFI(base) (for Tcase<=85'C), and the duration of each refresh command is the normal refresh cycle time (tRFC1). In 2x mode (either fixed 2x or on-the-fly 2x mode), Refresh commands should be issued to the DRAM at the double frequency (tREFI2 = tREFI(base)/2) of the normal Refresh rate. In 4x mode, Refresh command rate should be quadrupled (tREFI4 = tREFI(base)/4). Per each mode and command type, tRFC parameter has different values as defined in below table.

The refresh command that should be issued at the normal refresh rate and has the normal refresh cycle duration may be referred to as a REF1x command. The refresh command that should be issued at the double frequency (tREFI2 = tREFI(base)/2) may be referred to as a REF2x command. Finally, the refresh command that should be issued at the quadruple rate (tREFI4 = tREFI(base)/4) may be referred to as a REF4x command.

In the Fixed 1x Refresh rate mode, only REF1x commands are permitted. In the Fixed 2x Refresh rate mode, only REF2x commands are permitted. In the Fixed 4x Refresh rate mode, only REF4x commands are permitted. When the on-the-fly 1x/2x Refresh rate mode is enabled, both REF1x and REF2x commands are permitted. When the on-the-fly 1x/4x Refresh rate mode is enabled, both REF1x and REF4x commands are permitted.

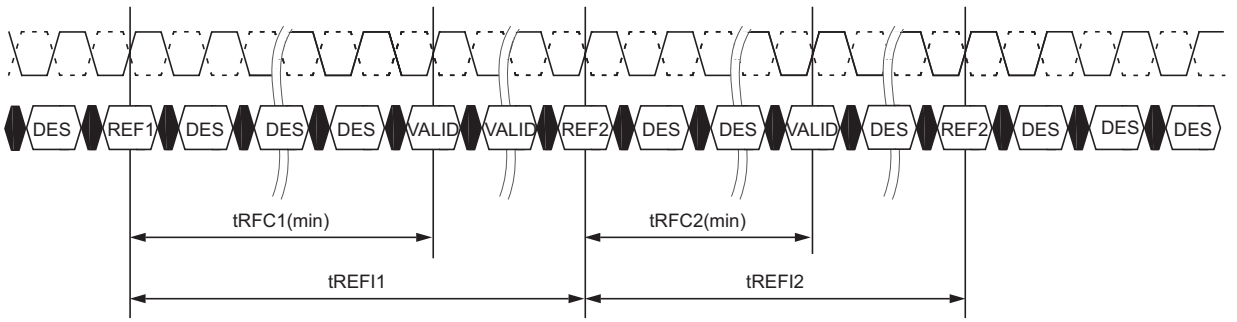
tREFI and tRFC parameters

Refresh Mode	Parameter		2Gb	4Gb	8Gb	16Gb	Unit
	tREFI(base)		7.8	7.8	7.8	TBD	us
1X mode	tREFI1	0'C <= TCASE <= 85'C	tREFI(base)	tREFI(base)	tREFI(base)	tREFI(base)	us
		85'C < TCASE <= 95'C	tREFI(base)/2	tREFI(base)/2	tREFI(base)/2	tREFI(base)/2	us
	tRFC1(min)		160	260	350	TBD	ns
2X mode	tREFI2	0'C <= TCASE <= 85'C	tREFI(base)/2	tREFI(base)/2	tREFI(base)/2	tREFI(base)/2	us
		85'C < TCASE <= 95'C	tREFI(base)/4	tREFI(base)/4	tREFI(base)/4	tREFI(base)/4	us
	tRFC2(min)		110	160	260	TBD	ns
4X mode	tREFI4	0'C <= TCASE <= 85'C	tREFI(base)/4	tREFI(base)/4	tREFI(base)/4	tREFI(base)/4	us
		85'C < TCASE <= 95'C	tREFI(base)/8	tREFI(base)/8	tREFI(base)/8	tREFI(base)/8	us
	tRFC4(min)		90	110	160	TBD	ns

Changing Refresh Rate

If Refresh rate is changed by either MRS or on the fly, new tREFI and tRFC parameters would be applied from the moment of the rate change. As shown in below figure, when REF1x command is issued to the DRAM, then tREF1 and tRFC1 are applied from the time that the command was issued. And then, when REF2x command is issued, then tREF2 and tRFC2 should be satisfied.

On-the-fly Refresh Command Timing



The following conditions must be satisfied before the Refresh rate can be changed. Otherwise, data retention of DDR4 SDRAM cannot be guaranteed.

1. In the fixed 2x Refresh rate mode or the on-the-fly 1x/2x Refresh mode, an even number of REF2x commands must be issued to the DDR4 SDRAM since the last change of the Refresh rate mode with an MRS command before the Refresh rate can be changed by another MRS command.

2. In the on-the-fly 1x/2x Refresh rate mode, an even number of REF2x commands must be issued between any two REF1x commands.

3. In the fixed 4x Refresh rate mode or the on-the-fly 1x/4x Refresh mode, a multiple of-four number of REF4x commands must be issued to the DDR4 SDRAM since the last change of the Refresh rate with an MRS command before the Refresh rate can be changed by another MRS command.

4. In the on-the-fly 1x/4x Refresh rate mode, a multiple-of-four number of REF4x commands must be issued between any two REF1x commands.

There are no special restrictions for the fixed 1x Refresh rate mode. Switching between fixed and on-the-fly modes keeping the samerate is not regarded as a Refresh rate change.

Usage with Temperature Controlled Refresh mode

If the Temperature Controlled Refresh mode is enabled, then only the normal mode (Fixed 1x mode; A8:A7:A6='000') is allowed. If any other Refresh mode than the normal mode is selected, then the temperature controlled Refresh mode must be disabled.

Self Refresh entry and exit

DDR4 SDRAM can enter Self Refresh mode anytime in 1x, 2x and 4x mode without any restriction on the number of Refresh commands that has been issued during the mode before the Self Refresh entry. However, upon Self Refresh exit, extra Refresh command(s) may be required depending on the condition of the Self Refresh entry. The conditions and requirements for the extra Refresh command(s) are defined as follows.

1. There are no special restrictions on the fixed 1x Refresh rate mode.

2. In the fixed 2x Refresh rate mode or the enable-on-the-fly 1x/2x Refresh rate mode, it is recommended that there should be an even number of REF2x commands before entry into Self Refresh since the last Self Refresh exit or REF1x command or MRS command that set the refresh mode. If this condition is met, no additional refresh commands are required upon Self Refresh exit. In the case that this condition is not met, either one extra REF1x command or two extra REF2x commands are required to be issued to the DDR4 SDRAM upon Self Refresh exit. These extra Refresh commands are not counted toward the computation of the average refresh interval (tREFI).

3. In the fixed 4x Refresh rate mode or the enable-on-the-fly 1x/4x Refresh rate mode, it is recommended that there should be a multiple-of-four number of REF4x commands before entry into Self Refresh since the last Self Refresh exit or REF1x command or MRS command that set the refresh mode. If this condition is met, no additional refresh commands are required upon Self Refresh exit. In the case that this condition is not met, either one extra REF1x command or four extra REF4x commands are required to be issued to the DDR4 SDRAM upon Self Refresh exit. These extra Refresh commands are not counted toward the computation of the average refresh interval (tREFI).

Power down Mode

Power-down is synchronously entered when CKE is registered low (along with Deselect command). CKE is not allowed to go low while mode register set command, MPR operations, ZQCAL operations, DLL locking or read / write operation are in progress. CKE is allowed to go low while any of other operations such as row activation, precharge or auto-precharge and refresh are in progress, but power-down IDD spec will not be applied until finishing those operations. Timing diagrams are shown in below figures with details for entry and exit of Power-Down.

The DLL should be in a locked state when power-down is entered for fastest power-down exit timing. If the DLL is not locked during power-down entry, the DLL must be reset after exiting power-down mode for proper read operation and synchronous ODT operation. DRAM design provides all AC and DC timing and voltage specification as well as proper DLL operation with any CKE intensive operations as long as DRAM controller complies with DRAM specifications.

During Power-Down, if all banks are closed after any in-progress commands are completed, the device will be in precharge Power-Down mode; if any bank is open after in-progress commands are completed, the device will be in active Power-Down mode.

Entering power-down deactivates the input and output buffers, excluding CK, $\overline{CK}$, CKE and $\overline{RESET}$. In power-down mode, DRAM ODT input buffer deactivation is based on MR5 bit A5. If it is configured to 0b, ODT input buffer remains on and ODT input signal must be at valid logic level. If it is configured to 1b, ODT input buffer is deactivated and DRAM ODT input signal may be floating and DRAM does not provide Rtt_Nom termination. Note that DRAM continues to provide Rtt_Park termination if it is enabled in DRAM mode register MR5 bit A8:A6 To protect DRAM internal delay on CKE line to block the input signals, multiple Deselect commands are needed during the CKE switch off and cycle(s) after, this timing period are defined as tCPDED. CKE_low will result in deactivation of command and address receivers after tCPDED has expired.

Power-Down Entry Definitions

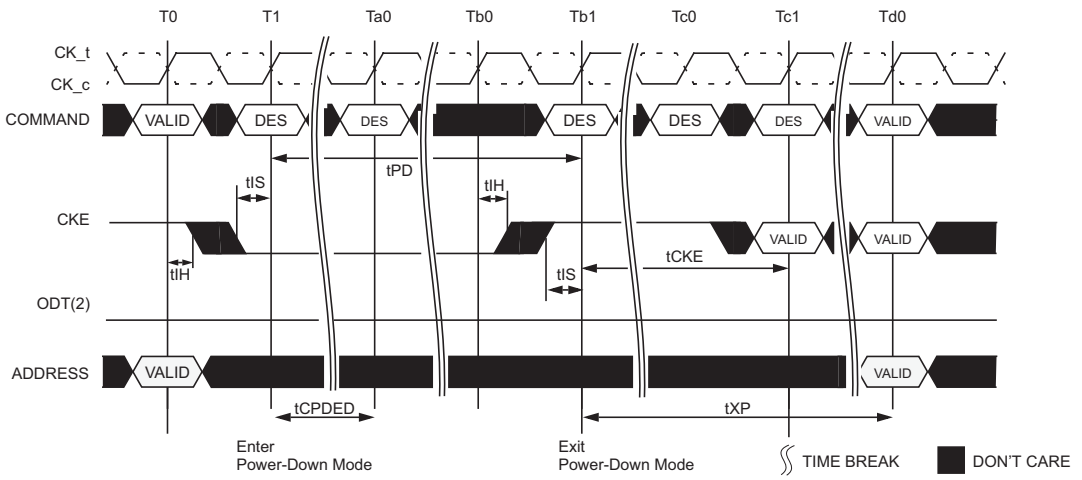
Status of DRAM	DLL	PD Exit	Relevant Parameters
Active (A bank or more Open)	On	Fast	tXP to any valid command
Precharged (All banks Precharged)	On	Fast	tXP to any valid command

Also, the DLL is kept enabled during precharge power-down or active power-down. In power-down mode, CKE low, $\overline{RESET}$ high,and a stable clock signal must be maintained at the inputs of the DDR4 SDRAM, and ODT should be in a valid state, but all other input signals are “Don’t Care.” (If $\overline{RESET}$ goes low during Power-Down, the DRAM will be out of PD mode and into reset state.)CKE low must be maintained until tCKE has been satisfied. Power-down duration is limited by 9 times tREFI of the device.

The power-down state is synchronously exited when CKE is registered high (along with a Deselect command). CKE high must be maintained until tCKE has been satisfied. DRAM ODT input signal must be at valid level when DRAM exits from power-down mode independent of MR5 bit A5 if Rtt_Nom is enabled in DRAM mode register. If DRAM Rtt_Nom is disabled then ODT input signal may remain floating. A valid, executable command can be applied with power-down exit latency, tXP after CKE goes high. Power-down exit latency is defined in the AC specifications Table.

Active Power Down Entry and Exit timing diagram example is shown in below figure. Timing Diagrams for CKE with PD Entry, PD Exit with Read and Read with Auto Precharge, Write, Write with Auto Precharge, Activate, Precharge, Refresh, and MRS are shown in below figures.

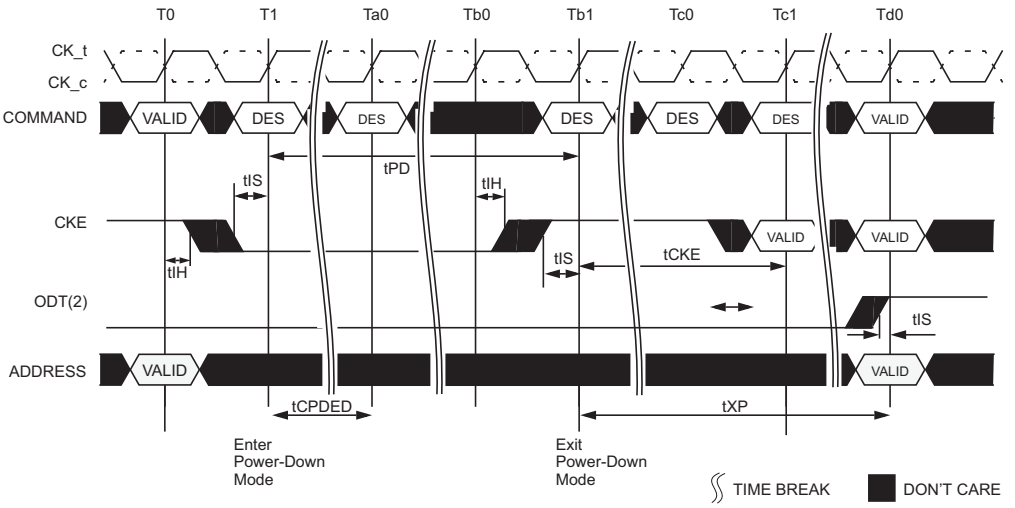
Active Power-Down Entry and Exit Timing Diagram MR5 bit A5 =0



NOTE 1 VALID command at T0 is ACT, DES or Precharge with still one bank remaining open after completion of the pre-charge command.

NOTE 2 ODT pin driven to a valid state. MR5 bit A5=0 (default setting) is shown.

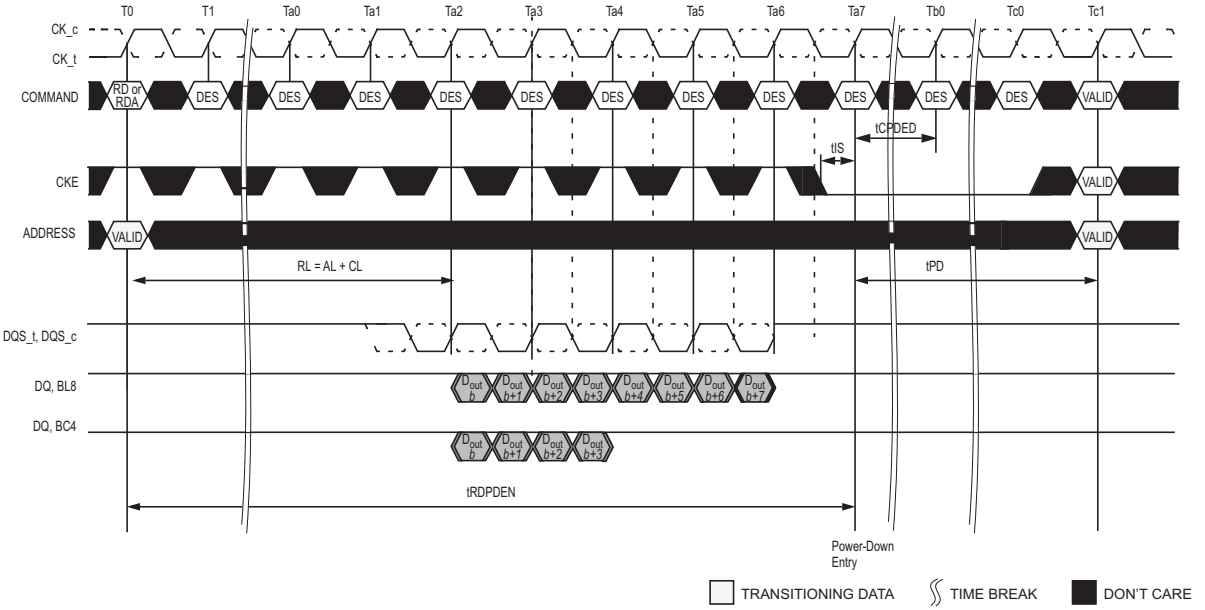
Active Power-Down Entry and Exit Timing Diagram MR5 bit A5 =1



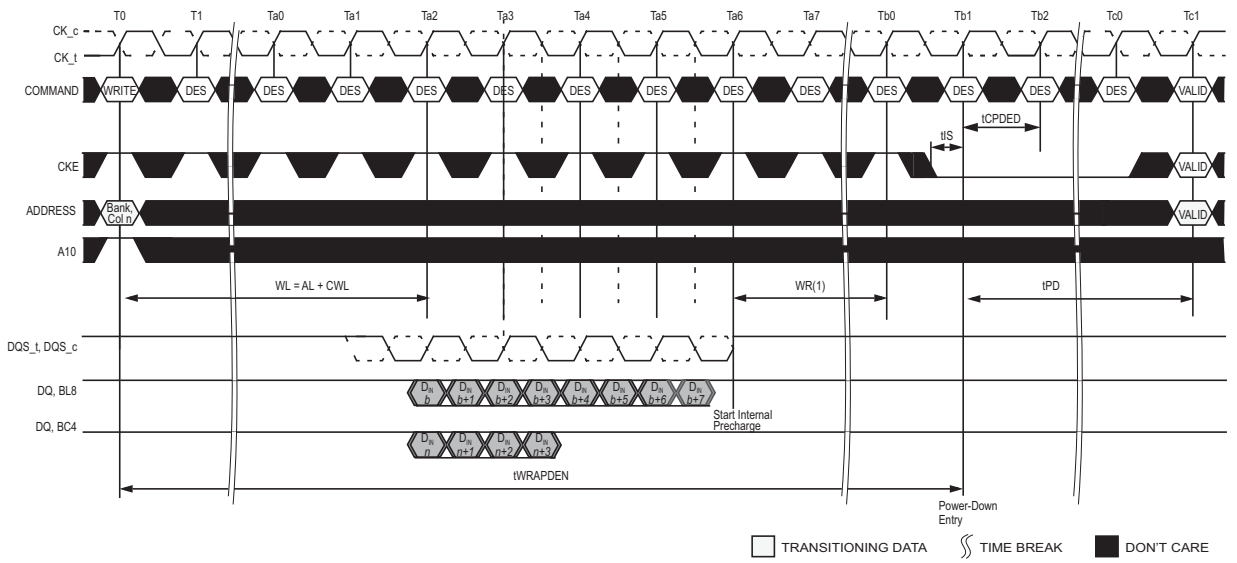
NOTE 1 VALID command at T0 is ACT, DES or Precharge with still one bank remaining open after completion of the pre-charge command.

NOTE 2 ODT pin driven to a valid state. MR5 bit A5=1 is shown.

Power-Down Entry after Read and Read with Auto Precharge

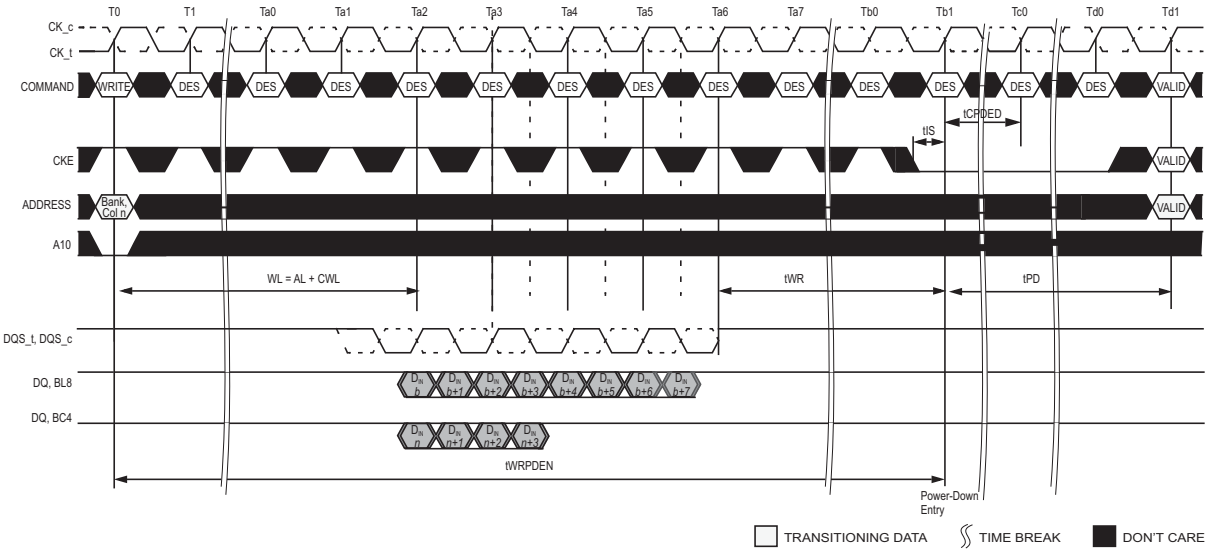


Power-Down Entry After Write with Auto Precharge

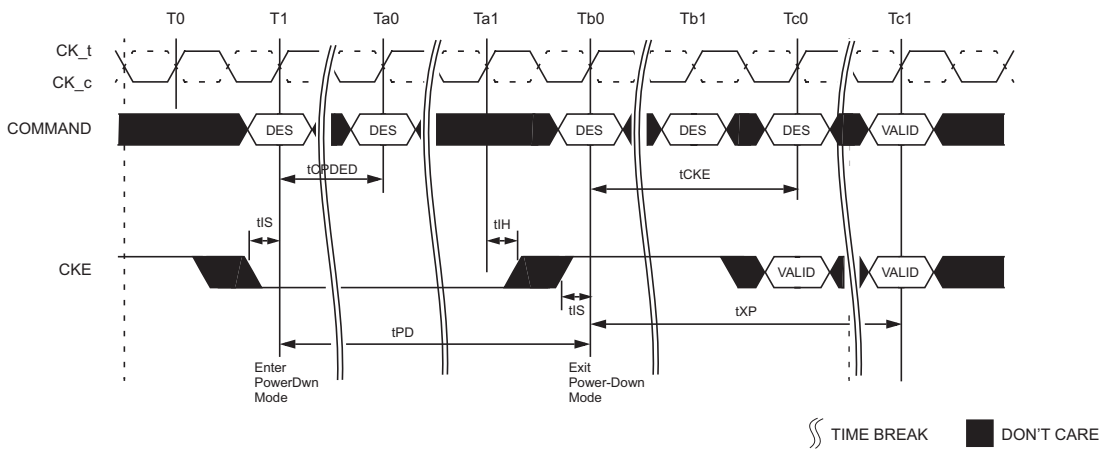


NOTE 1 tWR is programmed through MR0.

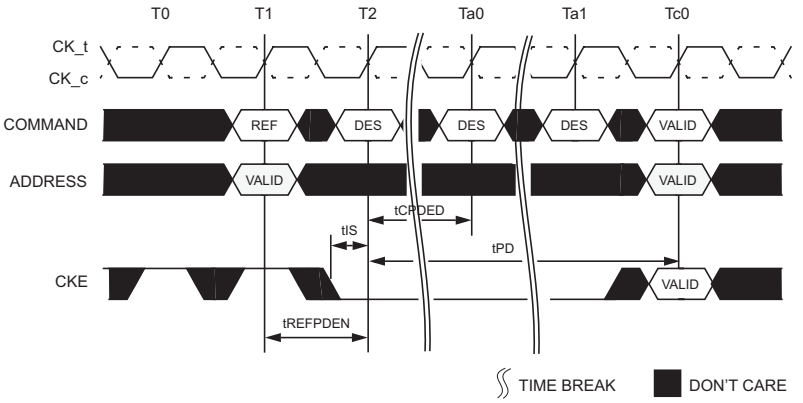
Power-Down Entry after Write



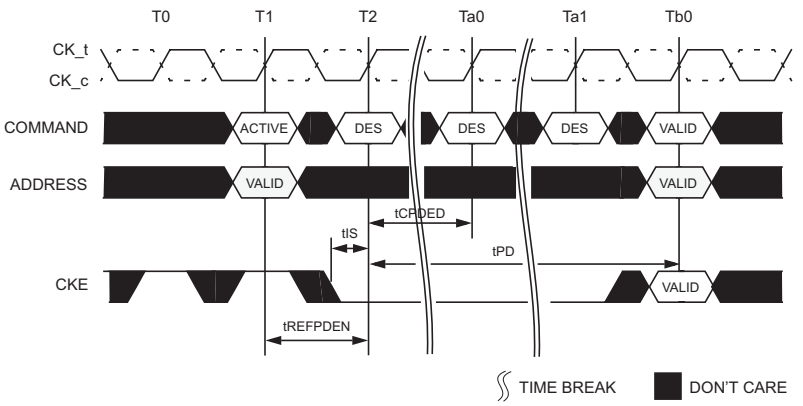
Precharge Power-Down Entry and Exit



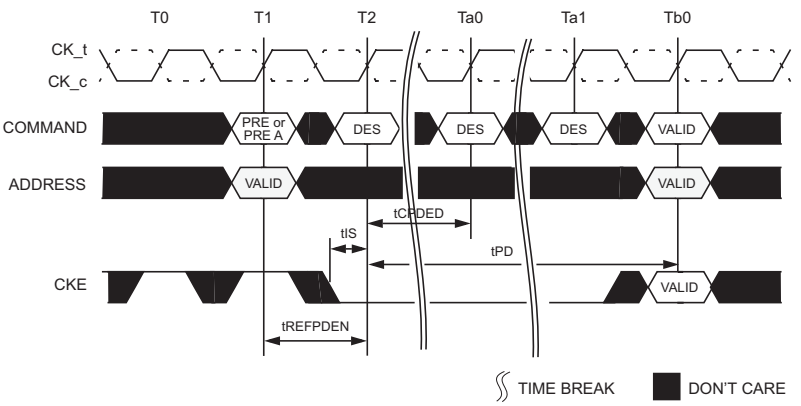
Refresh Command to Power-Down Entry



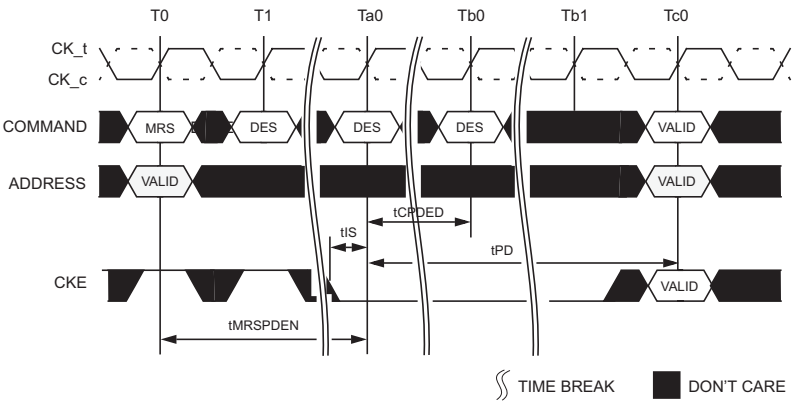
Activate Command to Power-Down Entry



Precharge/Precharge all Command to Power-Down Entry



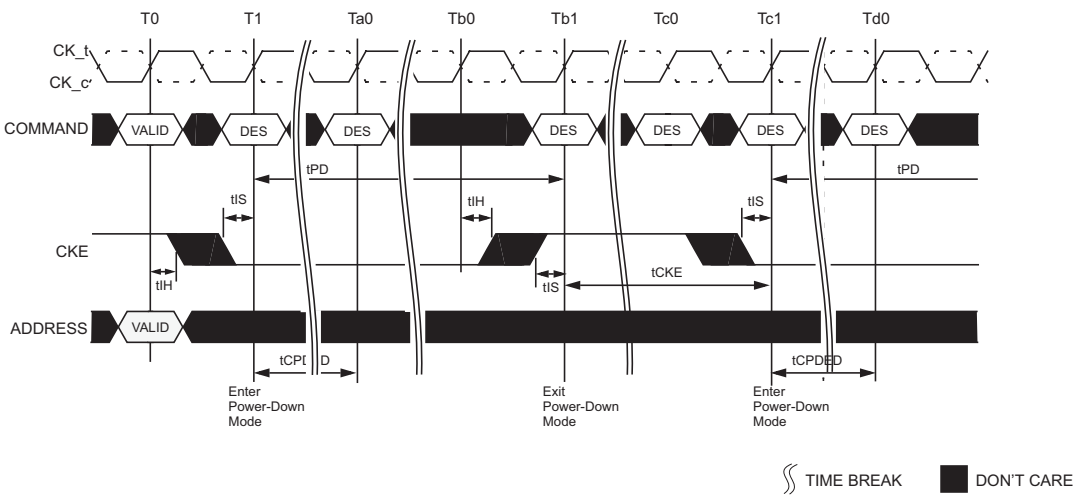
MRS Command to Power-Down Entry



Power-Down clarifications

When CKE is registered low for power-down entry, tPD(min) must be satisfied before CKE can be registered high for power-down exit. The minimum value of parameter tPD(min) is equal to the minimum value of parameter tCKE(min) as shown in Table "Timing Parameters by Speed Bin". A detailed example of Case1 is shown in below figure.

Power-Down Entry/Exit Clarification



CRC

CRC Polynomial and logic equation

DDR4 supports CRC for write operation, and doesn't support CRC for read operation.

The CRC polynomial used by DDR4 is the ATM-8 HEC, X^8+X^2+X^1+1

A combinatorial logic block implementation of this 8-bit CRC for 72-bits of data contains 272 two-input XOR gates contained in eight 6 XOR gate deep trees.

The CRC polynomial and combinatorial logic used by DDR4 is the same as used on GDDR5.

Error Detection Details

ERROR TYPE	DETECTION CAPABILITY
Random Single Bit Error	100%
Random Double Bit Error	100%
Random Odd Count Error	100%
Random one Multi-bit UI vertical column error detection excluding DBI bits	100%

CRC COMBINATORIAL LOGIC EQUATIONS

```
module CRC8_D72;
// polynomial: (0 1 2 8)
// data width: 72
// convention: the first serial data bit is D[71]
// initial condition all 0 implied
function [7:0]
nextCRC8_D72;
input [71:0] Data;
reg [71:0] D;
reg [7:0] NewCRC;
beginD = Data;

NewCRC[0] = D[69] ^ D[68] ^ D[67] ^ D[66] ^ D[64] ^ D[63] ^ D[60] ^D[56] ^ D[54] ^ D[53] ^ D[52] ^ D[50] ^ D[49] ^ D[48] ^D[45] ^ D[43] ^ D[40] ^ D[39] ^ D[35] ^ D[34] ^ D[31] ^D[30] ^ D[28] ^ D[23] ^ D[21] ^ D[19] ^ D[18] ^ D[16] ^D[14] ^ D[12] ^ D[8] ^ D[7] ^ D[6] ^ D[0] ;
NewCRC[1] = D[70] ^ D[66] ^ D[65] ^ D[63] ^ D[61] ^ D[60] ^ D[57] ^D[56] ^ D[55] ^ D[52] ^ D[51] ^ D[48] ^ D[46] ^ D[45] ^D[44] ^ D[43] ^ D[41] ^ D[39] ^ D[36] ^ D[34] ^ D[32] ^D[30] ^ D[29] ^ D[28] ^ D[24] ^ D[23] ^ D[22] ^ D[21] ^D[20] ^ D[18] ^ D[17] ^ D[16] ^ D[15] ^ D[14] ^ D[13] ^D[12] ^ D[9] ^ D[6] ^ D[1] ^ D[0];
NewCRC[2] = D[71] ^ D[69] ^ D[68] ^ D[63] ^ D[62] ^ D[61] ^ D[60] ^D[58] ^ D[57] ^ D[54] ^ D[50] ^ D[48] ^ D[47] ^ D[46] ^D[44] ^ D[43] ^ D[42] ^ D[39] ^ D[37] ^ D[34] ^ D[33] ^D[29] ^ D[28] ^ D[25] ^ D[24] ^ D[22] ^ D[17] ^ D[15] ^D[13] ^ D[12] ^ D[10] ^ D[8] ^ D[6] ^ D[2] ^ D[1] ^ D[0];
NewCRC[3] = D[70] ^ D[69] ^ D[64] ^ D[63] ^ D[62] ^ D[61] ^ D[59] ^D[58] ^ D[55] ^ D[51] ^ D[49] ^ D[48] ^ D[47] ^ D[45] ^D[44] ^ D[43] ^ D[40] ^ D[38] ^ D[35] ^ D[34] ^ D[30] ^D[29] ^ D[26] ^ D[25] ^ D[23] ^ D[18] ^ D[16] ^ D[14] ^D[13] ^ D[11] ^ D[9] ^ D[7] ^ D[3] ^ D[2] ^ D[1];
NewCRC[4] = D[71] ^ D[70] ^ D[65] ^ D[64] ^ D[63] ^ D[62] ^ D[60] ^D[59] ^ D[56] ^ D[52] ^ D[50] ^ D[49] ^ D[48] ^ D[46] ^D[45] ^ D[44] ^ D[41] ^ D[39] ^ D[36] ^ D[35] ^ D[31] ^D[30] ^ D[27] ^ D[26] ^ D[24] ^ D[19] ^ D[17] ^ D[15] ^D[14] ^ D[12] ^ D[10] ^ D[8] ^ D[4] ^ D[3] ^ D[2];
NewCRC[5] = D[71] ^ D[66] ^ D[65] ^ D[64] ^ D[63] ^ D[61] ^ D[60] ^D[57] ^ D[53] ^ D[51] ^ D[50] ^ D[49] ^ D[47] ^ D[46]
```

^D[45] ^ D[42] ^ D[40] ^ D[37] ^ D[36] ^ D[32] ^ D[31] ^D[28] ^ D[27] ^ D[25] ^ D[20] ^ D[18] ^ D[16] ^ D[15] ^D[13] ^ D[11] ^ D[9] ^ D[5] ^ D[4] ^ D[3];

NewCRC[6] = D[67] ^ D[66] ^ D[65] ^ D[64] ^ D[62] ^ D[61] ^ D[58] ^D[54] ^ D[52] ^ D[51] ^ D[50] ^ D[48] ^ D[47] ^ D[46] ^D[43] ^ D[41] ^ D[38] ^ D[37] ^ D[33] ^ D[32] ^ D[29] ^D[28] ^ D[26] ^ D[21] ^ D[19] ^ D[17] ^ D[16] ^ D[14] ^D[12] ^ D[10] ^ D[6] ^ D[5] ^ D[4];

NewCRC[7] = D[68] ^ D[67] ^ D[66] ^ D[65] ^ D[63] ^ D[62] ^ D[59] ^D[55] ^ D[53] ^ D[52] ^ D[51] ^ D[49] ^ D[48] ^ D[47] ^D[44] ^ D[42] ^ D[39] ^ D[38] ^ D[34] ^ D[33] ^ D[30] ^D[29] ^ D[27] ^ D[22] ^ D[20] ^ D[18] ^ D[17] ^ D[15] ^D[13] ^ D[11] ^ D[7] ^ D[6] ^ D[5];

nextCRC8_D72 = NewCRC;

CRC data bit mapping for x4 devices(BL=8)

	0	1	2	3	4	5	6	7	8	9
DQ0	d0	d1	d2	d3	d4	d5	d6	d7	CRC0	CRC4
DQ1	d8	d9	d10	d11	d12	d13	d14	d15	CRC1	CRC5
DQ2	d16	d17	d18	d19	d20	d21	d22	d23	CRC2	CRC6
DQ3	d24	d25	d26	d27	d28	d29	d30	d31	CRC3	CRC7

CRC data bit mapping for x8 devices(BL=8)

	0	1	2	3	4	5	6	7	8	9
DQ0	d0	d1	d2	d3	d4	d5	d6	d7	CRC0	1
DQ1	d8	d9	d10	d11	d12	d13	d14	d15	CRC1	1
DQ2	d16	d17	d18	d19	d20	d21	d22	d23	CRC2	1
DQ3	d24	d25	d26	d27	d28	d29	d30	d31	CRC3	1
DQ4	d32	d33	d34	d35	d36	d37	d38	d39	CRC4	1
DQ5	d40	d41	d42	d43	d44	d45	d46	d47	CRC5	1
DQ6	d48	d49	d50	d51	d52	d53	d54	d55	CRC6	1
DQ7	d56	d57	d58	d59	d60	d61	d62	d63	CRC7	1
$\overline{DM}/\overline{DBI}$	d64	d65	d66	d67	d68	d69	d70	d71	1	1

CRC data bit mapping for x16 devices(BL=8)

A x16 device is treated as two x8 devices. x16 device will have two identical CRC trees implemented. CRC(0-7) covers data bits d(0-71). CRC(8-15) covers data bits d(72-143).

	0	1	2	3	4	5	6	7	8	9
DQ0	d0	d1	d2	d3	d4	d5	d6	d7	CRC0	1
DQ1	d8	d9	d10	d11	d12	d13	d14	d15	CRC1	1
DQ2	d16	d17	d18	d19	d20	d21	d22	d23	CRC2	1
DQ3	d24	d25	d26	d27	d28	d29	d30	d31	CRC3	1
DQ4	d32	d33	d34	d35	d36	d37	d38	d39	CRC4	1
DQ5	d40	d41	d42	d43	d44	d45	d46	d47	CRC5	1
DQ6	d48	d49	d50	d51	d52	d53	d54	d55	CRC6	1
DQ7	d56	d57	d58	d59	d60	d61	d62	d63	CRC7	1
$\overline{\text{LDM}}$/$\overline{\text{LDBI}}$	d64	d65	d66	d67	d68	d69	d70	d71	1	1
DQ8	d72	d73	d74	d75	d76	d77	d78	d79	CRC8	1
DQ9	d80	d81	d82	d83	d84	d85	d86	d87	CRC9	1
DQ10	d88	d89	d90	d91	d92	d93	d94	d95	CRC10	1
DQ11	d96	d97	d98	d99	d100	d101	d102	d103	CRC11	1
DQ12	d104	d105	d106	d107	d108	d109	d110	d111	CRC12	1
DQ13	d112	d113	d114	d115	d116	d117	d118	d119	CRC13	1
DQ14	d120	d121	d122	d123	d124	d125	d126	d127	CRC14	1
DQ15	d128	d129	d130	d131	d132	d133	d134	d135	CRC15	1
$\overline{\text{UDM}}$/$\overline{\text{UDBI}}$	d136	d137	d138	d139	d140	d141	d142	d143	1	1

Write CRC for x4, x8 and x16 devices

The Controller generates the CRC checksum and forms the write data frames.

For a x8 DRAM the controller must send 1's in the transfer 9 if CRC is enabled and must send 1's in transfer 8 and transfer 9 of the $\overline{\text{DBI}}$ lane if DBI function is enabled.

For a x16 DRAM the controller must send 1's in the transfer 9 if CRC is enabled and must send 1's in transfer 8 and transfer 9 of the $\overline{\text{LDBI}}$ and $\overline{\text{UDBI}}$ lanes if DBI function is enabled.

The DRAM checks for an error in a received code word D[71:0] by comparing the received checksum against the computed checksum and reports errors using the $\overline{\text{ALERT}}$ signal if there is a mis-match.

A x8 device has a CRC tree with 72 input bits. The upper 8 bits are used for DBI inputs if DBI is enabled. If DBI is disabled then theinputs of the upper 8 bits D[71:64] are '1's.

A x16 device has two identical CRC trees with 72 input bits each. The upper 8 bits are used for DBI inputs if DBI is enabled. If DBI is disabled then the input of the upper 8 bits [D(143:136) and D(71:64)] is '1'.

A x4 device has a CRC tree with 32 input bits. The input for the upper 40 bits D[71:32] are '1's.

DRAM can write data to the DRAM core without waiting for CRC check for full writes. If bad data is written to the DRAM core then controller will retry the transaction and overwrite the bad data. Controller is responsible for data coherency.

CRC Frame format with BC4

DDR4 SDRAM supports CRC function for Write operation for Burst Chop 4 (BC4). The CRC function is programmable using DRAMmode register and can be enabled for writes.

When CRC is enabled the data frame length is fixed at 10UI for both BL8 and BC4 operations. DDR4 SDRAM also supports burstlength on the fly with CRC enabled. This is enabled using mode register.

CRC data bit mapping for x4 devices(BC4, A2=0)

For a x4 SDRAM, the CRC tree input is 16 data bits. The input for the remaining bits are '1'.

	0	1	2	3	4	5	6	7	8	9
DQ0	d0	d1	d2	d3	1	1	1	1	CRC0	CRC4
DQ1	d8	d9	d10	d11	1	1	1	1	CRC1	CRC5
DQ2	d16	d17	d18	d19	1	1	1	1	CRC2	CRC6
DQ3	d24	d25	d26	d27	1	1	1	1	CRC3	CRC7

CRC data bit mapping for x4 devices(BC4, A2=1)

When A2 = 1, data bits d(4:7) are used as inputs for d(0:3), d(12:15) are used as inputs to d(8:11) and so forth for the CRC tree.

	0	1	2	3	4	5	6	7	8	9
DQ0	d4	d5	d6	d7	1	1	1	1	CRC0	CRC4
DQ1	d12	d13	d14	d15	1	1	1	1	CRC1	CRC5
DQ2	d20	d21	d22	d23	1	1	1	1	CRC2	CRC6
DQ3	d28	d29	d30	d31	1	1	1	1	CRC3	CRC7

CRC data bit mapping for x8 devices(BC4, A2=0)

For a x8 SDRAM, the CRC tree inputs are 36 bits as shown in the figure. The input bits d(64:67) are used if DBI or DMfunctions are enabled. If DBI and DM are disabled then d(64:67) are '1'.

	0	1	2	3	4	5	6	7	8	9
DQ0	d0	d1	d2	d3	1	1	1	1	CRC0	1
DQ1	d8	d9	d10	d11	1	1	1	1	CRC1	1
DQ2	d16	d17	d18	d19	1	1	1	1	CRC2	1
DQ3	d24	d25	d26	d27	1	1	1	1	CRC3	1
DQ4	d32	d33	d34	d35	1	1	1	1	CRC4	1
DQ5	d40	d41	d42	d43	1	1	1	1	CRC5	1
DQ6	d48	d49	d50	d51	1	1	1	1	CRC6	1
DQ7	d56	d57	d58	d59	1	1	1	1	CRC7	1
$\overline{DM}/\overline{DBI}$	d64	d65	d66	d67	1	1	1	1	1	1

CRC data bit mapping for x8 devices(BC4, A2=1)

When A2 = 1, data bits d(4:7) are used as inputs for d(0:3), d(12:15) are used as inputs to d(8:11) and so forth for the CRC tree. The input bits d(68:71) are used if DM or DBI functions are enabled; if DM and DBI are disabled then d(68:71) are 1's.

	0	1	2	3	4	5	6	7	8	9
DQ0	d4	d5	d6	d7	1	1	1	1	CRC0	1
DQ1	d12	d13	d14	d15	1	1	1	1	CRC1	1
DQ2	d20	d21	d22	d23	1	1	1	1	CRC2	1
DQ3	d28	d29	d30	d31	1	1	1	1	CRC3	1
DQ4	d36	d37	d38	d39	1	1	1	1	CRC4	1
DQ5	d44	d45	d46	d47	1	1	1	1	CRC5	1
DQ6	d52	d53	d54	d55	1	1	1	1	CRC6	1
DQ7	d60	d61	d62	d63	1	1	1	1	CRC7	1
$\overline{DM}/\overline{DBI}$	d64	d65	d66	d67	1	1	1	1	1	1

CRC data bit mapping for x16 devices(BC4, A2=0)

For a x16 SDRAM there are two identical CRC trees. The input bits d(64:67) are used if DBI or DM functions are enabled. If DBI and DM are disabled then d(64:67) are ‘1’. The input bits d(136:139) are used if DBI or DM functions areenabled. If DBI and DM are disabled then d(136:139) are ‘1’.

	0	1	2	3	4	5	6	7	8	9
DQ0	d0	d1	d2	d3	1	1	1	1	CRC0	1
DQ1	d8	d9	d10	d11	1	1	1	1	CRC1	1
DQ2	d16	d17	d18	d19	1	1	1	1	CRC2	1
DQ3	d24	d25	d26	d27	1	1	1	1	CRC3	1
DQ4	d32	d33	d34	d35	1	1	1	1	CRC4	1
DQ5	d40	d41	d42	d43	1	1	1	1	CRC5	1
DQ6	d48	d49	d50	d51	1	1	1	1	CRC6	1
DQ7	d56	d57	d58	d59	1	1	1	1	CRC7	1
$\overline{LDM}/\overline{LDBI}$	d64	d65	d66	d67	1	1	1	1	1	1
DQ8	d72	d73	d74	d75	1	1	1	1	CRC8	1
DQ9	d80	d81	d82	d83	1	1	1	1	CRC9	1
DQ10	d88	d89	d90	d91	1	1	1	1	CRC10	1
DQ11	d96	d97	d98	d99	1	1	1	1	CRC11	1
DQ12	d104	d105	d106	d107	1	1	1	1	CRC12	1
DQ13	d112	d113	d114	d115	1	1	1	1	CRC13	1
DQ14	d120	d121	d122	d123	1	1	1	1	CRC14	1
DQ15	d128	d129	d130	d131	1	1	1	1	CRC15	1
$\overline{UDM}/\overline{UDBI}$	d136	d137	d138	d139	1	1	1	1	1	1

CRC data bit mapping for x16 devices(BC4, A2=1)

When A2 = 1, data bits d(4:7) are used as inputs for d(0:3), d(12:15) are used as inputs to d(8:11) and so forth for the CRC tree. Input bits d(68:71) are used if DM or DBI functions are enabled and if DM and DBI are disabled then d(68:71) are 1; input bits d(140:143) are used if DM or DBI functions are enabled and if DM and DBI are disabled, then d(140:143) are 1's.

	0	1	2	3	4	5	6	7	8	9
DQ0	d4	d5	d6	d7	1	1	1	1	CRC0	1
DQ1	d12	d13	d14	d15	1	1	1	1	CRC1	1
DQ2	d20	d21	d22	d23	1	1	1	1	CRC2	1
DQ3	d28	d29	d30	d31	1	1	1	1	CRC3	1
DQ4	d36	d37	d38	d39	1	1	1	1	CRC4	1
DQ5	d44	d45	d46	d47	1	1	1	1	CRC5	1
DQ6	d52	d53	d54	d55	1	1	1	1	CRC6	1
DQ7	d60	d61	d62	d63	1	1	1	1	CRC7	1
$\overline{\text{LDM}}$/$\overline{\text{LDBI}}$	d68	d69	d70	d71	1	1	1	1	1	1
DQ8	d76	d77	d78	d79	1	1	1	1	CRC8	1
DQ9	d84	d85	d86	d87	1	1	1	1	CRC9	1
DQ10	d92	d93	d94	d95	1	1	1	1	CRC10	1
DQ11	d100	d101	d102	d103	1	1	1	1	CRC11	1
DQ12	d108	d109	d110	d111	1	1	1	1	CRC12	1
DQ13	d116	d117	d118	d119	1	1	1	1	CRC13	1
DQ14	d124	d125	d126	d127	1	1	1	1	CRC14	1
DQ15	d132	d133	d134	d135	1	1	1	1	CRC15	1
$\overline{\text{UDM}}$/$\overline{\text{UDBI}}$	d140	d141	d142	d143	1	1	1	1	1	1

CRC equations for x8 device in BC4 mode with A2=0 are as follows:

CRC[0] = D[69]=1 ^ D[68]=1 ^ D[67] ^ D[66] ^ D[64] ^ D[63]=1 ^ D[60]=1 ^ D[56] ^ D[54]=1 ^ D[53]=1 ^ D[52]=1 ^ D[50] ^ D[49] ^D[48] ^ D[45]=1 ^ D[43] ^ D[40] ^ D[39]=1 ^ D[35] ^ D[34] ^ D[31]=1^ D[30]=1 ^ D[28]=1 ^ D[23]=1 ^ D[21]=1 ^ D[19]^ D[18] ^ D[16] ^ D[14]=1 ^ D[12]=1 ^ D[8] ^ D[7]=1 ^ D[6] =1 ^ D[0] ;

CRC[1] = D[70]=1 ^ D[66] ^ D[65] ^ D[63]=1 ^ D[61]=1 ^ D[60]=1 ^ D[57] ^D[56] ^ D[55]=1 ^ D[52]=1 ^ D[51] ^ D[48] ^ D[46]=1 ^D[45]=1 ^ D[44]=1 ^ D[43] ^ D[41] ^ D[39]=1 ^ D[36]=1 ^ D[34] ^ D[32] ^ D[30]=1 ^ D[29]=1 ^ D[28]=1 ^ D[24] ^ D[23]=1^ D[22]=1 ^ D[21]=1 ^ D[20]=1 ^ D[18] ^ D[17] ^ D[16] ^ D[15]=1 ^ D[14]=1 ^ D[13]=1 ^ D[12]=1 ^ D[9] ^ D[6]=1 ^ D[1] ^ D[0];

CRC[2] = D[71]=1 ^ D[69]=1 ^ D[68]=1 ^ D[63]=1 ^ D[62]=1 ^ D[61]=1 ^ D[60]=1 ^ D[58] ^ D[57] ^ D[54]=1 ^ D[50] ^ D[48] ^D[47]=1 ^ D[46]=1 ^ D[44]=1 ^ D[43] ^ D[42] ^ D[39]=1 ^ D[37]=1 ^ D[34] ^ D[33] ^ D[29]=1 ^ D[28]=1 ^ D[25] ^ D[24] ^ D[22]=1 ^ D[17] ^ D[15]=1 ^ D[13]=1 ^ D[12]=1 ^ D[10] ^ D[8] ^ D[6]=1 ^ D[2] ^ D[1] ^ D[0];

CRC[3] = D[70]=1 ^ D[69]=1 ^ D[64] ^ D[63]=1 ^ D[62]=1 ^ D[61]=1 ^ D[59] ^ D[58] ^ D[55]=1 ^ D[51] ^ D[49] ^ D[48] ^ D[47]=1 ^D[45]=1 ^ D[44]=1 ^ D[43] ^ D[40] ^ D[38]=1 ^ D[35] ^ D[34] ^ D[30]=1 ^ D[29]=1 ^ D[26] ^ D[25] ^ D[23]=1 ^ D[18] ^D[16] ^ D[14]=1 ^ D[13]=1 ^ D[11] ^ D[9] ^ D[7]=1 ^ D[3] ^ D[2] ^ D[1];

CRC[4] = D[71]=1 ^ D[70]=1 ^ D[65] ^ D[64] ^ D[63]=1 ^ D[62]=1 ^ D[60]=1 ^ D[59] ^ D[56] ^ D[52]=1 ^ D[50] ^ D[49] ^ D[48] ^D[46]=1 ^ D[45]=1 ^ D[44]=1 ^ D[41] ^ D[39]=1 ^ D[36]=1 ^ D[35] ^ D[31]=1 ^ D[30]=1 ^ D[27] ^ D[26] ^ D[24] ^ D[19] ^ D[17] ^ D[15]=1 ^ D[14]=1 ^ D[12]=1 ^ D[10] ^ D[8] ^ D[4]=1 ^ D[3] ^ D[2];

CRC[5] = D[71]=1 ^ D[66] ^ D[65] ^ D[64] ^ D[63]=1 ^ D[61]=1 ^ D[60]=1 ^ D[57] ^ D[53]=1 ^ D[51] ^ D[50] ^ D[49] ^

D[47]=1 ^D[46]=1 ^ D[45]=1 ^ D[42] ^ D[40] ^ D[37]=1 ^ D[36]=1 ^ D[32] ^ D[31]=1 ^ D[28]=1 ^ D[27] ^ D[25] ^ D[20]=1 ^ D[18]^ D[16] ^ D[15]=1 ^ D[13]=1 ^ D[11] ^ D[9] ^ D[5]=1 ^ D[4]=1 ^ D[3];

CRC[6] = D[67] ^ D[66] ^ D[65] ^ D[64] ^ D[62]=1 ^ D[61]=1 ^ D[58] ^ D[54]=1 ^ D[52]=1 ^ D[51] ^ D[50] ^ D[48] ^ D[47]=1 ^D[46]=1 ^ D[43] ^ D[41] ^ D[38]=1 ^ D[37]=1 ^ D[33] ^ D[32] ^ D[29]=1 ^ D[28]=1 ^ D[26] ^ D[21]=1 ^ D[19] ^ D[17] ^D[16] ^ D[14]=1 ^ D[12]=1 ^ D[10] ^ D[6]=1 ^ D[5]=1 ^ D[4]=1;

CRC[7] = D[68]=1 ^ D[67] ^ D[66] ^ D[65] ^ D[63]=1 ^ D[62]=1 ^ D[59] ^ D[55]=1 ^ D[53]=1 ^ D[52]=1 ^ D[51] ^ D[49] ^ D[48] ^D[47]=1 ^ D[44]=1 ^ D[42] ^ D[39]=1 ^ D[38]=1 ^ D[34] ^ D[33] ^ D[30]=1 ^ D[29]=1 ^ D[27] ^ D[22]=1 ^ D[20]=1 ^ D[18]^ D[17] ^ D[15] =1^ D[13]=1 ^ D[11] ^ D[7]=1 ^ D[6]=1 ^ D[5]=1;

CRC equations for x8 device in BC4 mode with A2=1 are as follows:

CRC[0] = 1 ^ 1 ^ D[71] ^ D[70] ^ D[68] ^ 1 ^ 1 ^ D[60] ^ 1 ^ 1 ^ 1 ^ D[54] ^ D[53] ^ D[52] ^ 1 ^ D[47] ^ D[44] ^ 1 ^ D[39] ^ D[38] ^1^ 1 ^ 1 ^ 1 ^ 1 ^ D[23] ^ D[22] ^ D[20] ^ 1 ^ 1 ^ D[12] ^ 1 ^ 1 ^ D[4] ;

CRC[1] = 1 ^ D[70] ^ D[69] ^ 1 ^ 1 ^ 1 ^ D[61] ^ D[60] ^ 1 ^ 1 ^ D[55] ^ D[52] ^ 1 ^ 1 ^ 1 ^ D[47] ^ D[45] ^ 1 ^ 1 ^ D[38] ^ D[36] ^ 1^ 1 ^ 1 ^ D[28] ^ 1 ^ 1 ^ 1 ^ 1 ^ D[22] ^ D[21] ^ D[20] ^1 ^ 1 ^1 ^ 1 ^ D[13] ^ 1 ^ D[5] ^ D[4];

CRC[2] = 1 ^ 1 ^ 1 ^1 ^1 ^ 1 ^ 1 ^ D[62] ^ D[61] ^ 1 ^ D[54] ^ D[52] ^ 1 ^ 1 ^ 1 ^ D[47] ^ D[46] ^ 1 ^ 1 ^ D[38] ^ D[37] ^ 1 ^ 1 ^ D[29]^ D[28] ^ 1 ^ D[21] ^ 1 ^ 1 ^ 1 ^ D[14] ^ D12] ^1 ^ D[6] ^ D[5] ^ D[4];

CRC[3] = 1 ^ 1 ^ D[68] ^ 1 ^ 1 ^ 1 ^ D[63] ^ D[62] ^ 1 ^ D[55] ^ D[53] ^ D[52] ^ 1 ^ 1 ^ 1 ^ D[47] ^ D[44] ^ 1 ^ D[39] ^ D[38] ^ 1 ^ 1^ D[30] ^ D[29] ^ 1 ^ D[22] ^ D[20] ^ 1 ^ 1 ^ D[15] ^ D[13] ^ 1 ^ D[7] ^ D[6] ^ D[5];

CRC[4] = 1 ^1 ^ D[69] ^ D[68] ^ 1 ^ 1 ^ 1 ^ D[63] ^ D[60] ^ 1 ^ D[54] ^ D[53] ^ D[52] ^ 1 ^1 ^ 1 ^ D[45] ^ 1 ^ 1 ^ D[39] ^1 ^ 1 ^ D[31]^ D[30] ^ D[28] ^ D[23] ^ D[21] ^ 1 ^ 1 ^ 1 ^ D[14] ^ D[12] ^ 1 ^ D[7] ^ D[6];

CRC[5] = 1 ^ D[70] ^ D[69] ^ D[68] ^ 1 ^ 1 ^ 1 ^ D[61] ^ 1 ^ D[55] ^ D[54] ^ D[53] ^ 1 ^ 1 ^ 1 ^ D[46] ^ D[44] ^ 1 ^ 1 ^ D[36] ^ 1 ^ 1^ D[31] ^ D[29] ^ 1 ^ D[22] ^ D[20] ^ 1 ^ 1 ^ D[15] ^ D[13] ^ 1 ^ 1 ^ D[7];

CRC[6] = D[71] ^ D[70] ^ D[69] ^ D[68] ^ 1 ^ 1 ^ D[62] ^ 1 ^ 1 ^ D[55] ^ D[54] ^ D[52] ^ 1 ^1 ^ D[47] ^ D[45] ^ 1 ^ 1 ^ D[37] ^ D[36]^1 ^ 1 ^ D[30] ^ 1 ^ D[23] ^ D[21] ^ D[20] ^ 1 ^ 1 ^ D[14] ^ 1 ^ 1 ^ 1;

CRC[7] = 1 ^ D[71] ^ D[70] ^ D[69] ^ 1 ^ 1 ^ D[63] ^ 1 ^ 1 ^ 1 ^ D[55] ^ D[53] ^ D[52] ^ 1 ^ 1 ^ D[46] ^ 1 ^ 1 ^ D[38] ^ D[37] ^ 1 ^ 1 ^ D[31] ^ 1 ^ 1 ^ D[22] ^ D[21] ^ 1^ 1 ^ D[15] ^ 1 ^ 1 ^ 1;

CRC Error Handling

CRC Error mechanism shares the same $\overline{\text{ALERT}}$ signal for reporting errors on writes to DRAM. The controller has no way to distinguish between CRC errors and Command/Address/Parity errors other than to read the DRAM mode registers. This is a very time consuming process in a multi-rank configuration.

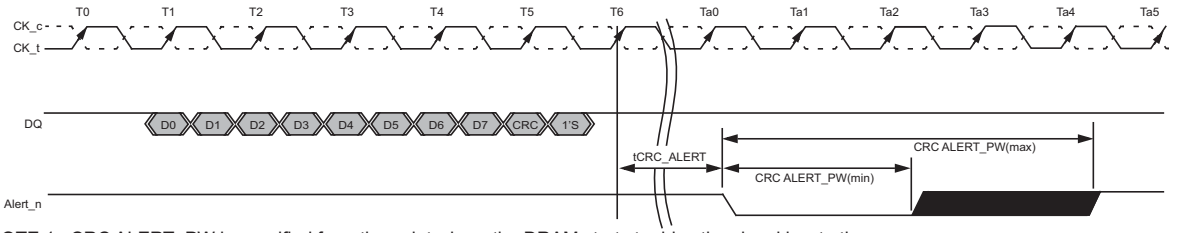
To speed up recovery for CRC errors, CRC errors are only sent back as a pulse. The minimum pulse-width is 2 clocks. The latency to $\overline{\text{ALERT}}$ signal is defined as tCRC_ALERT in the figure below.

DRAM will set CRC Error Clear bit in A4 of MR5 to '1' and CRC Error Status bit in MPR3 of page1 to '1' upon detecting a CRC error. The CRC Error Clear bit remains set at '1' until the host clears it explicitly using an MRS command.

The controller upon seeing an error as a pulse width will retry the write transactions. The controller understands the worst case delay for $\overline{\text{ALERT}}$ (during init) and can backup the transactions accordingly or the controller can be made more intelligent and try to correlate the write CRC error to a specific rank or a transaction. The controller is also responsible for opening any pages and ensuring that retrying of writes is done in a coherent fashion.

The pulse width may be seen longer than two clocks at the controller if there are multiple CRC errors as the $\overline{\text{ALERT}}$ is a daisy chain bus.

CRC Error Reporting



NOTE 1 CRC ALERT_PW is specified from the point where the DRAM starts to drive the signal low to the point where the DRAM driver releases and the controller starts to pull the signal up.

NOTE 2 Timing diagram applies to x4, x8, and x16 devices.

TIME BREAK

TRANSITIONING DATA

CRC Error Timing Parmeters

		DDR4-1600 /1866		DDR4-1866/ 2133		DDR4-2666		DDR4-3200		Unit
Parameter	**Symbol**	**min**	**max**	**min**	**max**	**min**	**max**	**min**	**max**	
CRC error to ALERT_n latency	tCRC_ALERT	-	13	-	13	-	13	-	13	ns
CRC ALERT_n pulse width	CRC ALERT_PW	6	10	6	10	6	10	6	10	nCK

Data Mask(DM), Data Bus Inversion (DBI) and TDQS

DDR4 SDRAM supports Data Mask (DM) function and Data Bus Inversion (DBI) function on in x8 and x16 DRAM configuration. x4 DDR4 SDRAM does not support DM and DBI function. x8 DDR4 SDRAM supports TDQS function. x4 and x16 DDR4 SDRAM does not support TDQS function.

DM, DBI & TDQS functions are supported with dedicated one pin labeled as $\overline{DM}$/$\overline{DBI}$/TDQS. The pin is bi-directional pin for DRAM. The $\overline{DM}$/$\overline{DBI}$ pin is Active Low as DDR4 supports VDDQ reference termination. TDQS function does not drive actual level on the pin.

DM, DBI & TDQS functions are programmable through DRAM Mode Register (MR). The MR bit location is bit A11 in MR1 and bit A12:A10 in MR5.

Write operation: Either DM or DBI function can be enabled but both functions cannot be enabled simultaneously. When both DM and DBI functions are disabled, DRAM turns off its input receiver and does not expect any valid logic level.

Read operation: Only DBI function applies. When DBI function is disabled, DRAM turns off its output driver and does not drive any valid logic level.

TDQS function: When TDQS function is enabled, DM & DBI functions are not supported. When TDQS function is disabled, DM andDBI functions are supported as described below table. When enabled, the same termination resistance function is applied tothe TDQS/$\overline{TDQS}$ pins that is applied to DQS/$\overline{DQS}$ pins.

TDQS Function Matrix

MR1 bit A11	DM (MR5 bit A10)	Write DBI (MR5 bit A11)	Read DBI (MR5 bit A12)
0 (TDQS Disabled)	Enabled	Disabled	Enabled or Disabled
	Disabled	Enabled	Enabled or Disabled
	Disabled	Disabled	Enabled or Disabled
1 (TDQS Enabled)	Disabled	Disabled	Disabled

DM function during Write operation: DRAM masks the write data received on the DQ inputs if $\overline{DM}$ was sampled Low on a given byte lane. If $\overline{DM}$ was sampled High on a given byte lane, DRAM does not mask the write data and writes into the DRAM core.

DBI function during Write operation: DRAM inverts write data received on the DQ inputs if $\overline{DBI}$ was sampled Low on a given byte lane. If $\overline{DBI}$ was sampled High on a given byte lane, DRAM leaves the data received on the DQ inputs non-inverted.

DBI function during Read operation: DRAM inverts read data on its DQ outputs and drives $\overline{DBI}$ pin Low when the number of '0' data bits within a given byte lane is greater than 4; otherwise DRAM does not invert the read data and drives $\overline{DBI}$ pin High.

x8 DRAM Write DQ Frame Format

	Data transfer							
	0	1	2	3	4	5	6	7
DQ[7:0]	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
$\overline{DM}$ or $\overline{DBI}$	DM0 or DBI0	DM1 or DBI1	DM2 or DBI2	DM3 or DB3	DM4 or DBI4	DM5 or DBI5	DM6 or DBI6	DM7 or DBI7

x8 DRAM Read DQ Frame Format

	Data transfer							
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
DQ[7:0]	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
$\overline{\text{DBI}}$	DBI0	DBI1	DBI2	DBI3	DBI4	DBI5	DBI6	DBI7

x16 DRAM Write DQ Frame Format

	Data transfer							
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
DQ[7:0]	LByte 0	LByte 1	LByte 2	LByte 3	LByte 4	LByte 5	LByte 6	LByte 7
$\overline{\text{LDM}}$ or $\overline{\text{LDBI}}$	LDM0 or LDBI0	LDM1 or LDBI1	LDM2 or LDBI2	LDM3 or LDBI3	LDM4 or LDBI4	LDM5 or LDBI5	LDM6 or LDBI6	LDM7 or LDBI7
DQ[7:0]	UByte 0	UByte 1	UByte 2	UByte 3	UByte 4	UByte 5	UByte 6	UByte 7
$\overline{\text{UDM}}$ or $\overline{\text{UDBI}}$	UDM0 or UDBI0	UDM1 or UDBI1	UDM2 or UDBI2	UDM3 or UDB3	UDM4 or UDBI4	UDM5 or UDBI5	UDM6 or UDBI6	UDM7 or UDBI7

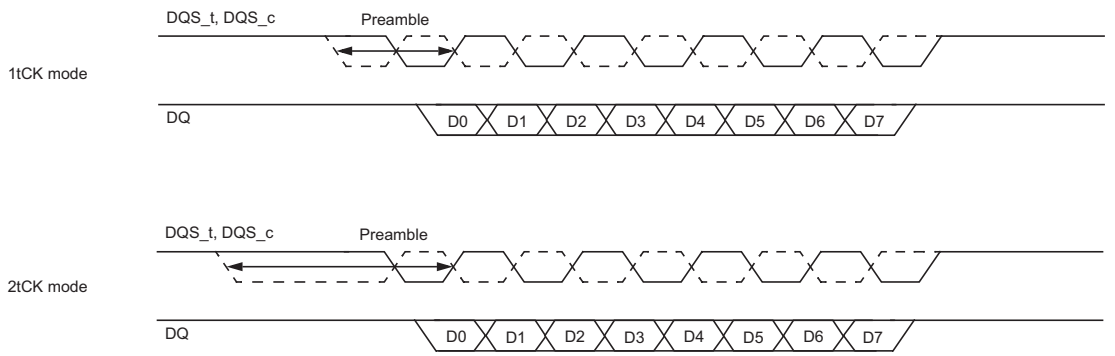
x16 DRAM Read DQ Frame Format

	Data transfer							
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
DQ[7:0]	LByte 0	LByte 1	LByte 2	LByte 3	LByte 4	LByte 5	LByte 6	LByte 7
$\overline{\text{LDBI}}$	LDBI0	LDBI1	LDBI2	LDBI3	LDBI4	LDBI5	LDBI6	LDBI7
DQ[7:0]	UByte 0	UByte 1	UByte 2	UByte 3	UByte 4	UByte 5	UByte 6	UByte 7
$\overline{\text{UDBI}}$	UDBI0	UDBI1	UDBI2	UDB3	UDBI4	UDBI5	UDBI6	UDBI7

Programmable Preamble

DDR4 will support a programmable write preamble.Write preamble modes of 1 tCK and 2 tCK are shown below.
1 tCK and 2 tCK modes are selectable by MRS.
CWL needs to be incremented by 1nCK when 2tCK preamble is enabled.
When operating in 2tCK Write Preamble Mode, tWTR and tWR must be programmed to a value 1 clock greater than the tWTR and tWR setting supported in the applicable speed bin.

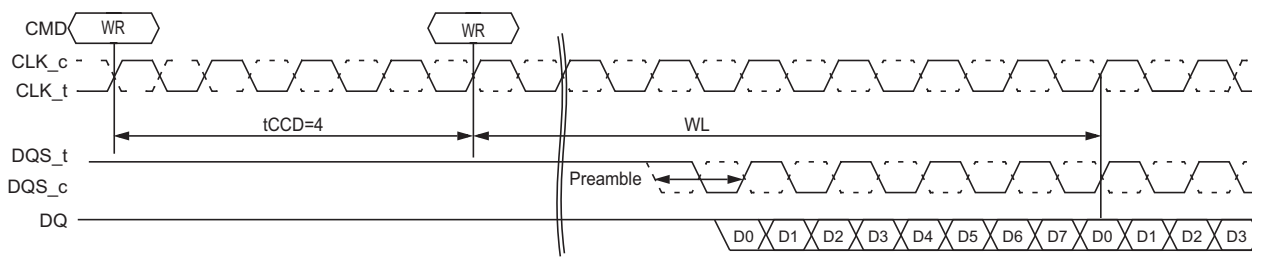
1tCK vs 2tCK Write Preamble Mode



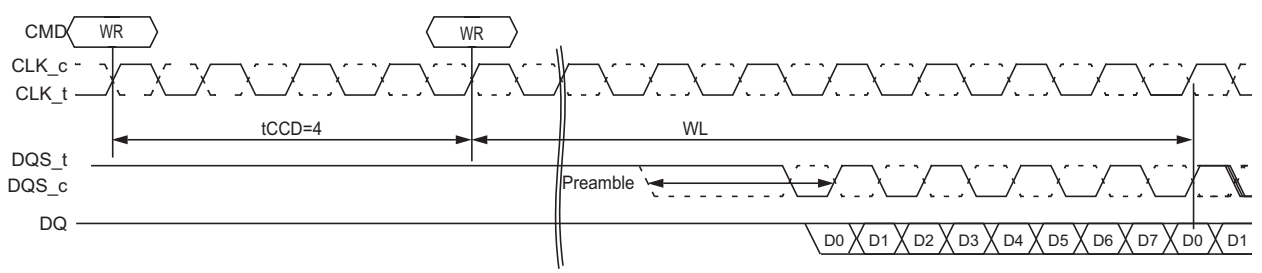
The timing diagrams contained in figure below illustrate 1 and 2 tCK preamble scenarios for consecutive write commands with tCCD timing of 4, 5 and 6 nCK, respectively. Setting tCCD to 5nCK is not allowed in 2 tCK preamble mode.

1tCK vs 2tCK Write Preamble Mode, tCCD=4 (AL=PL=0)

1tCK mode

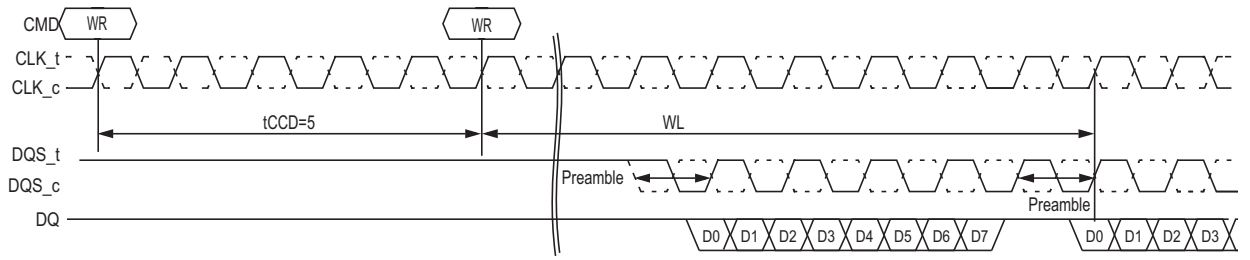


2tCK mode



1tCK vs 2tCK Write Preamble Mode, tCCD=5 (AL=PL=0)

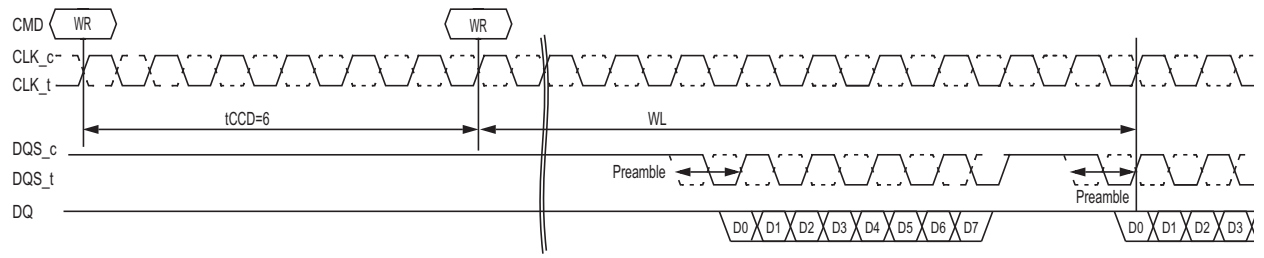
1tCK mode



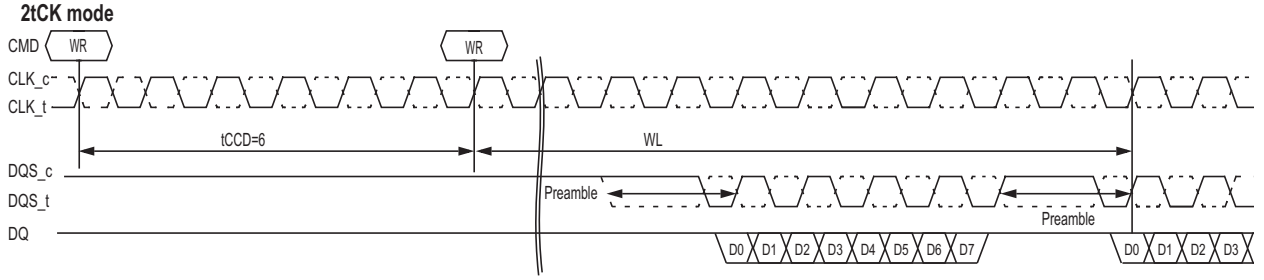
2tCK mode: tCCD=5 is not allowed in 2tCK mode

1tCK vs 2tCK Write Preamble Mode, tCCD=6 (AL=PL=0)

1tCK mode



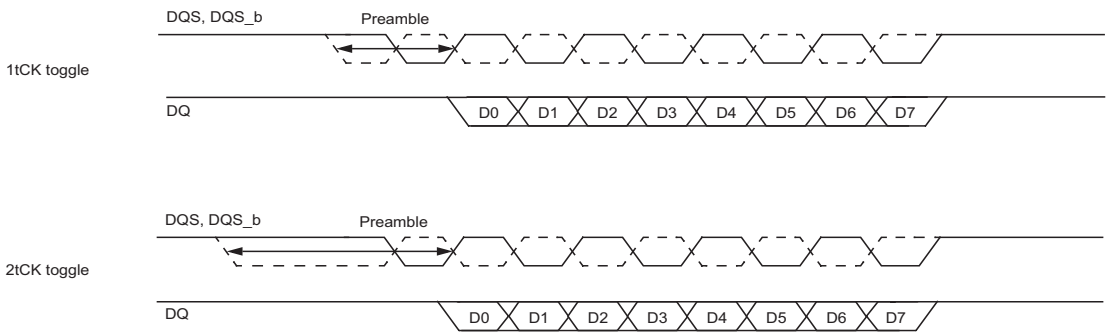
2tCK mode



Read Preamble

DDR4 will support a programmable read preamble.

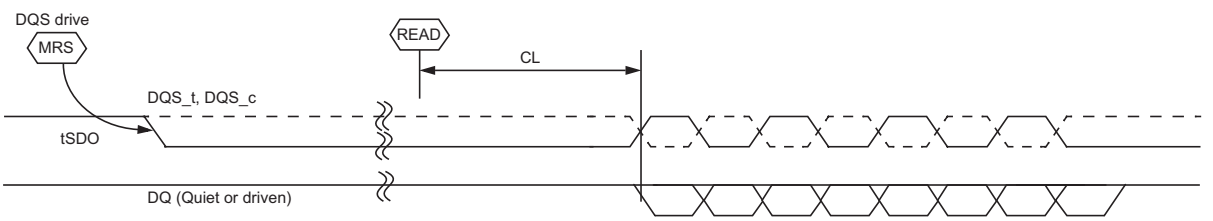
1tCK vs 2tCK Read Preamble Mode



Read Preamble Training

DDR4 will support a programmable read preamble. This requires an additional MRS mode to train the read preamble for read leveling. The MRS mode below will be used for Read preamble training and It is only available in MPR mode.

Illegal READ commands, any command during the READ process or initiating the READS process, are not allowed during Read Preamble Training.



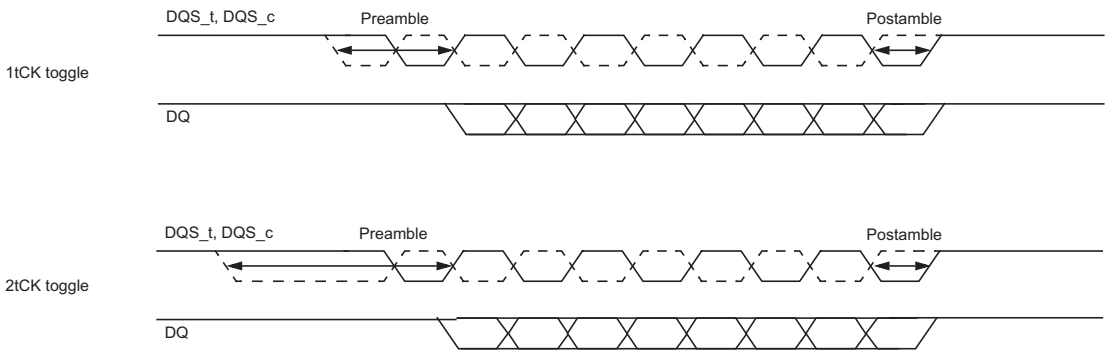
Parameter	Symbol	DDR4-2133,2400,2666		Units	NOTE
		Min	Max		
Delay from MRS Command to Data Strobe Drive Out	tSDO	-	tMOD+9ns		

Postamble

Read Postamble

DDR4 will support a fixed read postamble.

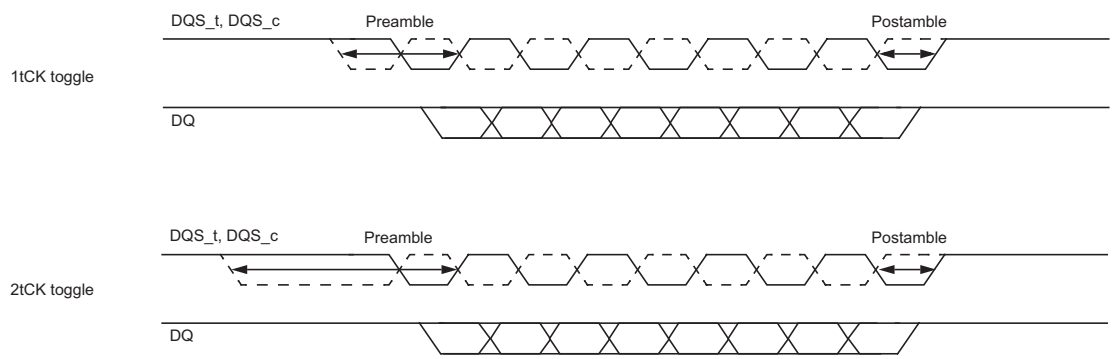
Read postamble of nominal 0.5tck for preamble modes 1,2 Tck are shown below:



Write Postamble

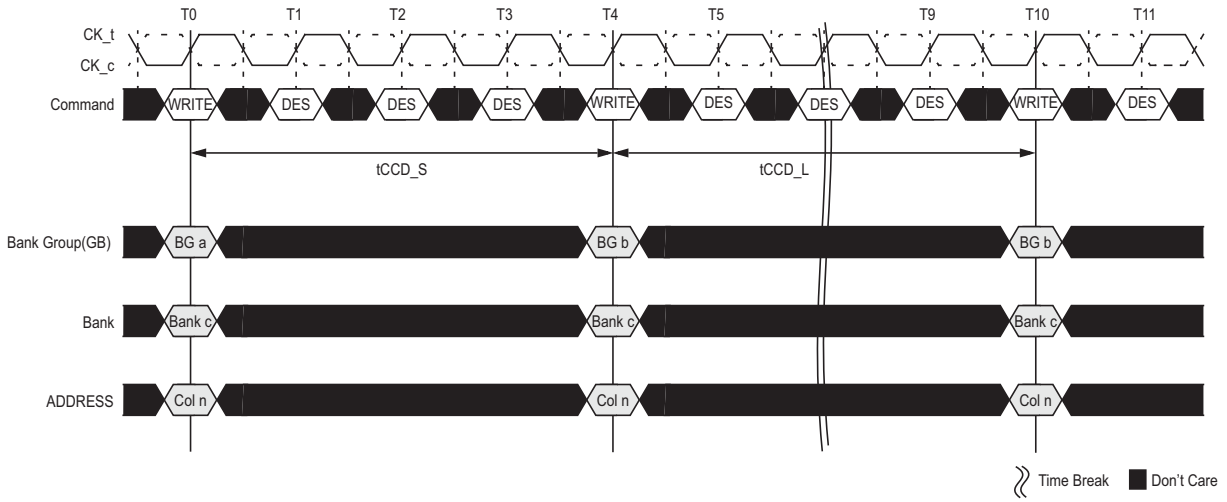
DDR4 will support a fixed Write postamble.

Write postamble nominal is 0.5tck for preamble modes 1,2 Tck are shown below:



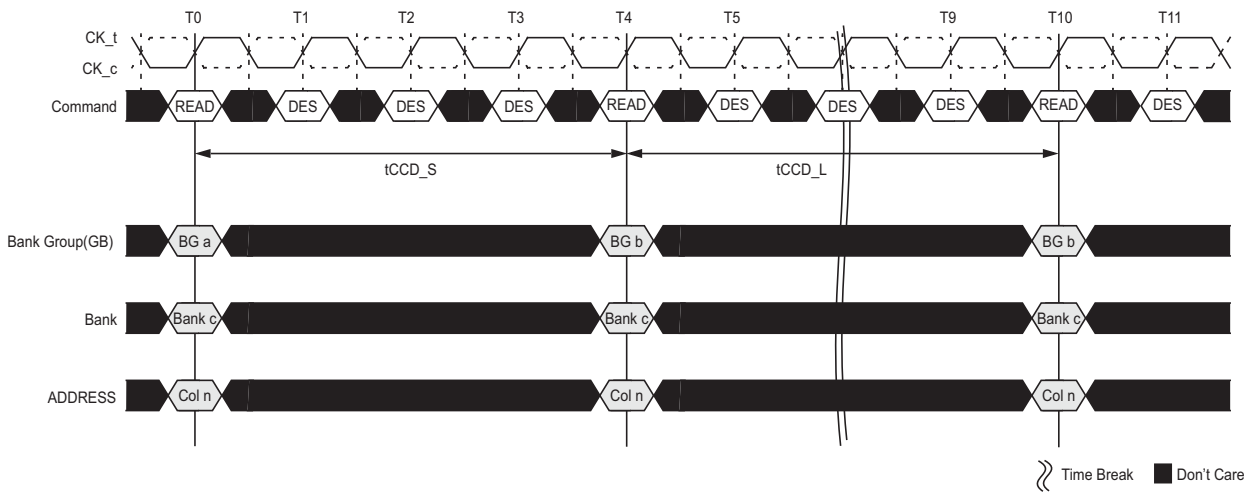
DDR4 Key Core Timing

tCCD Timing (WRITE to WRITE Example)



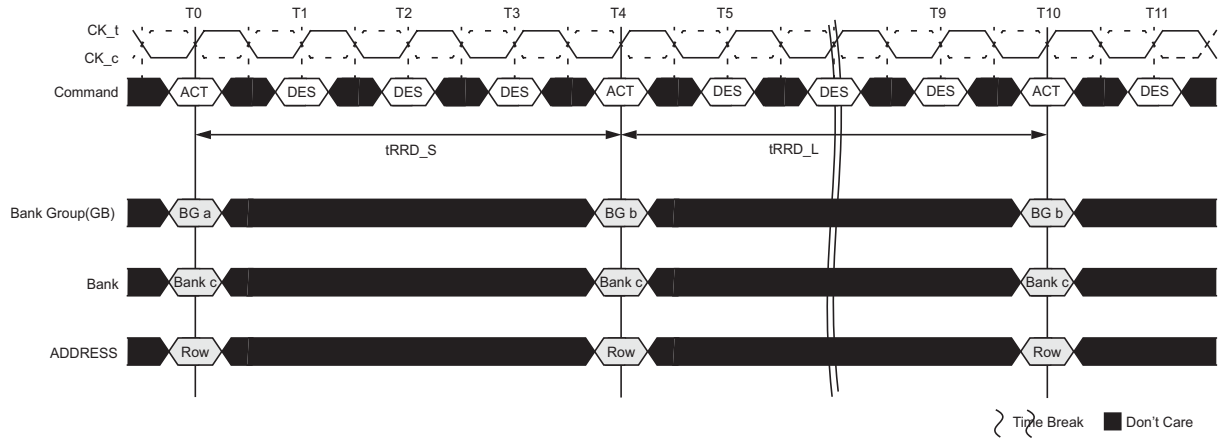
NOTE 1 tCCD_S : $\overline{CAS}$-to-$\overline{CAS}$ delay (short) : Applies to consecutive $\overline{CAS}$ to different Bank Group (i.e., T0 to T4)
NOTE 2 tCCD_L : $\overline{CAS}$-to-$\overline{CAS}$ delay (long) : Applies to consecutive $\overline{CAS}$ to the same Bank Group (i.e., T4 to T10)

tCCD Timing (READ to READ Example)



NOTE 1 tCCD_S : $\overline{CAS}$-to-$\overline{CAS}$ delay (short) : Applies to consecutive $\overline{CAS}$ to different Bank Group (i.e., T0 to T4)
NOTE 2 tCCD_L : $\overline{CAS}$-to-$\overline{CAS}$ delay (long) : Applies to consecutive $\overline{CAS}$ to the same Bank Group (i.e., T4 to T10)

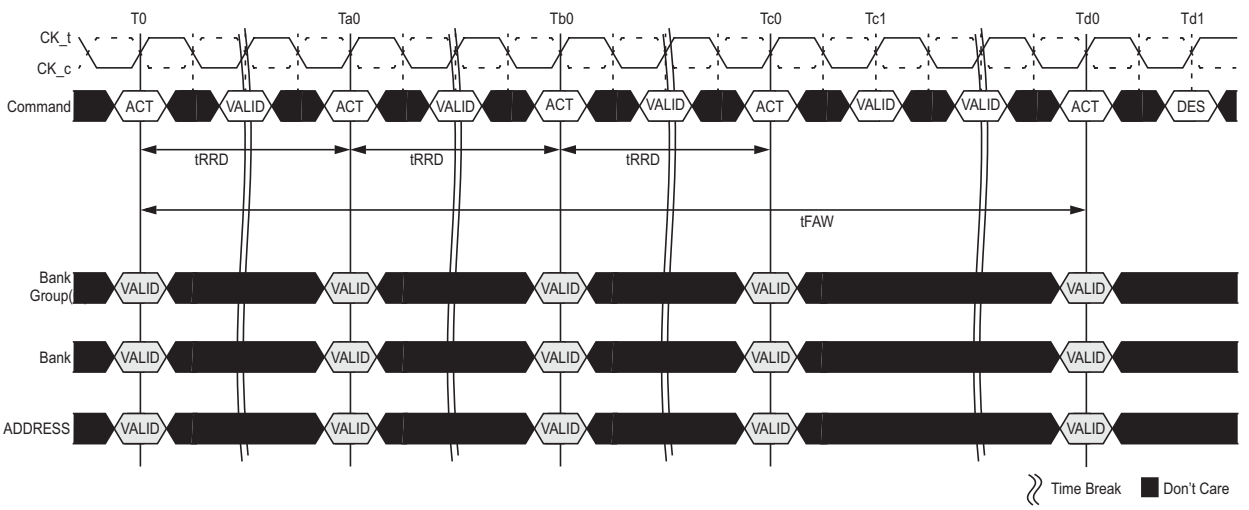
tRRD Timing



NOTE 1 RRD_S : ACTIVATE to ACTIVATE Command period (short) : Applies to consecutive ACTIVATE Commands to different Bank Group (i.e. T0 toT4)

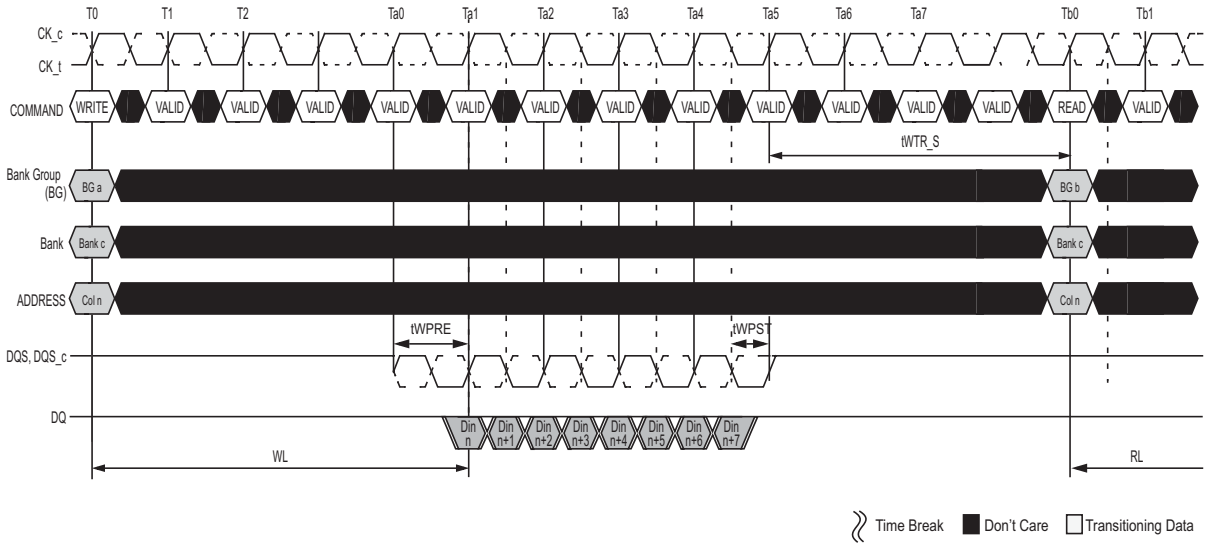
NOTE 2 tRRD_L : ACTIVATE to ACTIVATE Command period (long) : Applies to consecutive ACTIVATE Commands to the different Banks of the sameBank Group (i.e. T4 to T10)

tFAW Timing



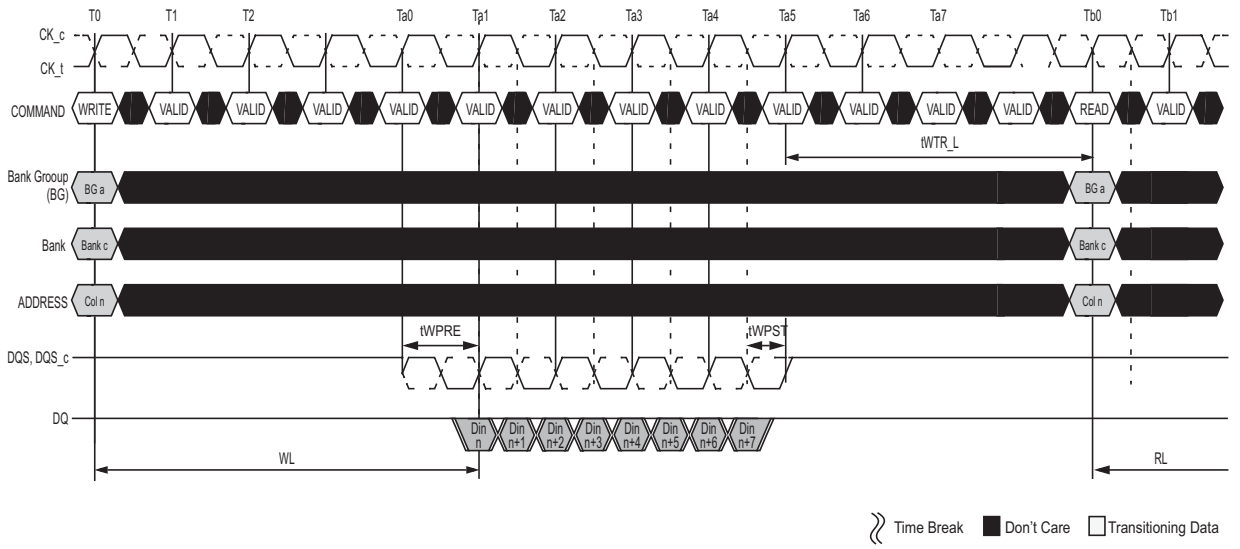
NOTE 1 tFAW : Four activate window.

tWTR_S Timing (WRITE to READ, Different Bank Group, CRC and DM Disabled)



NOTE 1 tWTR_S : Delay from start of internal write transaction to internal read command to a different Bank Group.

tWTR_L Timing (WRITE to READ, Same Bank Group, CRC and DM Disabled)



NOTE 1 tWTR_L : Delay from start of internal write transaction to internal read command to the same Bank Group.

Read Operation

READ Timing Definitions

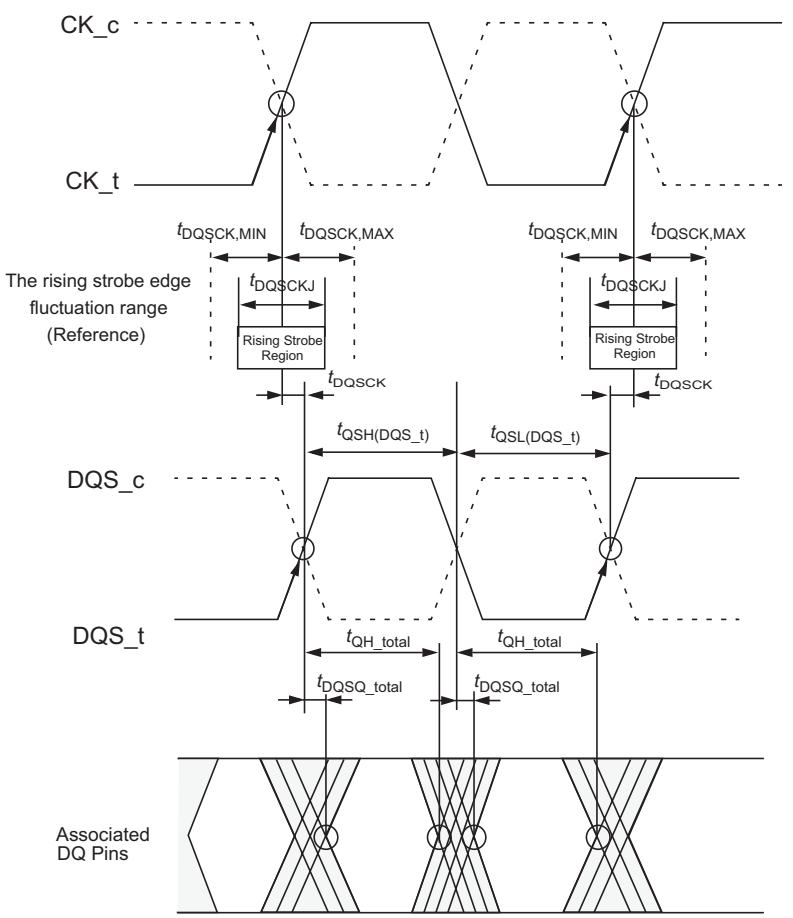
Read timing shown in this section is applied when the DLL is enabled and locked.

Rising data strobe edge parameters:
-tDQSCK min/max describes the allowed range for a rising data strobe edge relative to CK, $\overline{CK}$.
-tDQSCK is the actual position of a rising strobe edge relative to CK, $\overline{CK}$.
-tQSH describes the DQS, $\overline{DQS}$ differential output high time.
-tDQSQ describes the latest valid transition of the associated DQ pins.
-tQH describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:
-tQSL describes the DQS, $\overline{DQS}$ differential output low time.
-tDQSQ describes the latest valid transition of the associated DQ pins.
-tQH describes the earliest invalid transition of the associated DQ pins.

tDQSQ; both rising/falling edges of DQS, no tAC defined.

READ Timing Definition



READ Timing; Clock to Data Strobe relationship

Clock to Data Strobe relationship is shown in figure below and is applied when the DLL is enabled and locked.

Rising data strobe edge parameters:

-tDQSCK min/max describes the allowed range for a rising data strobe edge relative to CK, $\overline{CK}$.

-tDQSCK is the actual position of a rising strobe edge relative to CK, $\overline{CK}$.

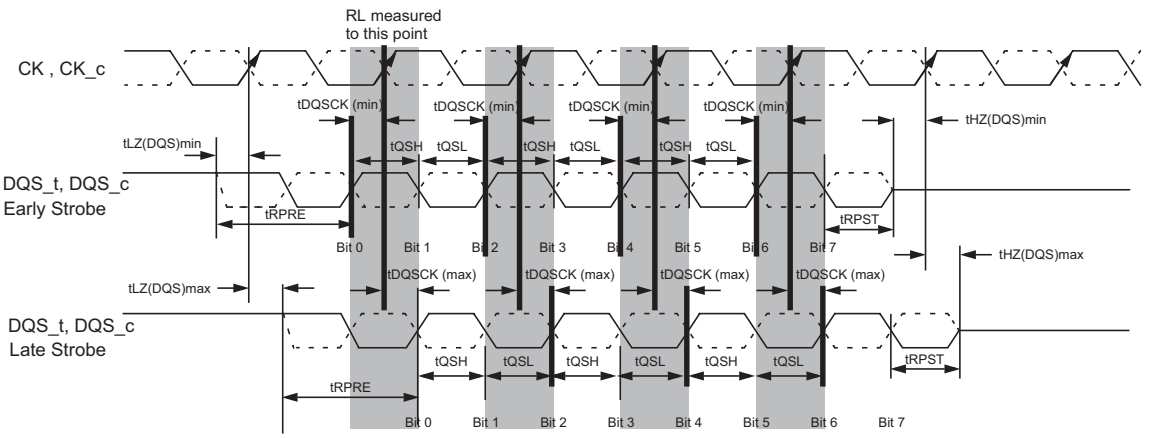
-tQSH describes the data strobe high pulse width.

Falling data strobe edge parameters:

-tQSL describes the data strobe low pulse width.

-tLZ(DQS), tHZ(DQS) for preamble/postamble.

Clock to Data Strobe Relationship



NOTE 1 Within a burst, rising strobe edge will be varied within tDQSCKJ by fixed and constant VDD. However incorporate the device, voltage and temperature variation, rising strobe edge will be varied between tDQSCK(min) and tDQSCK(max).

NOTE 2 Notwithstanding note 1, a rising strobe edge with tDQSCK(max) at T(n) can not be immediately followed by a rising strobe edge with tDQSCK(min) at T(n+1). This is because other timing relationships (tQSH, tQSL) exist:

if tDQSCK(n+1) < 0:

tDQSCK(n) < 1.0 tCK - (tQSHmin + tQSLmin) - |tDQSCK(n+1)|

NOTE 3 The DQS, $\overline{DQS}$ differential output high time is defined by tQSH and the DQS, $\overline{DQS}$ differential output low time is defined by tQSL.

NOTE 4 Likewise, tLZ(DQS)min and tHZ(DQS)min are not tied to tDQSCKmin (early strobe case) and tLZ(DQS)max and tHZ(DQS)max are not tied to tDQSCKmax (late strobe case).

NOTE 5 The minimum pulse width of read preamble is defined by tRPRE(min).

NOTE 6 The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZDQS(max) on the right side.

NOTE 7 The minimum pulse width of read postamble is defined by tRPST(min).

NOTE 8 The maximum read preamble is bound by tLZDQS(min) on the left side and tDQSCK(max) on the right side.

READ Timing; Data Strobe to Data relationship

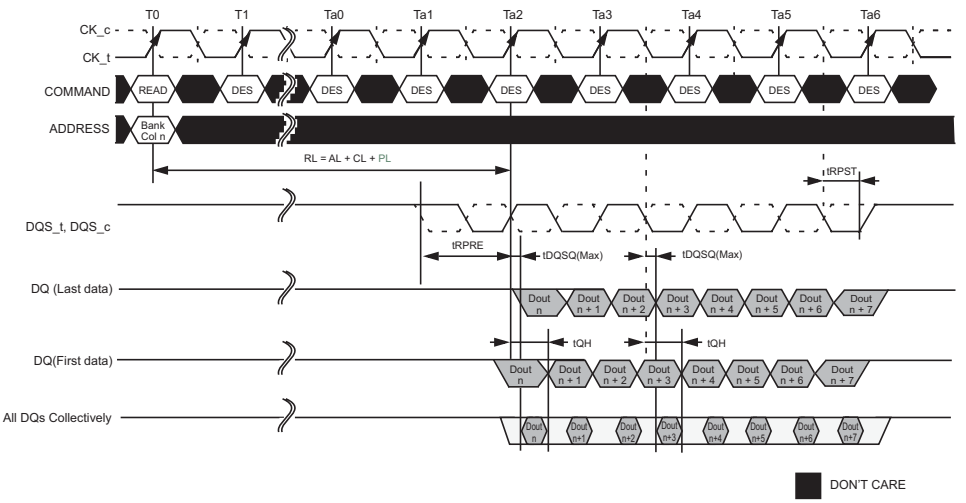
The Data Strobe to Data relationship is shown in Figure 67 and is applied when the DLL is enabled and locked.

Rising data strobe edge parameters:
-tDQSQ describes the latest valid transition of the associated DQ pins.
-tQH describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:
-tDQSQ describes the latest valid transition of the associated DQ pins.
-tQH describes the earliest invalid transition of the associated DQ pins.

tDQSQ; both rising/falling edges of DQS, no tAC defined

Data Strobe to Data Relationship



NOTE 1 BL = 8, AL = 0, CL = 11, Preamble = 1tCK.

NOTE 2 DOUT n = data-out from column n.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T0.

NOTE 5 Output timings are referenced to VDDQ, and DLL on for locking.

NOTE 6 tDQSQ defines the skew between DQS,$\overline{\text{DQS}}$ to Data and does not define DQS, $\overline{\text{DQS}}$ to Clock.

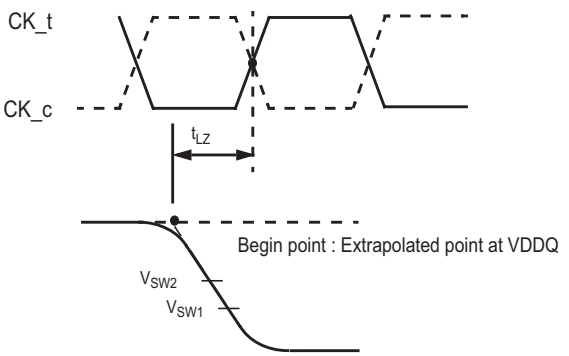
NOTE 7 Early Data transitions may not always happen at the same DQ. Data transitions of a DQ can vary (either early or late) within a burst.

tLZ(DQS), tLZ(DQ), tHZ(DQS), tHZ(DQ) Calculation

tHZ and tLZ transitions occur in the same time window as valid data transitions. These parameters are referenced to a specific voltage level that specifies when the device output is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ). The figure below shows a method to calculate the point when the device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ), by measuring the signal at two different voltages. The actual voltage measurement points are not critical aslong as the calculation is consistent. The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single ended.

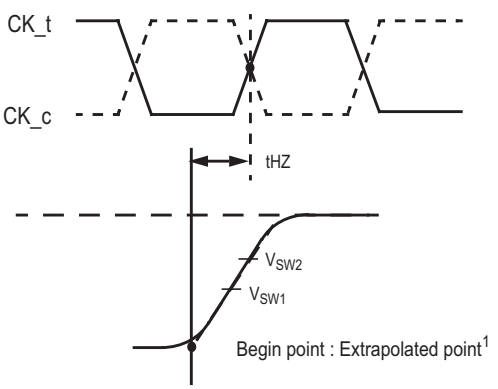
tLZ and tHZ method for calculating transitions and begin points

tLZ(DQ): CK_t - CK_c rising crossing at RL



tLZ(DQ) begin point is above-mentioned extrapolated point.

tHZ(DQ) with BL8: CK_t - CK_c rising crossing at RL + 4 nCK
tHZ(DQ) with BC4: CK_t - CK_c rising crossing at RL + 2 nCK



tHZ(DQ) is begin point is above-mentioned extrapolated point.

NOTE 1 Extrapolated point (Low Level) = VDDQ - ((VDDQ/(50+34)) X 34)
- Ron = 34ohm
- Reference Load= 50ohm

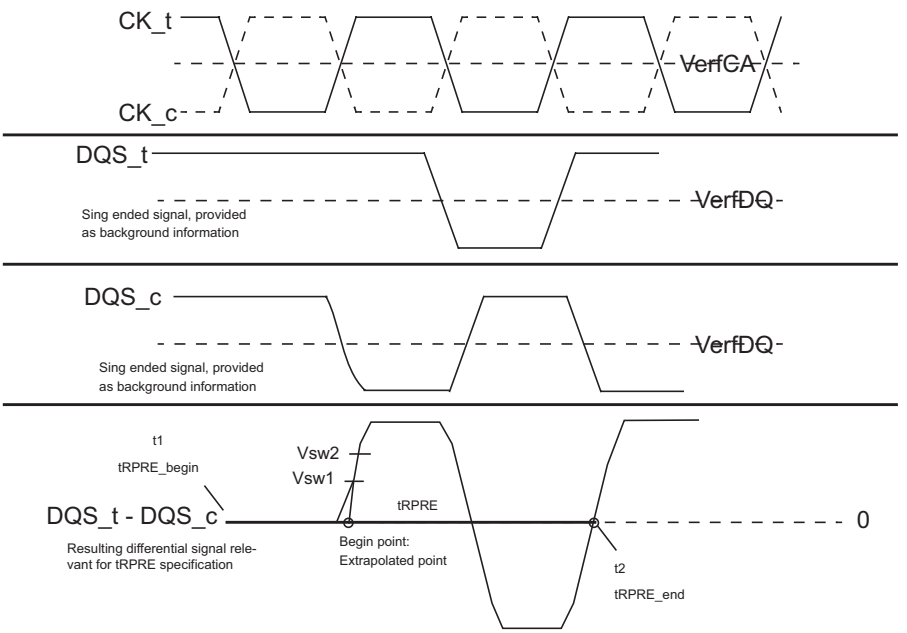
Reference Voltage for tLZ, tHZ Timing Measurements

Measured Parameter Symbol	Measured Parameter	Vsw1 [V]	Vsw2 [V]
tLZ	DQ low-impedance time from CK, $\overline{CK}$	(0.70-0.04) x VDDQ	(0.70+0.04) x VDDQ
tHZ	DQ high-impedance time from CK, $\overline{CK}$	(0.70-0.04) x VDDQ	(0.70+0.04) x VDDQ

tRPRE Calculation

The method for calculating differential pulse widths for tRPRE is shown in figure below.

Method for calculating tRPRE transitions and endpoints



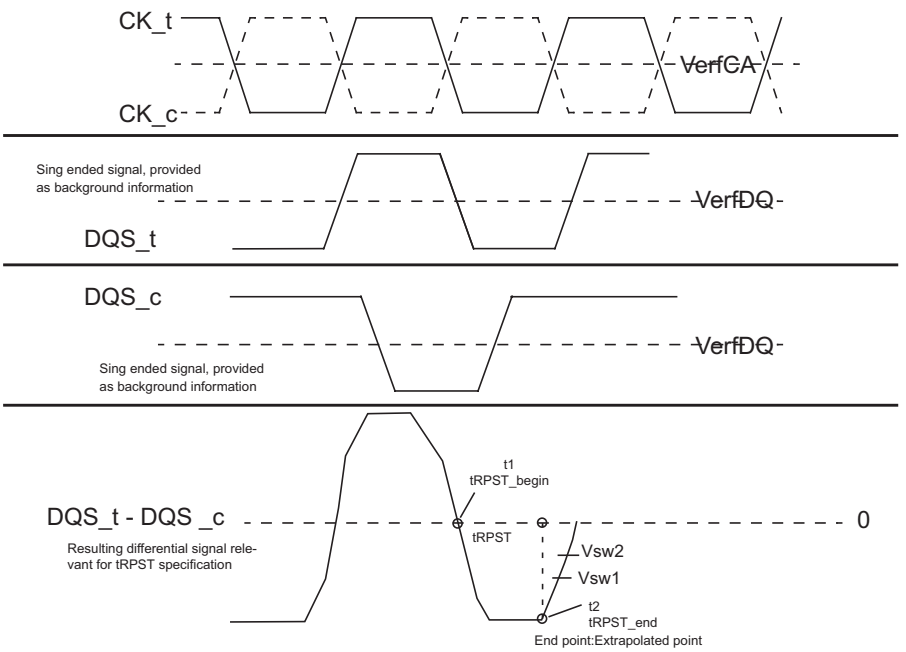
Reference Voltage for tRPRE Timing Measurements

Measured Parameter Symbol	Measured Parameter	Vsw1 [V]	Vsw2 [V]
tRPRE	DQS, $\overline{DQS}$ differential READ Preamble	(0.30-0.04) x VDDQ	(0.30+0.04) x VDDQ

tRPST Calculation

The method for calculating differential pulse widths for tRPST is shown in figure below.

Method for calculating tRPST transitions and endpoints



Reference Voltage for tRPRE Timing Measurements

Measured Parameter Symbol	Measured Parameter	Vsw1 [V]	Vsw2 [V]
tRPST	DQS, $\overline{DQS}$ differential READ Postamble	(-0.30-0.04) x VDDQ	(-0.30+0.04) x VDDQ

READ Burst Operation

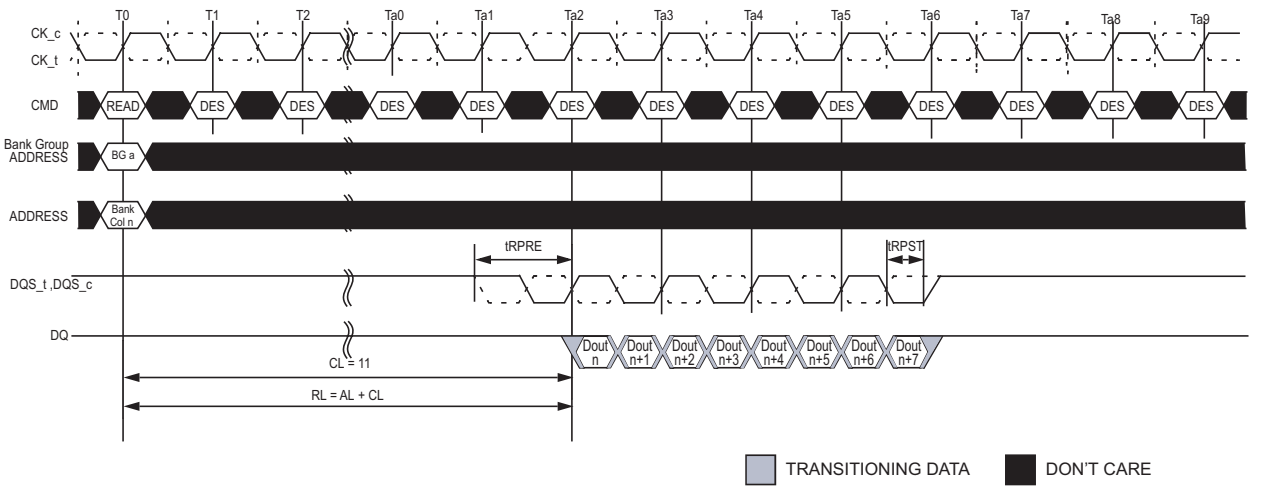
During a READ or WRITE command, DDR4 will support BC4 and BL8 on the fly using address A12 during the READ or WRITE (AUTO PRECHARGE can be enabled or disabled).

-A12 = 0 : BC4 (BC4 = burst chop)

-A12 = 1 : BL8

A12 is used only for burst length control, not as a column address.

READ Burst Operation RL = 11 (AL = 0, CL = 11, BL8)



NOTE 1 BL = 8, AL = 0, CL = 11, Preamble = 1tCK

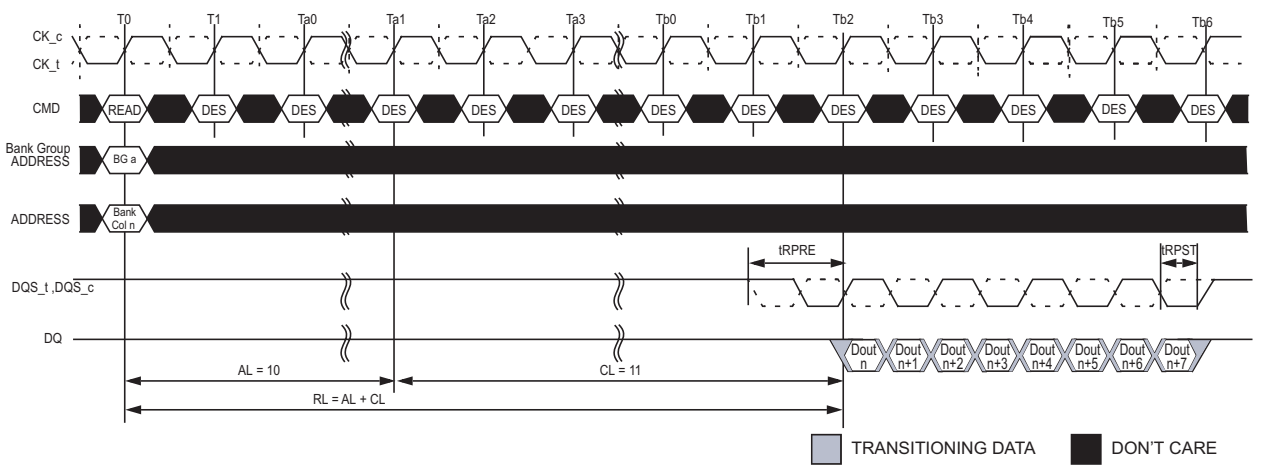
NOTE 2 DOUT n = data-out from column n.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T0.

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable

READ Burst Operation RL = 21 (AL = 10, CL = 11, BL8)



NOTE 1 BL = 8, RL = 21, AL = (CL-1), CL = 11, Preamble = 1tCK

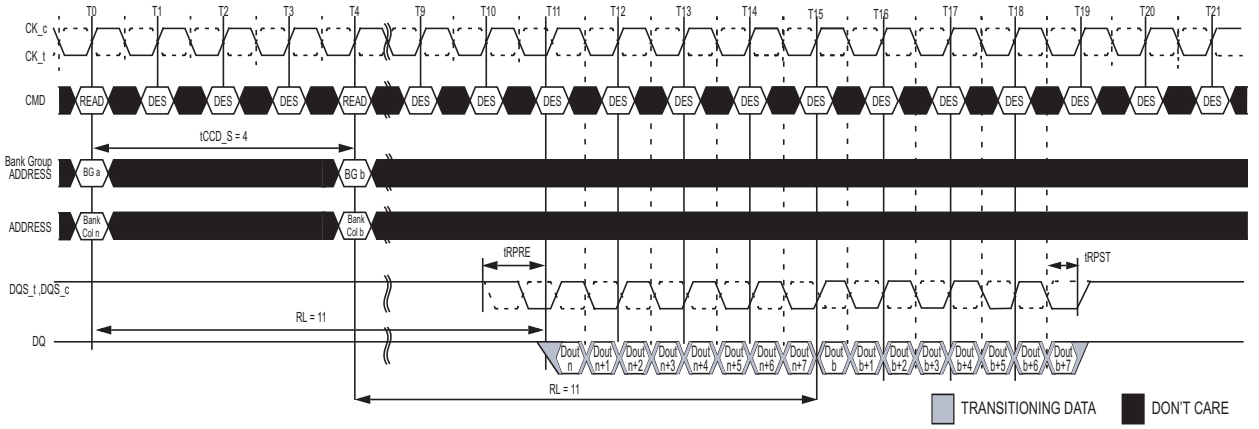
NOTE 2 DOUT n = data-out from column n.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T0.

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable

Consecutive READ (BL8) with 1tCK Preamble in Different Bank Group



NOTE 1 BL = 8, AL = 0, CL = 11, Preamble = 1tCK

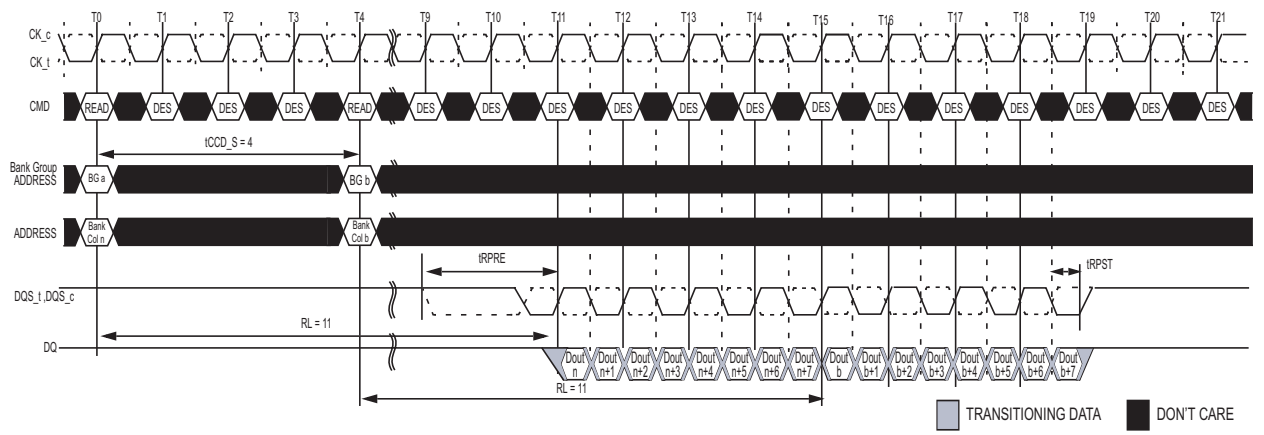
NOTE 2 DOUT n (or b) = data-out from column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and T4.

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable

Consecutive READ (BL8) with 2tCK Preamble in Different Bank Group



NOTE 1 BL = 8, AL = 0, CL = 11, Preamble = 2tCK

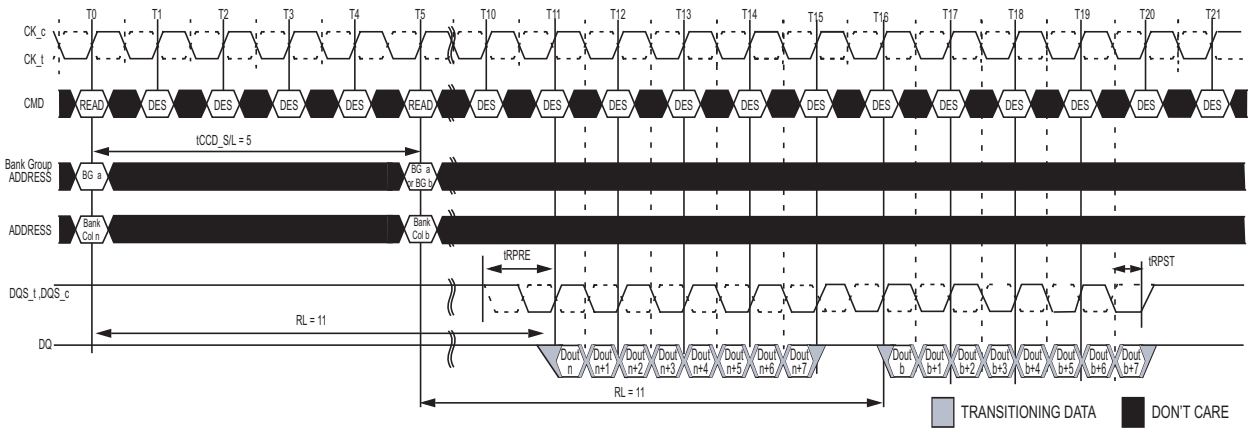
NOTE 2 DOUT n (or b) = data-out from column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and T4.

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable

Nonconsecutive READ (BL8) with 1tCK Preamble in Same or Different Bank Group



NOTE 1 BL = 8, AL = 0, CL = 11, Preamble = 1tCK, tCCD_S/L = 5

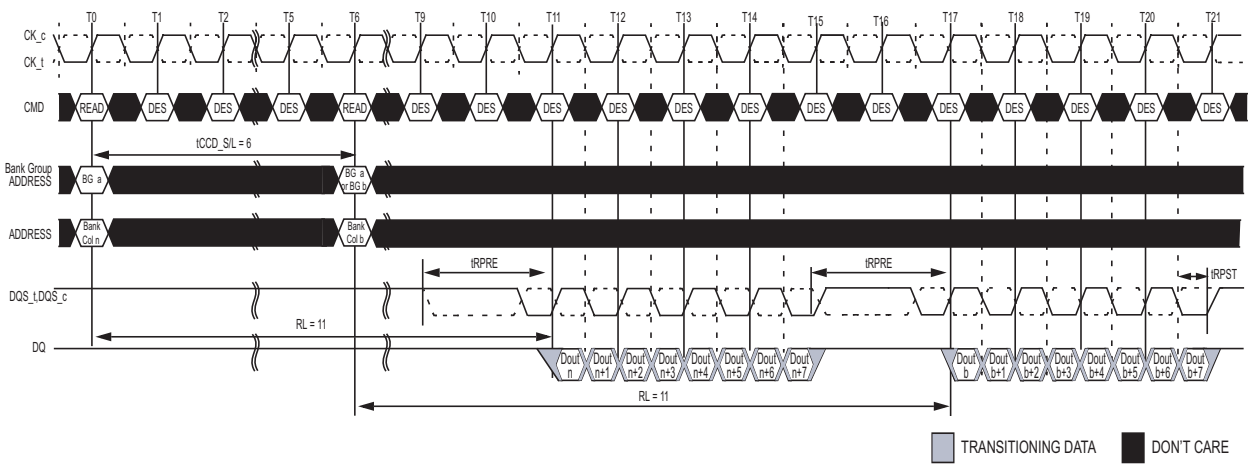
NOTE 2 DOUT n (or b) = data-out from column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and T5.

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable

Nonconsecutive READ (BL8) with 2tCK Preamble in Same or Different Bank Group



NOTE 1 BL = 8, AL = 0, CL = 11, Preamble = 2tCK, tCCD_S/L = 6

NOTE 2 DOUT n (or b) = data-out from column n (or column b).

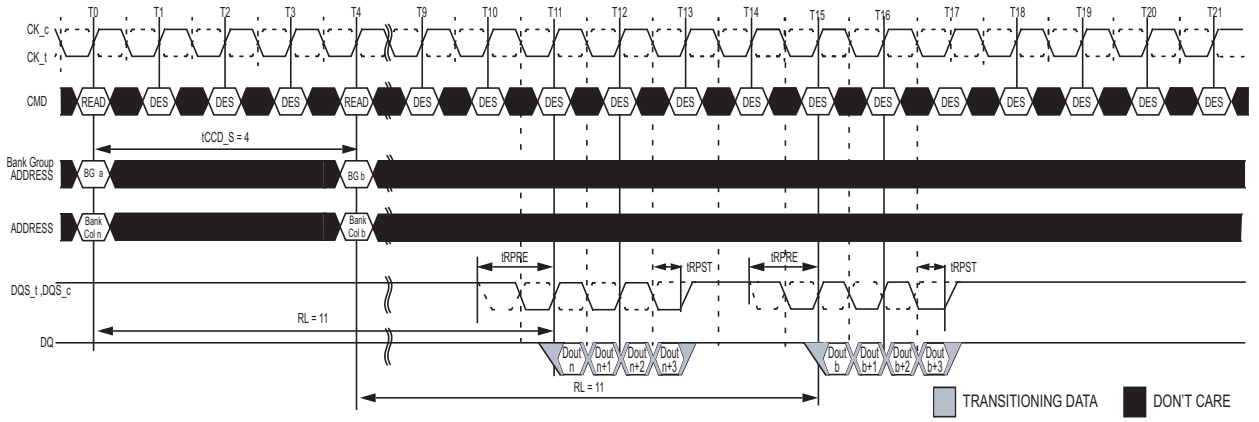
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and T6.

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable

NOTE 6 tCCD_S/L=5 isn't allowed in 2tCK preamble mode.

READ (BC4) to READ (BC4) with 1tCK Preamble in Different Bank Group



NOTE 1 BL = 8, AL = 0, CL = 11, Preamble = 1tCK

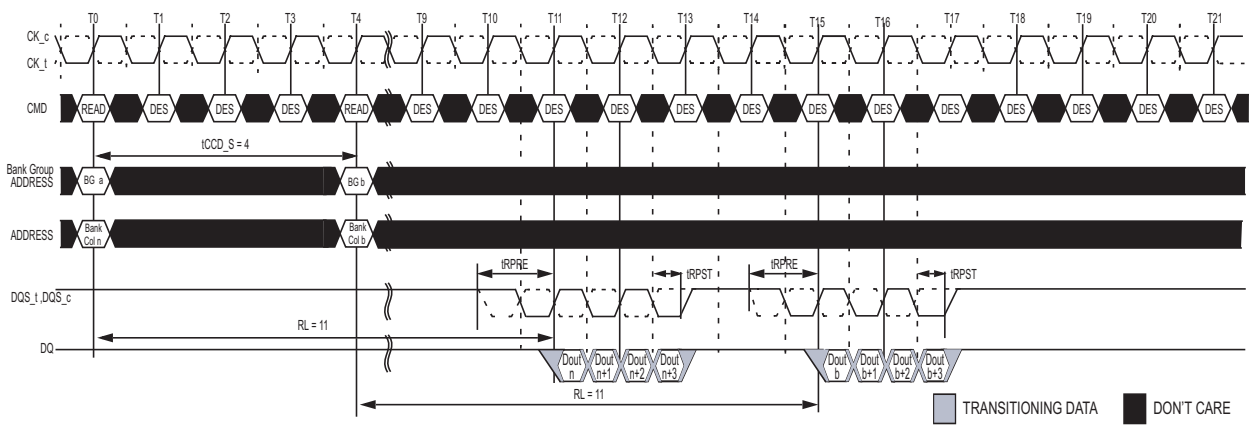
NOTE 2 DOUT n (or b) = data-out from column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by either MR0[A1:A0 = 1:0] or MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0 and T4.

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable

READ (BC4) to READ (BC4) with 2tCK Preamble in Different Bank Group



NOTE 1 BL = 8, AL = 0, CL = 11, Preamble = 2tCK

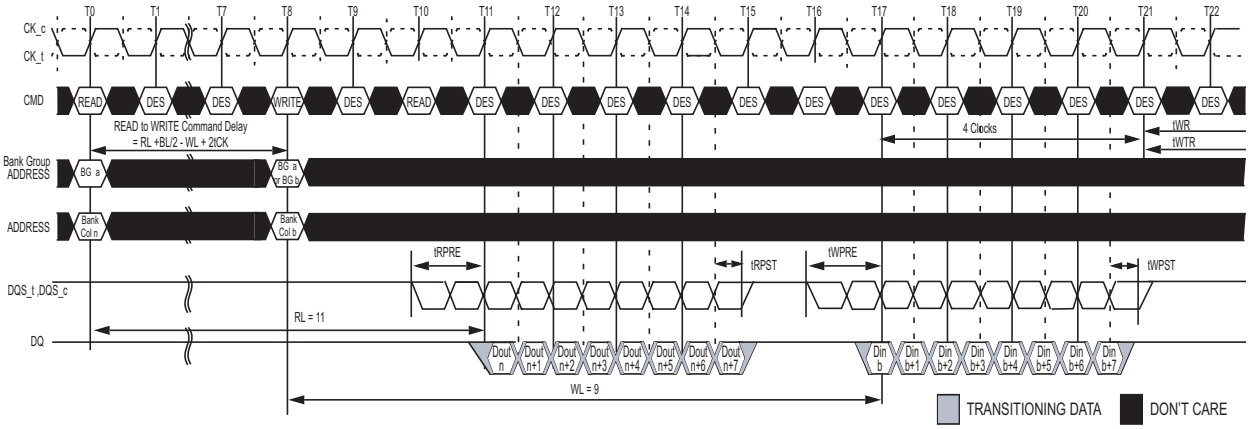
NOTE 2 DOUT n (or b) = data-out from column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by either MR0[A1:A0 = 1:0] or MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0 and T4.

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable

READ (BL8) to WRITE (BL8) with 1tCK Preamble in Same or Different Bank Group



NOTE 1 BL = 8, RL = 11 (CL = 11, AL = 0), Read Preamble = 1tCK, WL =9 (CWL = 9, AL = 0), Write Preamble = 1tCK

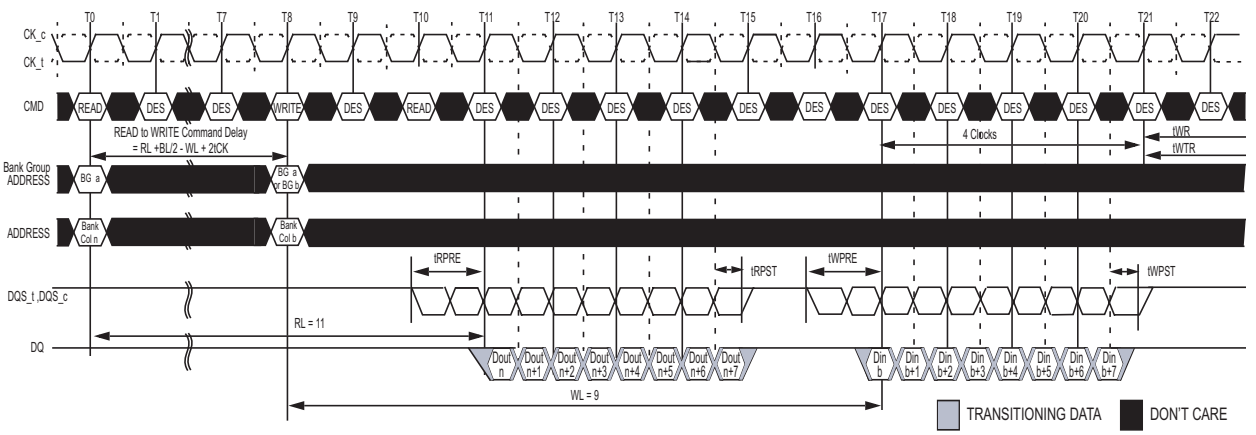
NOTE 2 DOUT n = data-out from column n, DIN b = data-in to column b.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and WRITE command at T8.

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

READ (BL8) to WRITE (BL8) with 2tCK Preamble in Same or Different Bank Group



NOTE 1 BL = 8, RL = 11 (CL = 11, AL = 0), Read Preamble = 2tCK, WL = 10 (CWL = 9+1[*5], AL = 0), Write Preamble = 2tCK

NOTE 2 DOUT n = data-out from column n, DIN b = data-in to column b.

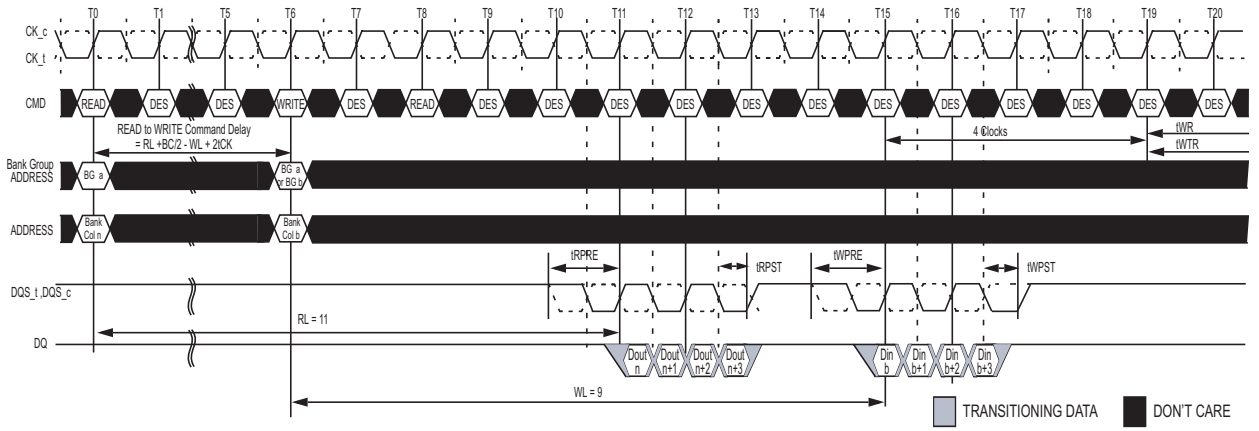
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and WRITE command at T8.

NOTE 5 When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting.

NOTE 6 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

READ (BC4) OTF to WRITE (BC4) OTF with 1tCK Preamble in Same or Different Bank Group



NOTE 1 BC = 4, RL = 11 (CL = 11, AL = 0), Read Preamble = 1tCK, WL = 9 (CWL = 9, AL = 0), Write Preamble = 1tCK

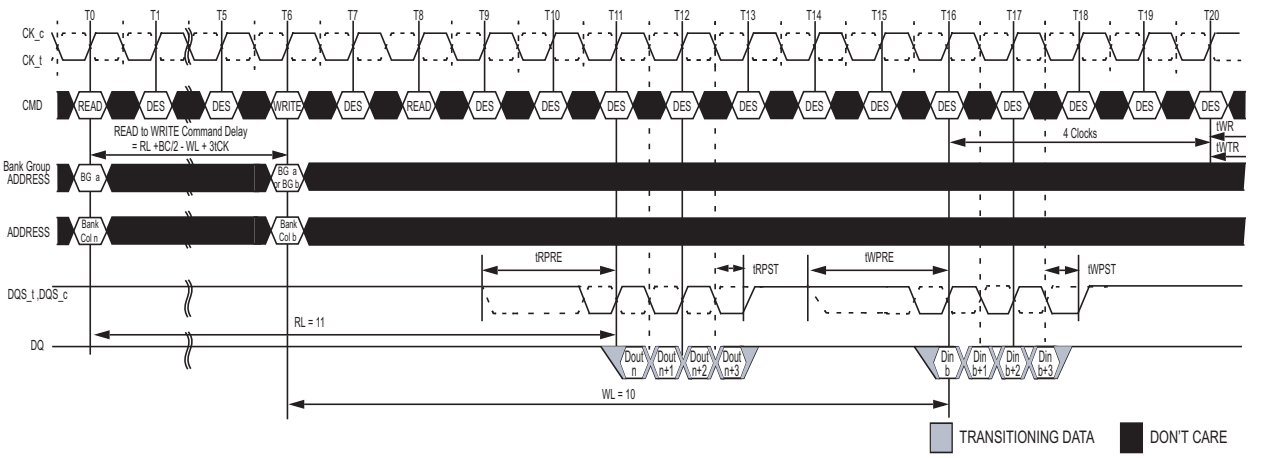
NOTE 2 DOUT n = data-out from column n, DIN b = data-in to column b.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4(OTF) setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0 and WRITE command at T6.

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

READ (BC4) OTF to WRITE (BC4) OTF with 2tCK Preamble in Same or Different Bank Group



NOTE 1 BC = 4, RL = 11 (CL = 11, AL = 0), Read Preamble = 2tCK, WL = 10 (CWL = 9+1[*5], AL = 0), Write Preamble = 2tCK

NOTE 2 DOUT n = data-out from column n, DIN b = data-in to column b.

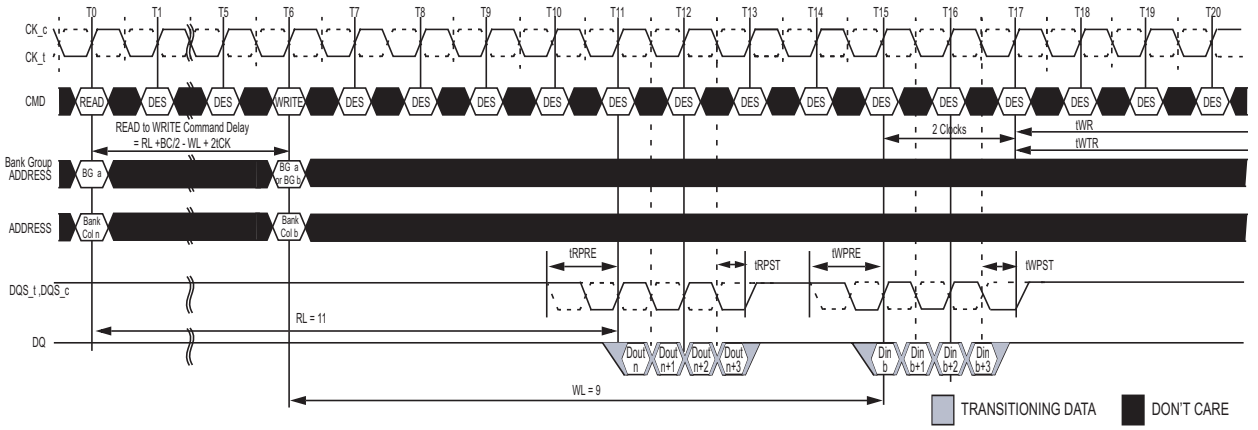
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4(OTF) setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0 and WRITE command at T6.

NOTE 5 When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting.

NOTE 6 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

READ (BC4) Fixed to WRITE (BC4) Fixed with 1tCK Preamble in Same or Different Bank Group



NOTE 1 BC = 4, RL = 11 (CL = 11, AL = 0), Read Preamble = 1tCK, WL = 9 (CWL = 9, AL = 0), Write Preamble = 1tCK

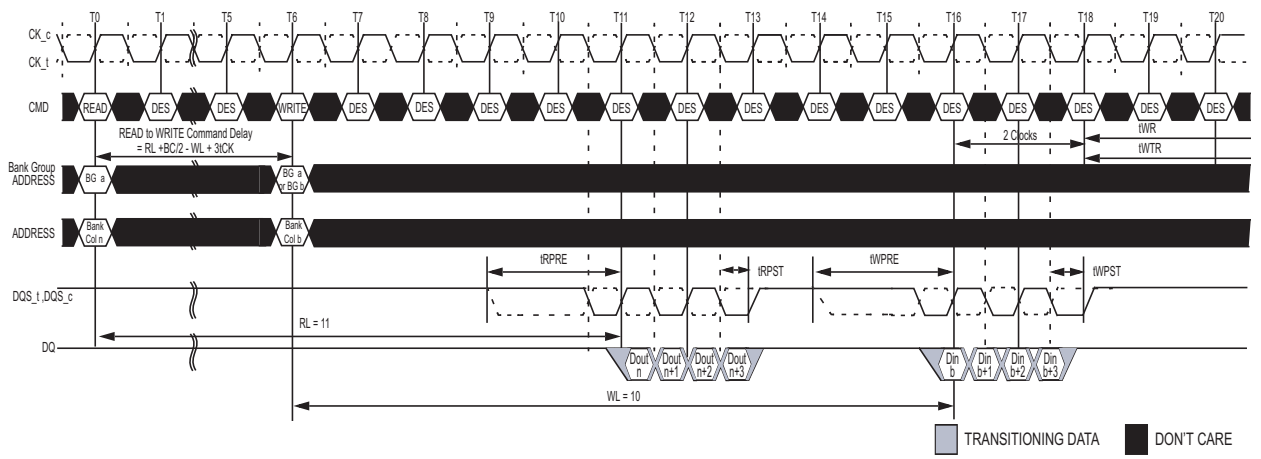
NOTE 2 DOUT n = data-out from column n, DIN b = data-in to column b.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4(Fixed) setting activated by MR0[A1:A0 = 1:0].

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

READ (BC4) Fixed to WRITE (BC4) Fixed with 1tCK Preamble in Same or Different Bank Group



NOTE 1 BC = 4, RL = 11 (CL = 11, AL = 0), Read Preamble = 2tCK, WL = 10 (CWL = 9+1[*5], AL = 0), Write Preamble = 2tCK

NOTE 2 DOUT n = data-out from column n, DIN b = data-in to column b.

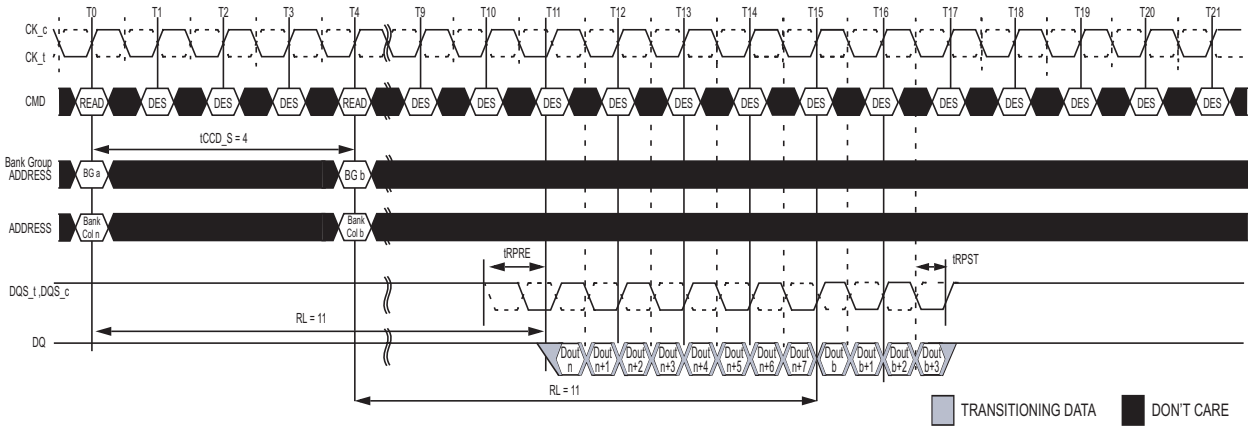
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4(Fixed) setting activated by MR0[A1:A0 = 1:0].

NOTE 5 When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting.

NOTE 6 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

READ (BL8) to READ (BC4) OTF with 1tCK Preamble in Different Bank Group



NOTE 1 BL = 8, AL =0, CL = 11 Preamble = 1tCK

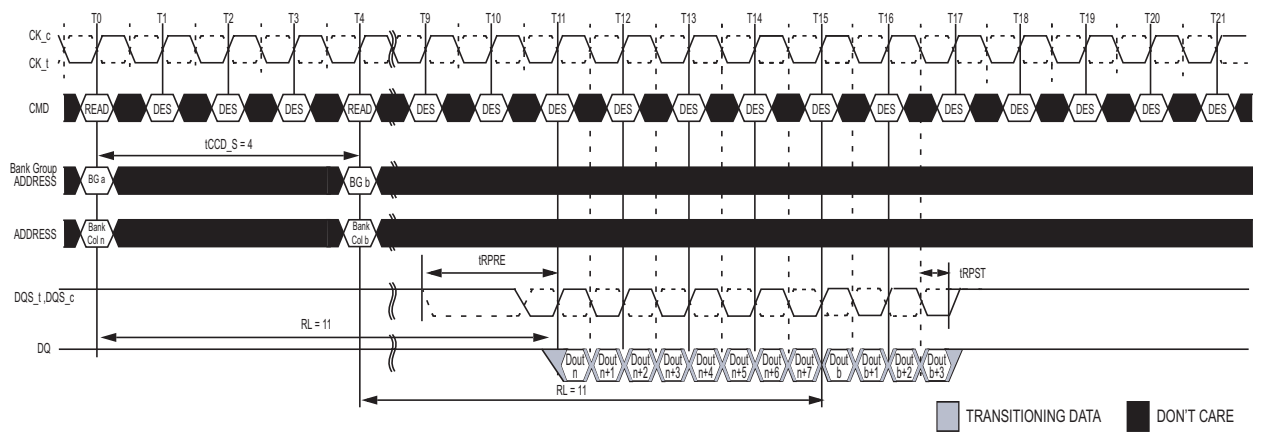
NOTE 2 DOUT n (or b) = data-out from column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T4.

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

READ (BL8) to READ (BC4) OTF with 2tCK Preamble in Different Bank Group



NOTE 1 BL = 8, AL =0, CL = 11 Preamble = 2tCK

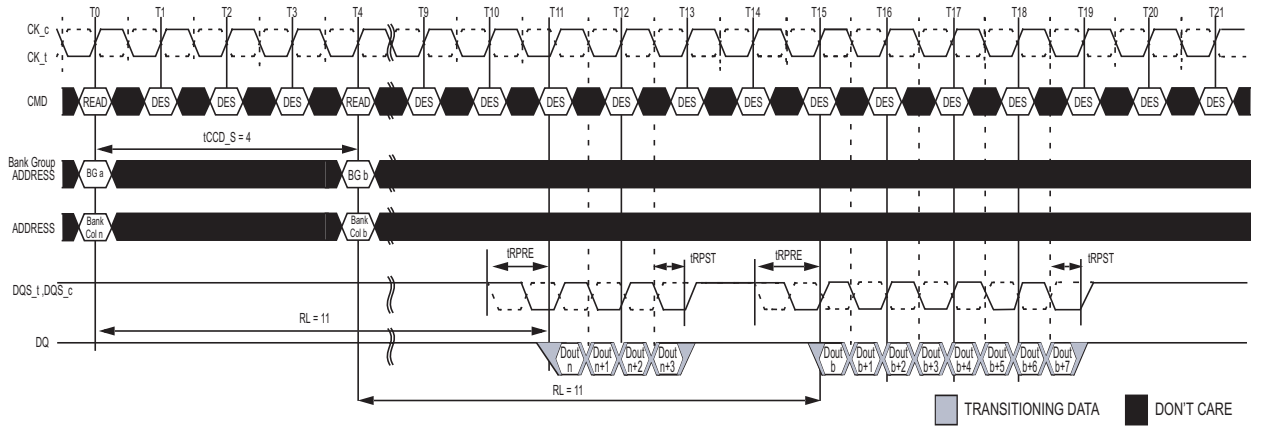
NOTE 2 DOUT n (or b) = data-out from column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T4.

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

READ (BC4) to READ (BL8) OTF with 1tCK Preamble in Different Bank Group



NOTE 1 BL = 8, AL =0, CL = 11 Preamble = 1tCK

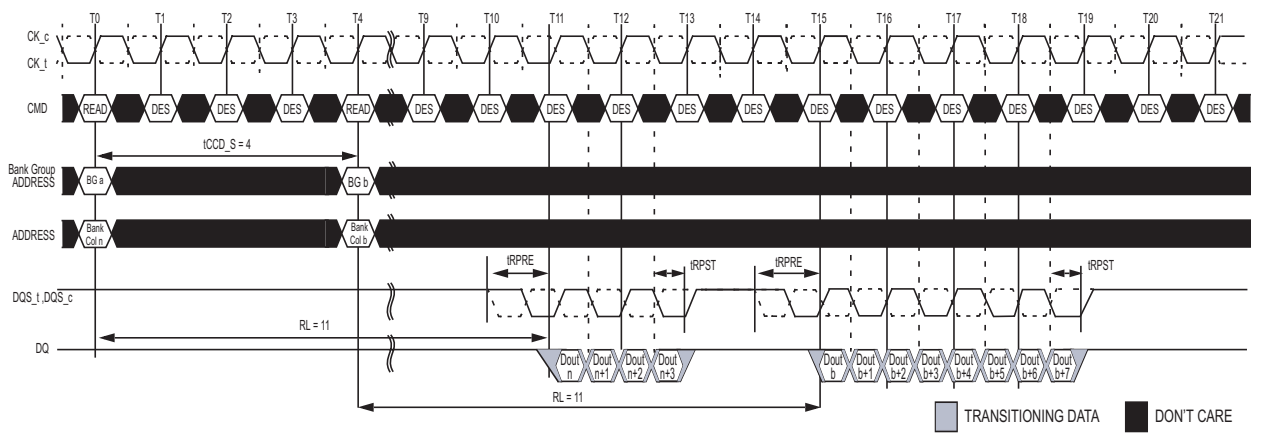
NOTE 2 DOUT n (or b) = data-out from column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0. BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T4.

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

READ (BC4) to READ (BL8) OTF with 2tCK Preamble in Different Bank Group



NOTE 1 BL = 8, AL =0, CL = 11 Preamble = 2tCK

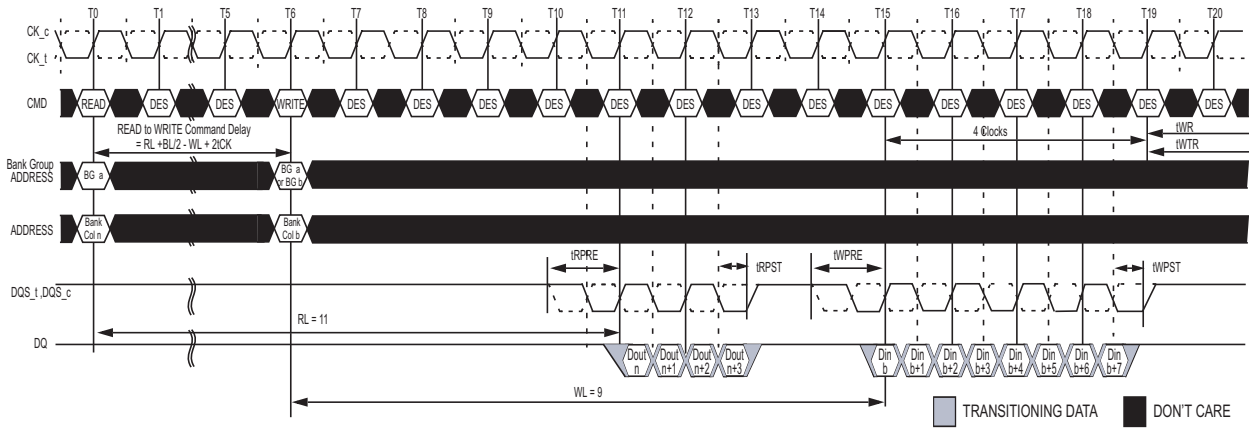
NOTE 2 DOUT n (or b) = data-out from column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0. BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T4.

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

READ (BC4) to WRITE (BL8) OTF with 1tCK Preamble in Same or Different Bank Group



NOTE 1 BC = 4, RL = 11(CL = 11, AL = 0), Read Preamble = 1tCK, WL=9(CWL=9,AL=0), Write Preamble = 1tCK

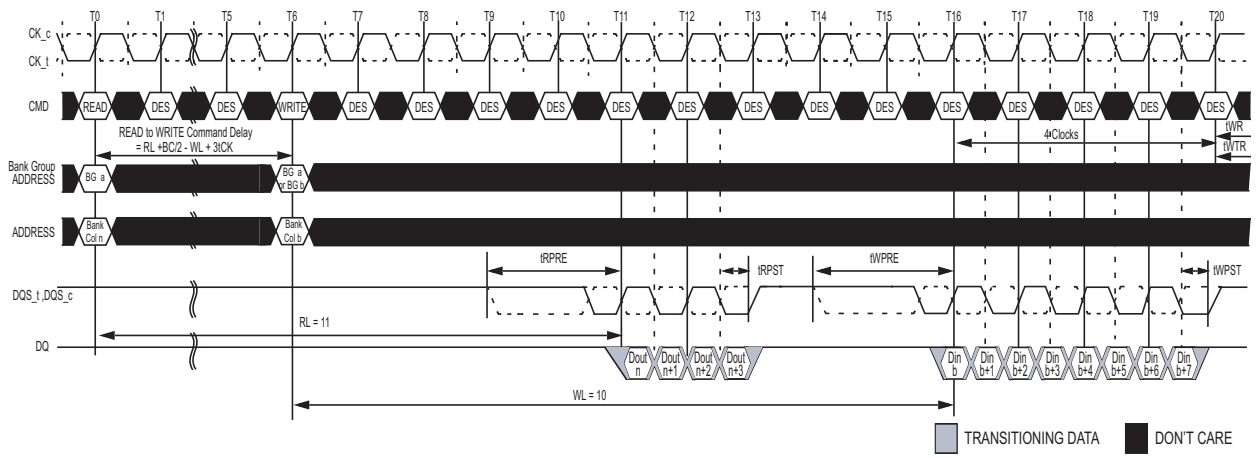
NOTE 2 DOUT n = data-out from column n, DIN b = data-in to column b.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0. BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T6.

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

READ (BC4) to WRITE (BL8) OTF with 2tCK Preamble in Same or Different Bank Group



NOTE 1 BC = 4, RL = 11 (CL = 11, AL = 0), Read Preamble = 2tCK, WL = 10 (CWL = 9+1[*5], AL = 0), Write Preamble = 2tCK

NOTE 2 DOUT n = data-out from column n, DIN b = data-in to column b.

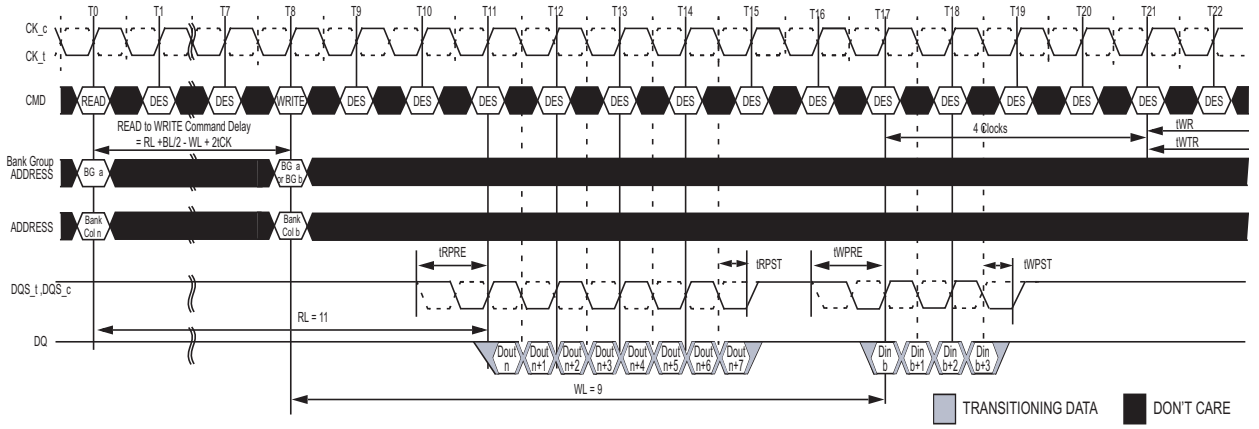
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0. BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T6.

NOTE 5 When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting.

NOTE 6 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

READ (BL8) to WRITE (BC4) OTF with 1tCK Preamble in Same or Different Bank Group



NOTE 1 BL = 8, RL = 11(CL = 11 , AL = 0), Read Preamble = 1tCK, WL=9(CWL=9,AL=0), Write Preamble = 1tCK

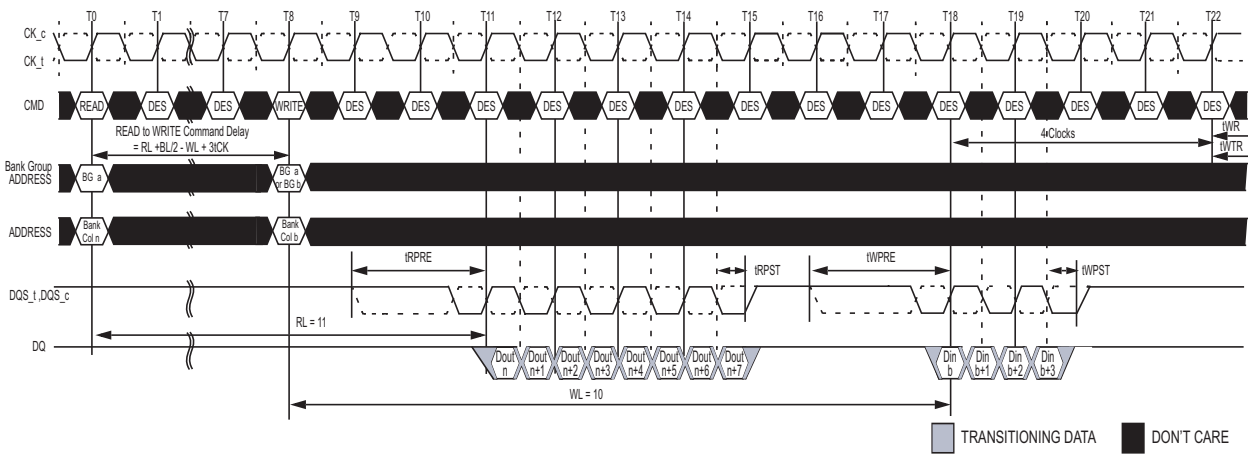
NOTE 2 DOUT n = data-out from column n, DIN b = data-in to column b.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T8.

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

READ (BL8) to WRITE (BC4) OTF with 2tCK Preamble in Same or Different Bank Group



NOTE 1 BL = 8, RL = 11 (CL = 11, AL = 0), Read Preamble = 2tCK, WL = 10 (CWL = 9+1[*5], AL = 0), Write Preamble = 2tCK

NOTE 2 DOUT n = data-out from column n, DIN b = data-in to column b.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T8.

NOTE 5 When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting.

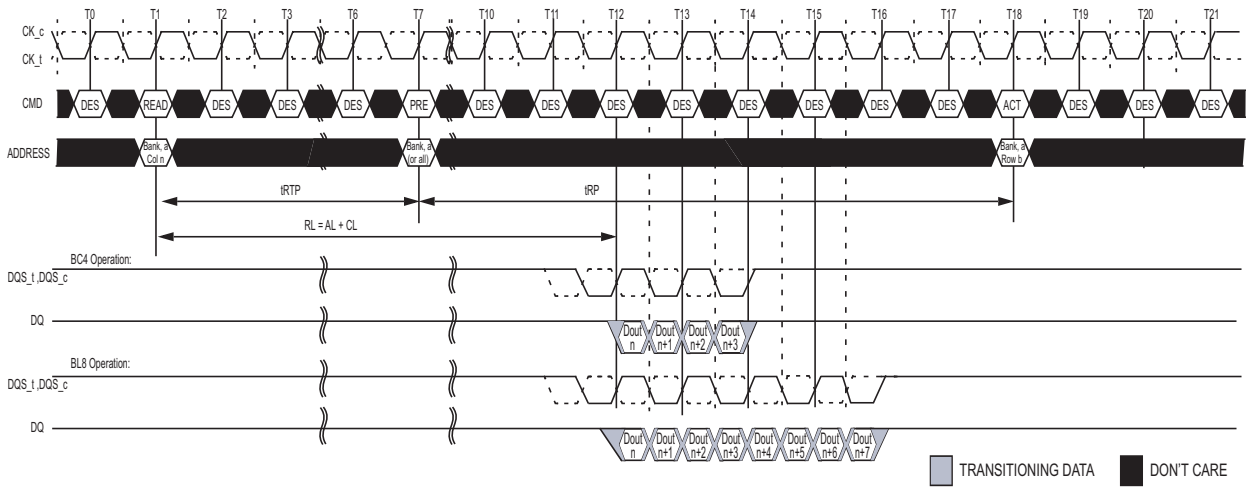
NOTE 6 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Burst Read Operation followed by a Precharge

The minimum external Read command to Precharge command spacing to the same bank is equal to AL + tRTP with tRTP being the Internal Read Command to Precharge Command Delay. Note that the minimum ACT to PRE timing, tRAS, must be satisfied as well. The minimum value for the Internal Read Command to Precharge Command Delay is given by tRTP.min, A new bank active command may be issued to the same bank if the following two conditions are satisfied simultaneously:

1. The minimum RAS precharge time (tRP.MIN) has been satisfied from the clock at which the precharge begins.
2. The minimum RAS cycle time (tRC.MIN) from the previous bank activation has been satisfied.

READ to PRECHARGE with 1tCK Preamble



NOTE 1 BL = 8, RL = 11(CL = 11, AL = 0), Preamble = 1tCK, tRTP = 6, tRP = 11

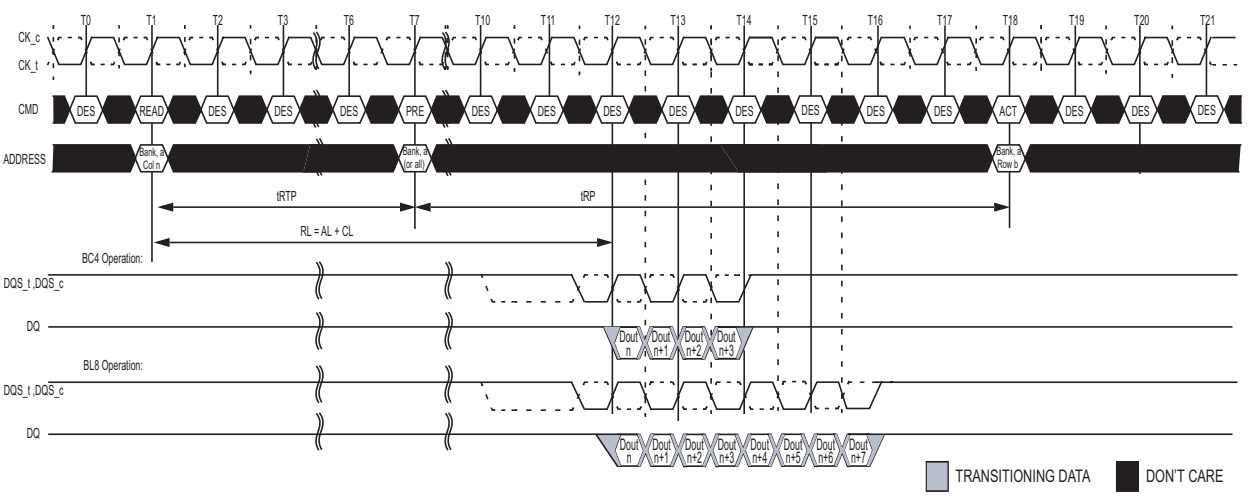
NOTE 2 DOUT n = data-out from column n.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 The example assumes tRAS. MIN is satisfied at Precharge command time(T7) and that tRC. MIN is satisfied at the next Active command time(T18).

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

READ to PRECHARGE with 2tCK Preamble



NOTE 1 BL = 8, RL = 11(CL = 11, AL = 0), Preamble = 2tCK, tRTP = 6, tRP = 11

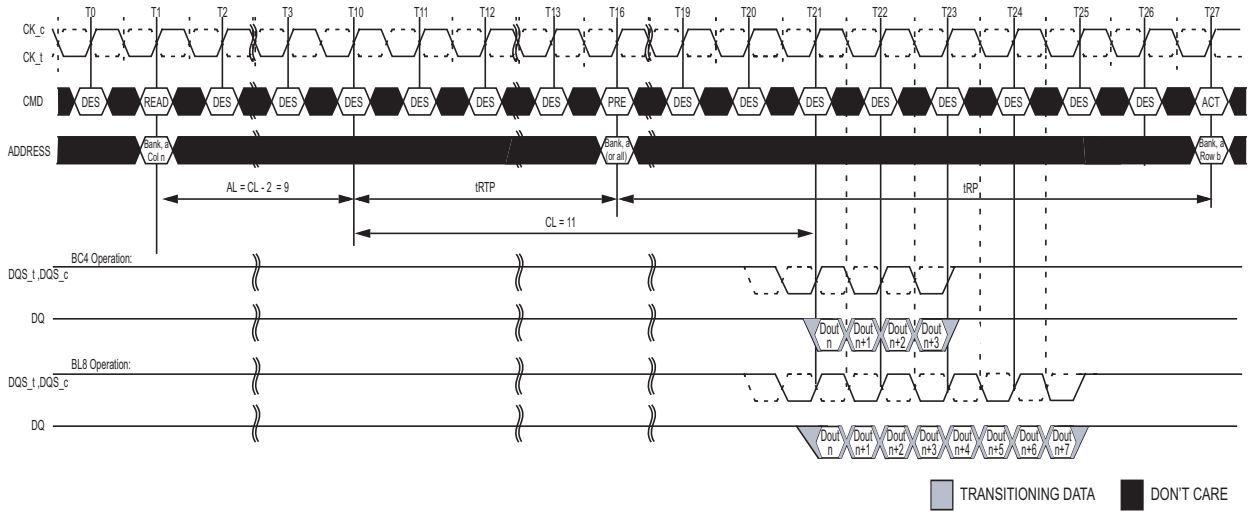
NOTE 2 DOUT n = data-out from column n.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 The example assumes tRAS. MIN is satisfied at Precharge command time(T7) and that tRC. MIN is satisfied at the next Active command time(T18).

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

READ to PRECHARGE with Additive Latency and 1tCK Preamble



NOTE 1 BL = 8, RL = 20 (CL = 11 , AL = CL- 2), Preamble = 1tCK, tRTP = 6, tRP = 11

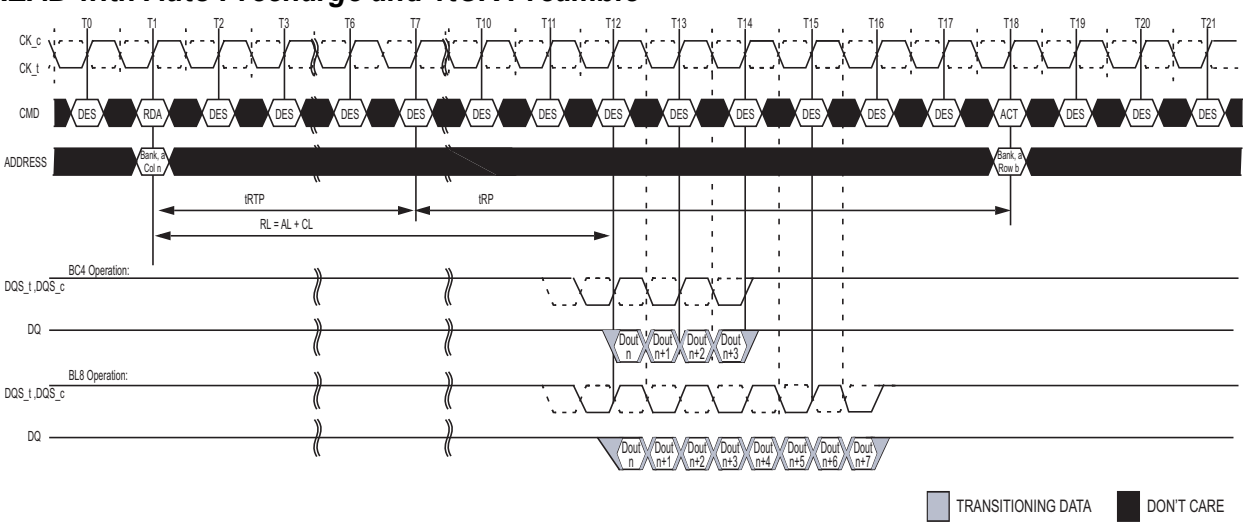
NOTE 2 DOUT n = data-out from column n.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 The example assumes tRAS. MIN is satisfied at Precharge command time(T16) and that tRC. MIN is satisfied at the next Active command time(T27).

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

READ with Auto Precharge and 1tCK Preamble



NOTE 1 BL = 8, RL = 11 (CL = 11 , AL = 0), Preamble = 1tCK, tRTP = 6, tRP = 11

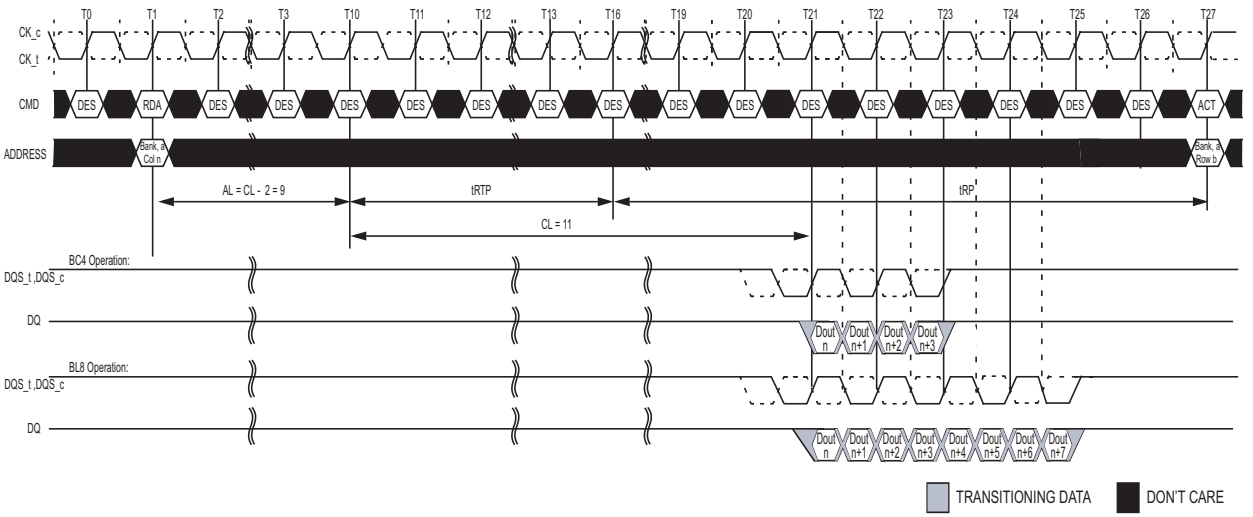
NOTE 2 DOUT n = data-out from column n.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 tRTP = 6 setting activated by MR0[A11:9 = 001]

NOTE 5 The example assumes tRC. MIN is satisfied at the next Active command time(T18).
NOTE 6 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

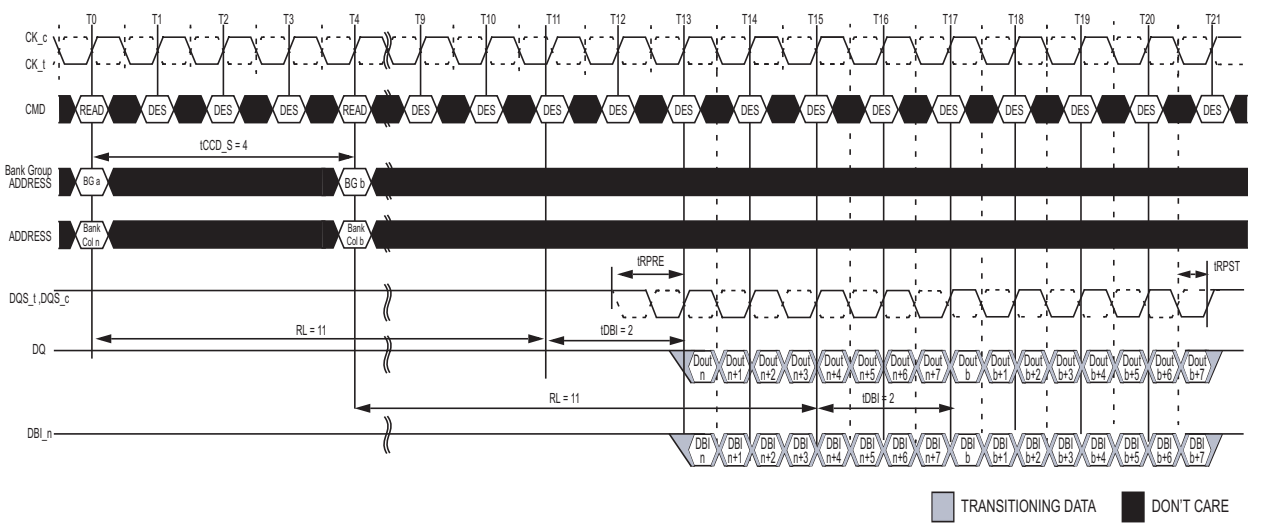
READ with Auto Precharge, Additive Latency and 1tCK Preamble



NOTE 1 BL = 8, RL = 20 (CL = 11, AL = CL- 2), Preamble = 1tCK, tRTP = 6, tRP = 11
NOTE 2 DOUT n = data-out from column n.
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.
NOTE 4 tRTP = 6 setting activated by MR0[A11:9 = 001]
NOTE 5 The example assumes tRC. MIN is satisfied at the next Active command time(T27).
NOTE 6 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

Burst Read Operation with Read DBI (Data Bus Inversion)

Consecutive READ (BL8) with 1tCK Preamble and DBI in Different Bank Group



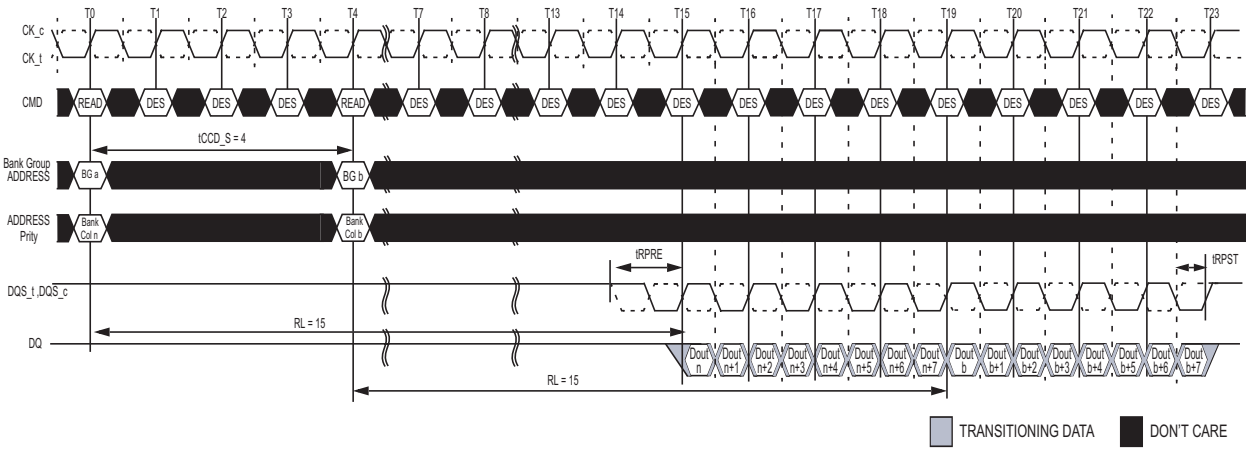
NOTE 1 BL = 8, AL = 0, CL = 11, Preamble = 1tCK, tDBI = 2tCK
NOTE 2 DOUT n (or b) = data-out from column n (or column b).
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:A0 = 00] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and T4.

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Enable.

Burst Read Operation with Command/Address Parity

Consecutive READ (BL8) with 1tCK Preamble and CA Parity in Different Bank Group



NOTE 1 BL = 8, AL = 0, CL = 11, PL = 4, (RL = CL + AL + PL = 15), Preamble = 1tCK

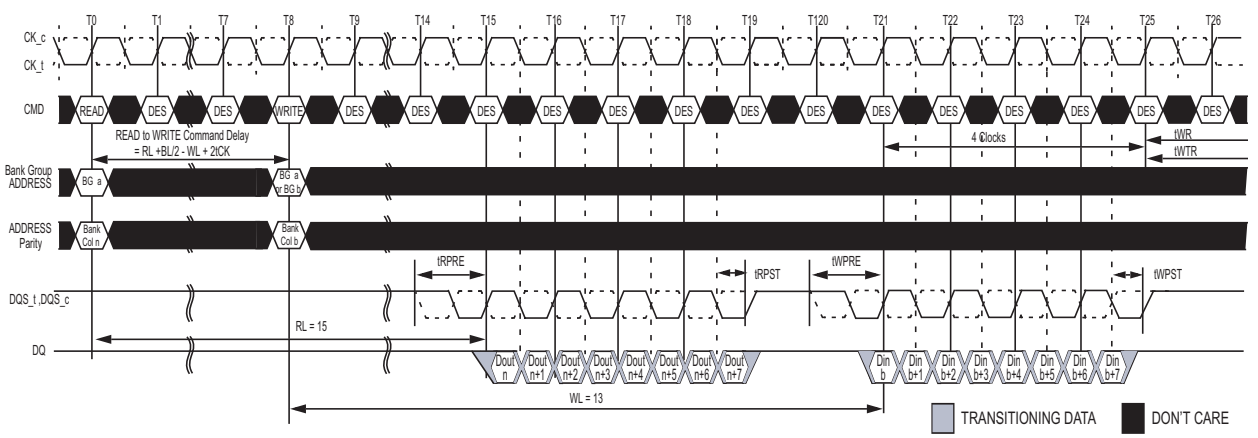
NOTE 2 DOUT n (or b) = data-out from column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and T4.

NOTE 5 CA Parity =Enable, CS to CA Latency = Disable, Read DBI = Disable.

READ (BL8) to WRITE (BL8) with 1tCK Preamble and CA parity in Same or Different Bank Group



NOTE 1 BL = 8, AL = 0, CL = 11, PL = 4, (RL = CL + AL + PL = 15), Read Preamble = 1tCK, CWL=9, AL=0, PL=4, (WL=CL+AL+PL=13), Write Preamble = 1tCK

NOTE 2 DOUT n (or b) = data-out from column n (or column b).

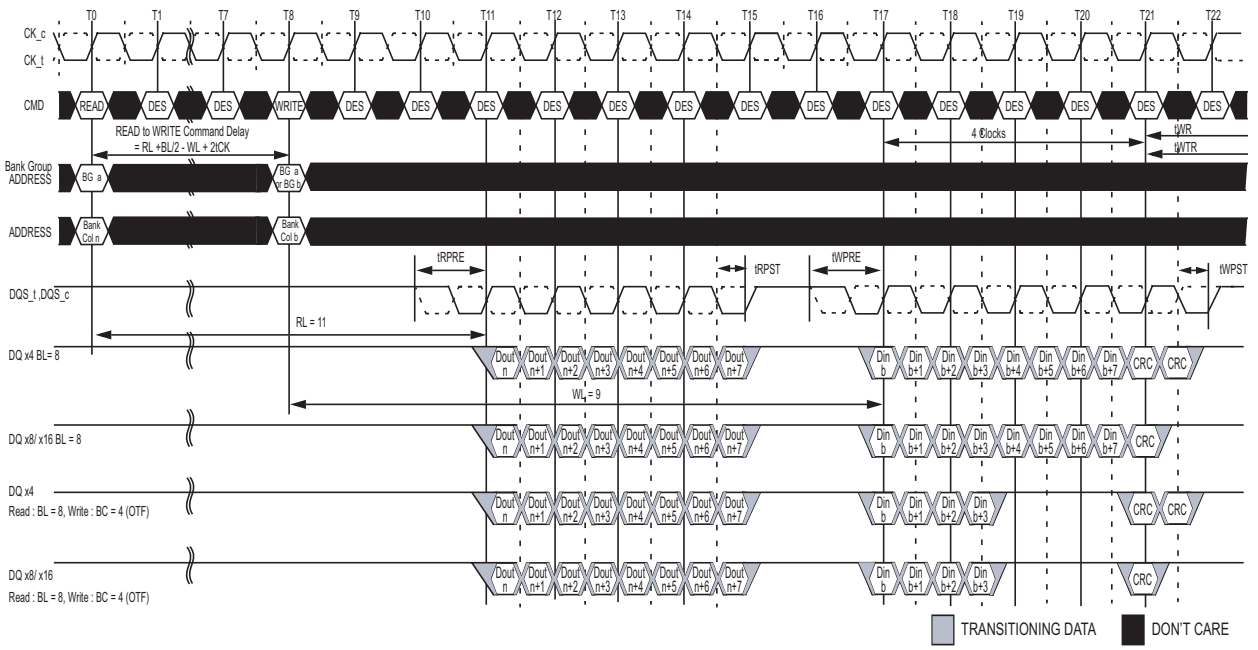
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and Write command at T8.

NOTE 5 CA Parity = Enable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Read to Write with Write CRC

READ (BL8) to WRITE (BL8 or BC4:OTF) with 1tCK Preamble and Write CRC in Same or Different Bank Group



NOTE 1 BL = 8 (or BC = 4 : OTF for Write), RL = 11 (CL = 11, AL = 0), Read Preamble = 1tCK, WL=9 (CWL=9, AL=0), Write Preamble = 1tCK

NOTE 2 DOUT n = data-out from column n . DIN b = data-in to column b.

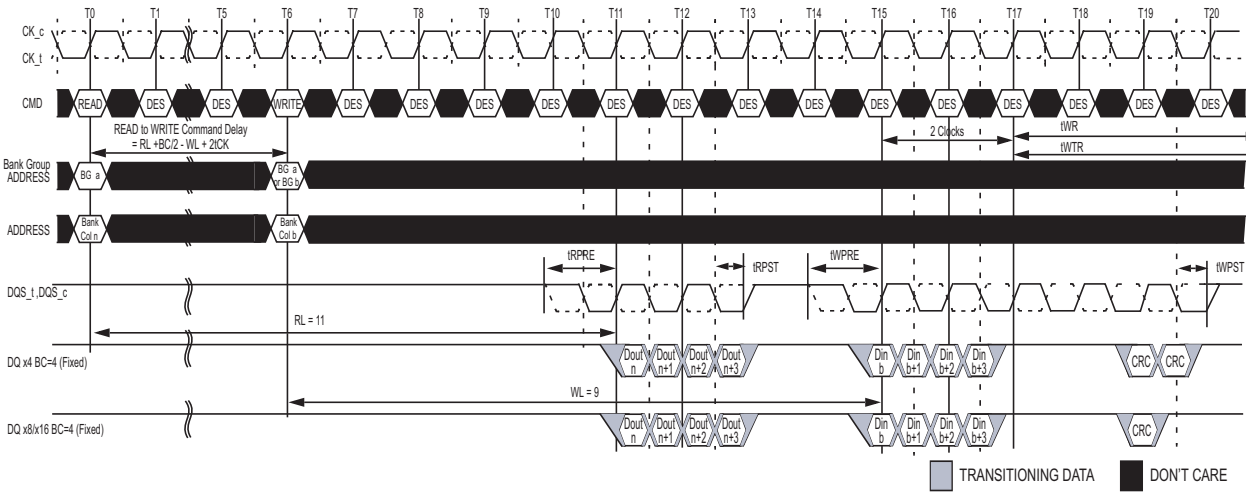
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and Write command at T8.

NOTE 5 BC4 setting activated by MR0[A1:0 = 01] and A12 = 0 during Write command at T8.

NOTE 6 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Enable.

READ (BC4:Fixed) to WRITE (BC4:Fixed) with 1tCK Preamble and Write CRC in Same or Different Bank Group



NOTE 1 BC = 4 (Fixed), RL = 11 (CL = 11, AL = 0), Read Preamble = 1tCK, WL=9 (CWL=9, AL=0), Write Preamble = 1tCK

NOTE 2 DOUT n = data-out from column n . DIN b = data-in to column b.

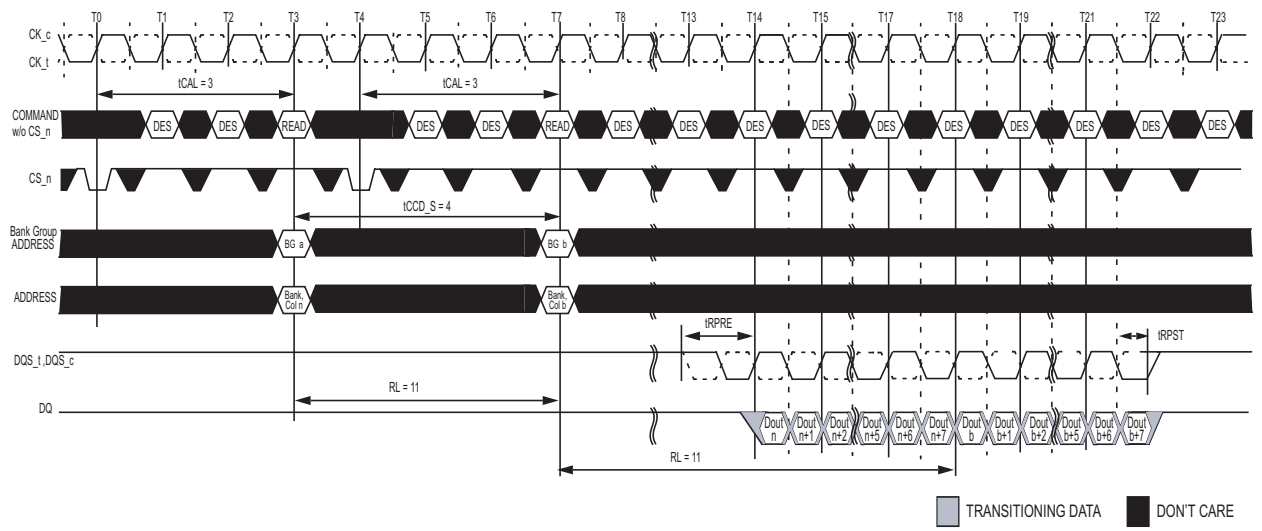
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0[A1:A0 = 1:0]

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Enable.

Read to Read with CS to CA Latency

Consecutive READ (BL8) with CAL(3) and 1tCK Preamble in Different Bank Group



NOTE 1 BL = 8 ,AL = 0, CL = 11, CAL = 3, Preamble = 1tCK

NOTE 2 DOUT n (or b) = data-out from column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

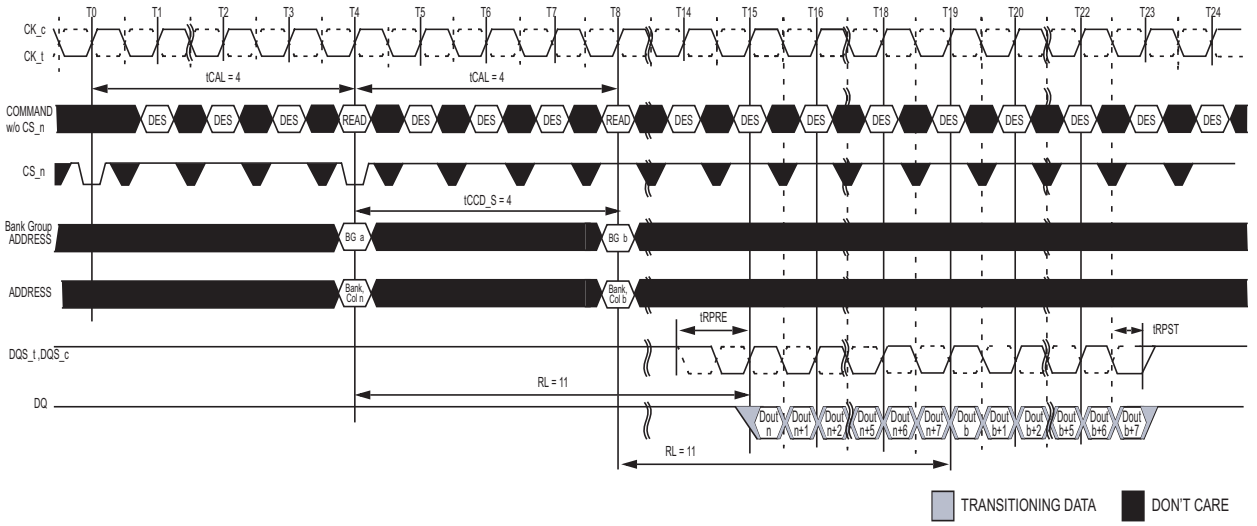
NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at

T3 and T7.

NOTE 5 CA Parity = Disable, CS to CA Latency = Enable, Read DBI = Disable.

NOTE 6 Enabling of CAL mode does not impact ODT control timings. Users should maintain the same timing relationship relative to the command/address bus as when CAL is disabled.

Consecutive READ (BL8) with CAL(4) and 1tCK Preamble in Different Bank Group



NOTE 1 BL = 8 ,AL = 0, CL = 11, CAL = 4, Preamble = 1tCK

NOTE 2 DOUT n (or b) = data-out from column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T4 and T8.

NOTE 5 CA Parity = Disable, CS to CA Latency = Enable, Read DBI = Disable.

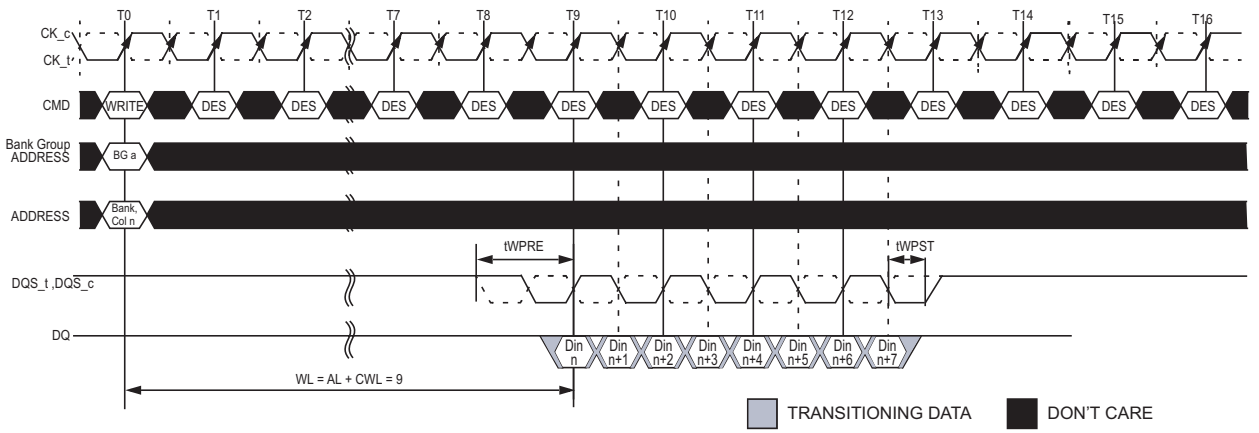
NOTE 6 EEnabling of CAL mode does not impact ODT control timings. Users should maintain the same timing relationship relative to the command/address bus as when CAL is disabled.

Write Operation

Write Burst Operation

The following write timing diagram is to help understanding of each write parameter's meaning and just examples. The details of the definition of each parameter will be defined separately.
In these write timing diagram, CK and DQS are shown aligned and also DQS and DQ are shown center aligned for illustration purpose.

WRITE Burst Operation WL = 9 (AL = 0, CWL = 9, BL8)



NOTE 1 BL = 8 ,WL = 9, AL = 0, CWL = 9, Preamble = 1tCK

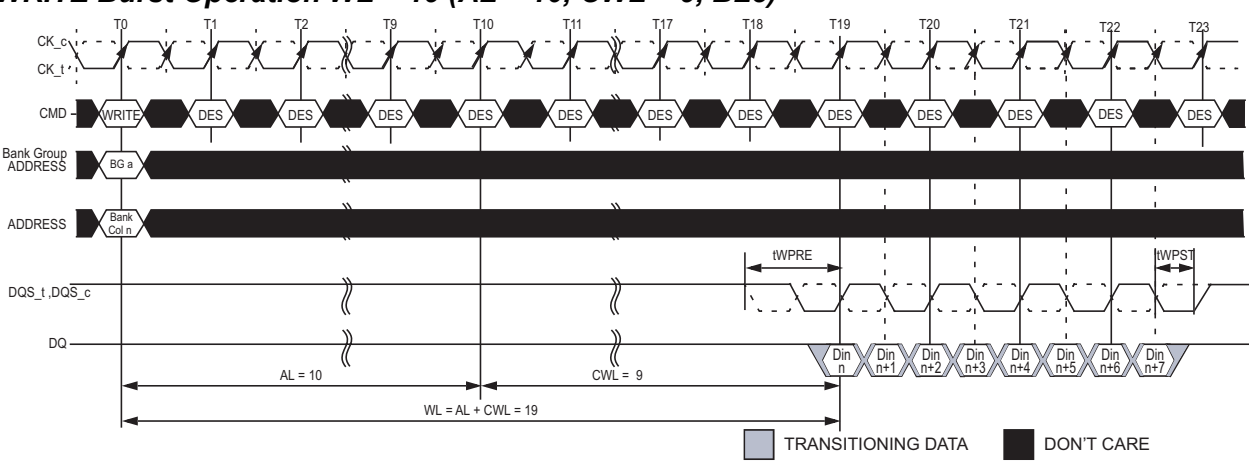
NOTE 2 DIN n = data-in to column n.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0.

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

WRITE Burst Operation WL = 19 (AL = 10, CWL = 9, BL8)



NOTE 1 BL = 8 ,WL = 19, AL = 10 (CL-1), CWL = 9, Preamble = 1tCK

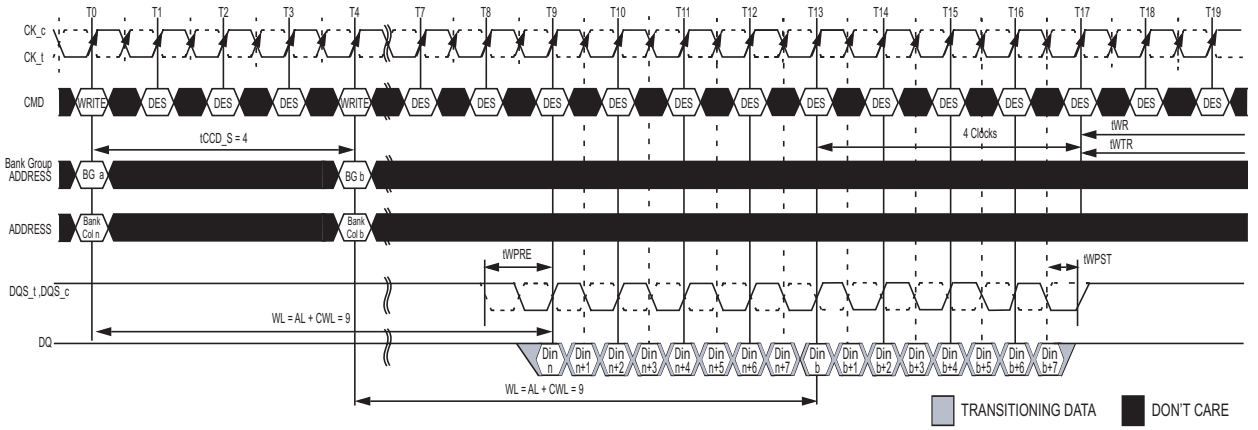
NOTE 2 DIN n = data-in to column n.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0.

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

Consecutive WRITE (BL8) with 1tCK Preamble in Different Bank Group



NOTE 1 BL = 8, AL = 0, CWL = 9, Preamble = 1tCK

NOTE 2 DIN n (or b) = data-in to column n (or column b).

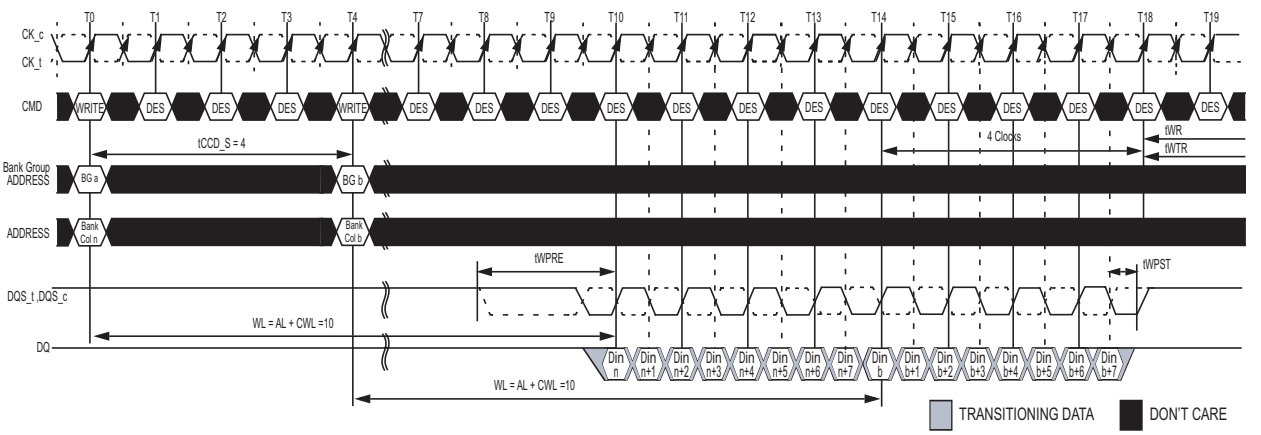
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0 and T4.

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

NOTE 6 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17.

Consecutive WRITE (BL8) with 2tCK Preamble in Different Bank Group



NOTE 1 BL = 8 ,AL = 0, CWL = 9 + 1 = 10[7], Preamble = 2tCK

NOTE 2 DIN n (or b) = data-in to column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

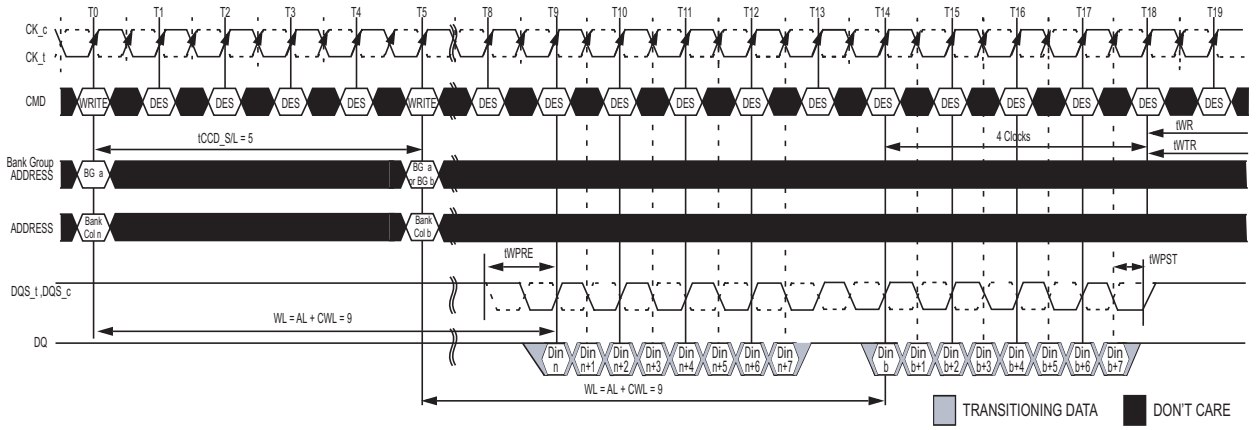
NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0 and T4.

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

NOTE 6 The write recovery time(tWR) and write timing parameter(tWTR) are referenced from the first rising clock edge after the last write data shown at T18.

NOTE 7 When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supportedin the applicable tCK range. That means CWL = 9 is not allowed when operating in 2tCK Write Preamble Mode.

Nonconsecutive WRITE (BL8) with 1tCK Preamble in Same or Different Bank Group



NOTE 1 BL = 8 ,AL = 0, CWL = 9 , Preamble = 1tCK, tCCD_S/L = 5

NOTE 2 DIN n (or b) = data-in to column n (or column b).

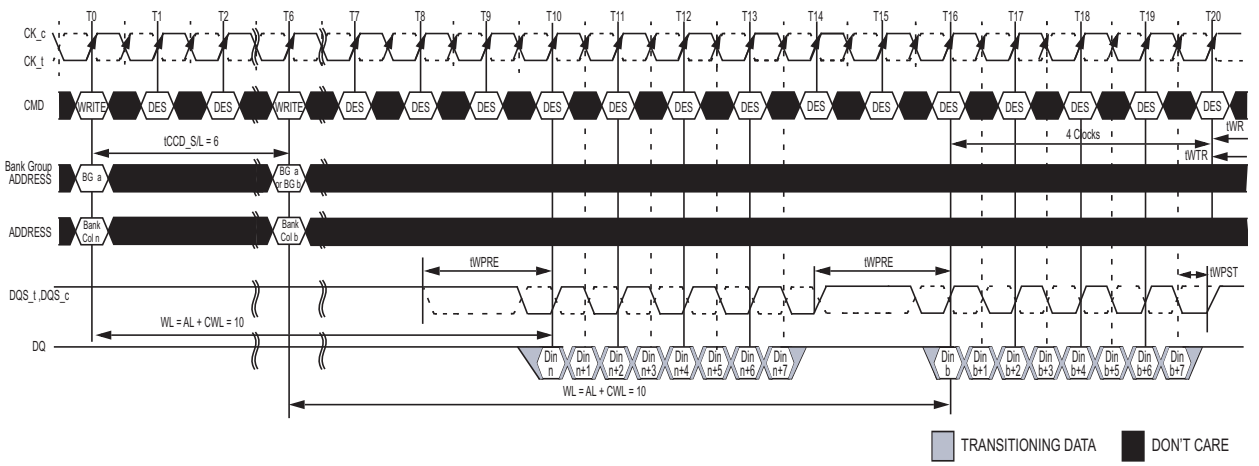
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0 and T5.

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

NOTE 6 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T18.

Nonconsecutive WRITE (BL8) with 2tCK Preamble in Same or Different Bank Group



NOTE 1 BL = 8 ,AL = 0, CWL = 9 + 1 = 10[8] , Preamble = 2tCK, tCCD_S/L = 6

NOTE 2 DIN n (or b) = data-in to column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0 and T6.

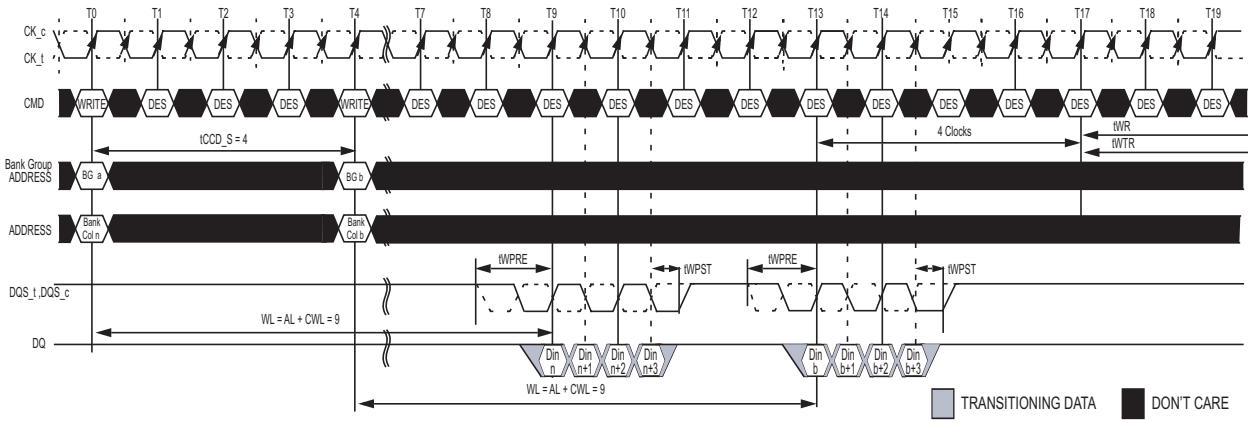
NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

NOTE 6 tCCD_S/L=5 isn't allowed in 2tCK preamble mode.

NOTE 7 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T20.

NOTE 8 When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range.That means CWL = 9 is not allowed when operating in 2tCK Write Preamble Mode.

WRITE (BC4) OTF to WRITE (BC4) OTF with 1tCK Preamble in Different Bank Group



NOTE 1 BC = 4, AL = 0, CWL = 9 , Preamble = 1tCK

NOTE 2 DIN n (or b) = data-in to column n (or column b).

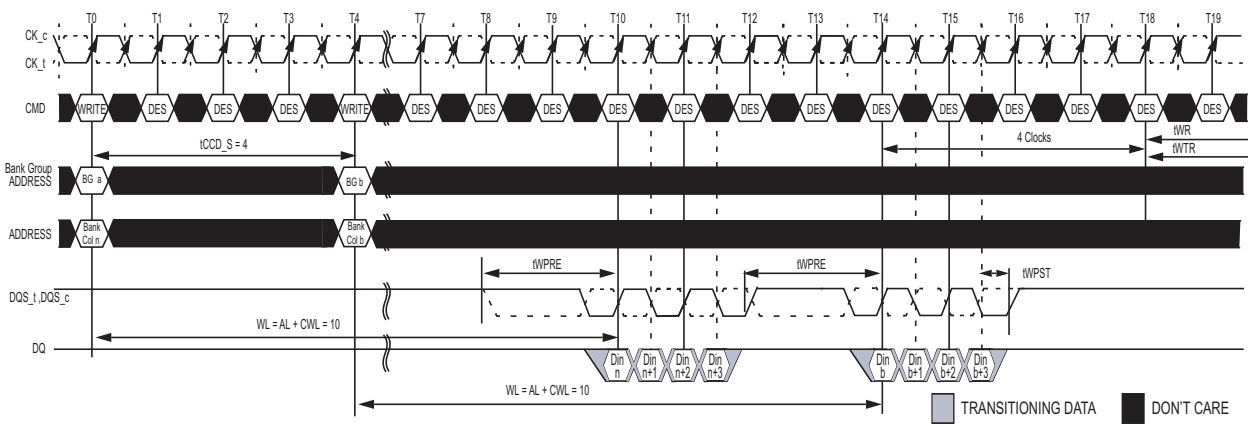
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T0 and T4.

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

NOTE 6 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17.

WRITE (BC4) OTF to WRITE (BC4) OTF with 2tCK Preamble in Different Bank Group



NOTE 1 BC = 4, AL = 0, CWL = 9 + 1 = 10^{7} , Preamble = 2tCK

NOTE 2 DIN n (or b) = data-in to column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

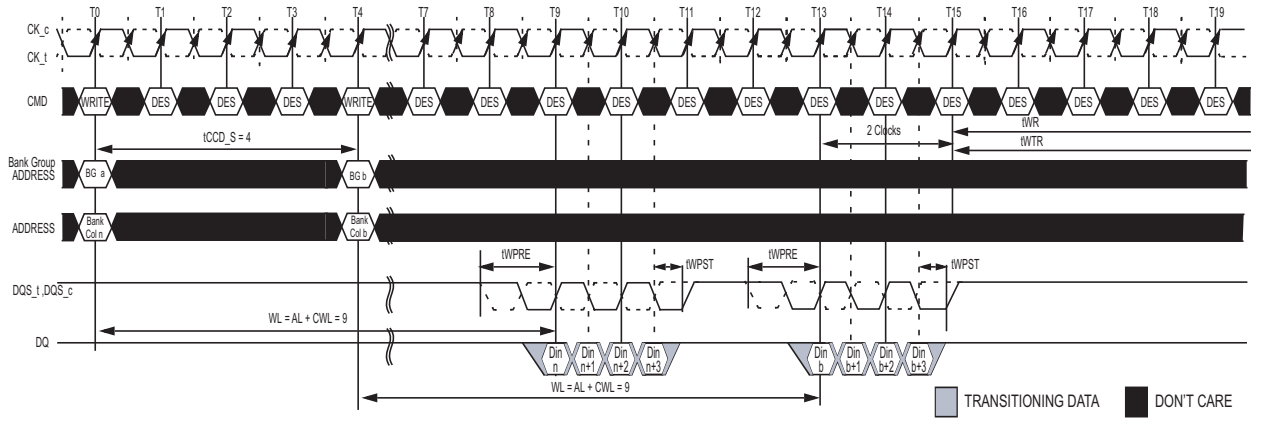
NOTE 4 BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T0 and T4.

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

NOTE 6 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T18.

NOTE 7 When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range.That means CWL = 9 is not allowed when operating in 2tCK Write Preamble Mode.

WRITE (BC4) Fixed to WRITE (BC4) Fixed with 1tCK Preamble in Different Bank Group



NOTE 1 BC = 4, AL = 0, CWL = 9 , Preamble = 1tCK

NOTE 2 DIN n (or b) = data-in to column n (or column b).

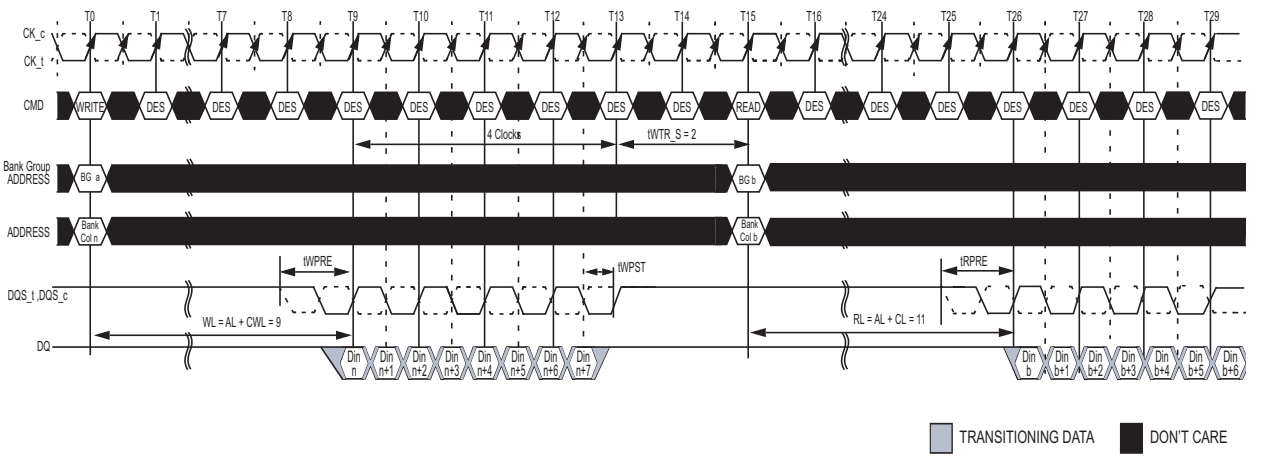
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0[A1:A0 = 1:0].

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

NOTE 6 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T15.

WRITE (BL8) to READ (BL8) with 1tCK Preamble in Different Bank Group



NOTE 1 BL = 8, AL = 0, CWL = 9, CL = 11, Preamble = 1tCK

NOTE 2 DIN n (or b) = data-in to column n (or column b).

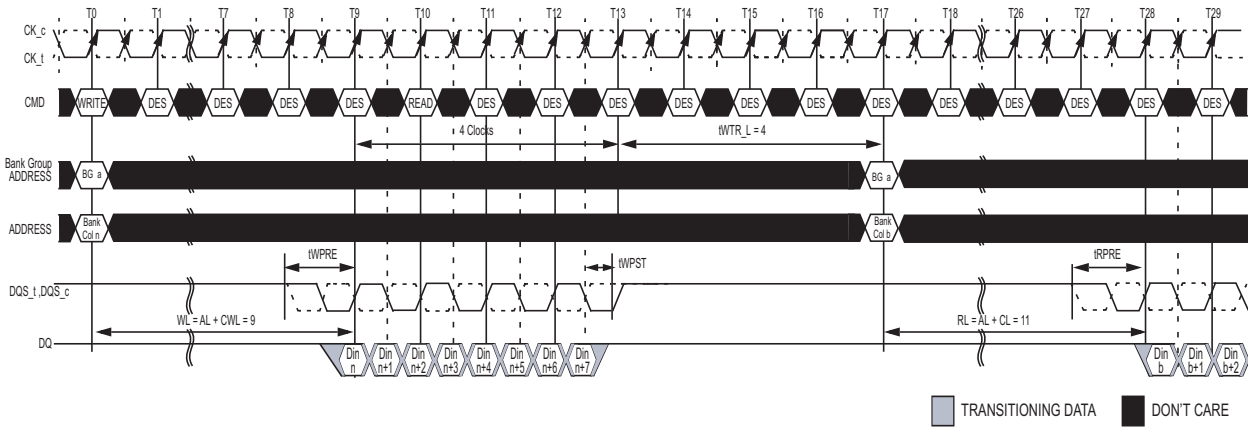
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0 and READ command at T15.

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

NOTE 6 The write timing parameter (tWTR_S) are referenced from the first rising clock edge after the last write data shown at T13.

WRITE (BL8) to READ (BL8) with 1tCK Preamble in Same Bank Group



NOTE 1 BL = 8, AL = 0, CWL = 9, CL = 11, Preamble = 1tCK

NOTE 2 DIN n = data-in to column n (or column b). DOUT b = data-out from column b.

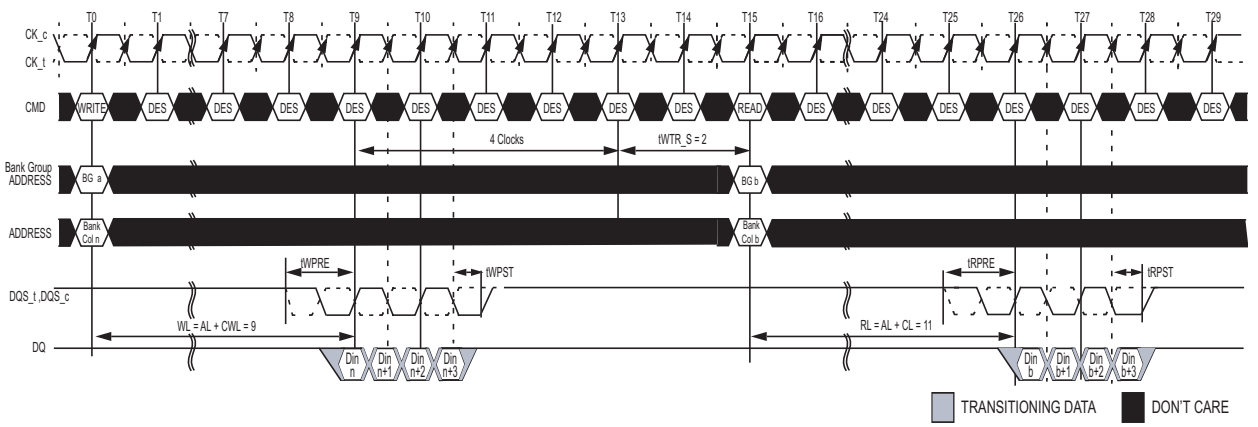
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0 and READ command at T17.

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

NOTE 6 The write timing parameter (tWTR_L) are referenced from the first rising clock edge after the last write data shown at T13.

WRITE (BC4)OTF to READ (BC4)OTF with 1tCK Preamble in Different Bank Group



NOTE 1 BC = 4, AL = 0, CWL = 9, CL = 11, Preamble = 1tCK

NOTE 2 DIN n = data-in to column n (or column b). DOUT b = data-out from column b.

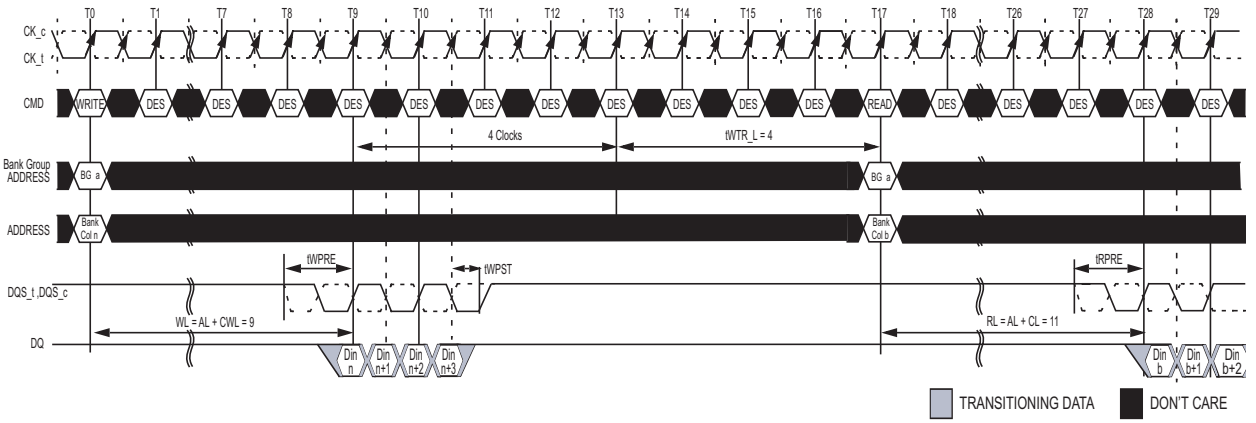
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T0 and READ command at T15.

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

NOTE 6 The write timing parameter (tWTR_S) are referenced from the first rising clock edge after the last write data shown at T13.

WRITE (BC4)OTF to READ (BC4)OTF with 1tCK Preamble in Same Bank Group



NOTE 1 BC = 4, AL = 0, CWL = 9, CL = 11, Preamble = 1tCK

NOTE 2 DIN n = data-in to column n (or column b). DOUT b = data-out from column b.

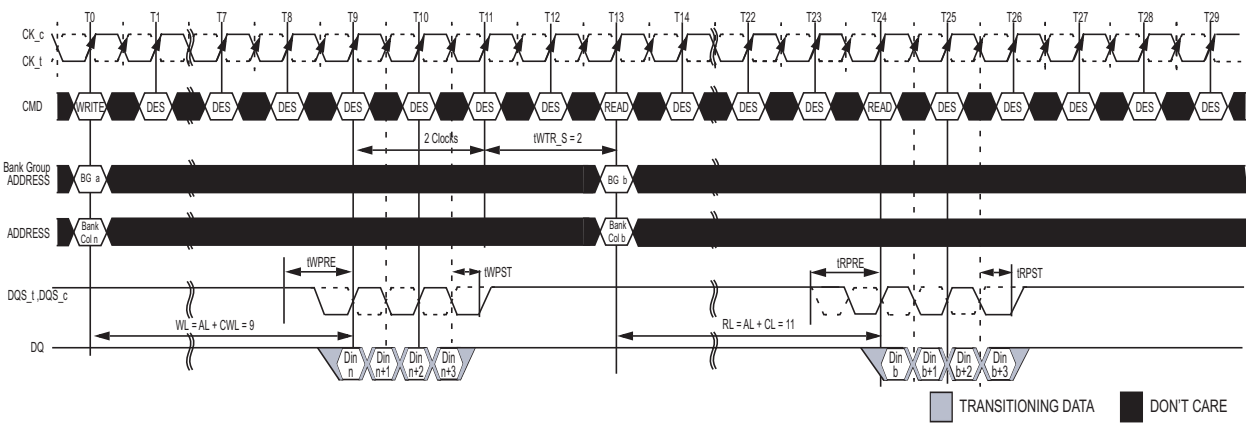
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T0 and READ command at T17.

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

NOTE 6 The write timing parameter (tWTR_L) are referenced from the first rising clock edge after the last write data shown at T13.

WRITE (BC4)Fixed to READ (BC4)Fixed with 1tCK Preamble in Different Bank Group



NOTE 1 BC = 4, AL = 0, CWL = 9, CL = 11, Preamble = 1tCK

NOTE 2 DIN n = data-in to column n (or column b). DOUT b = data-out from column b.

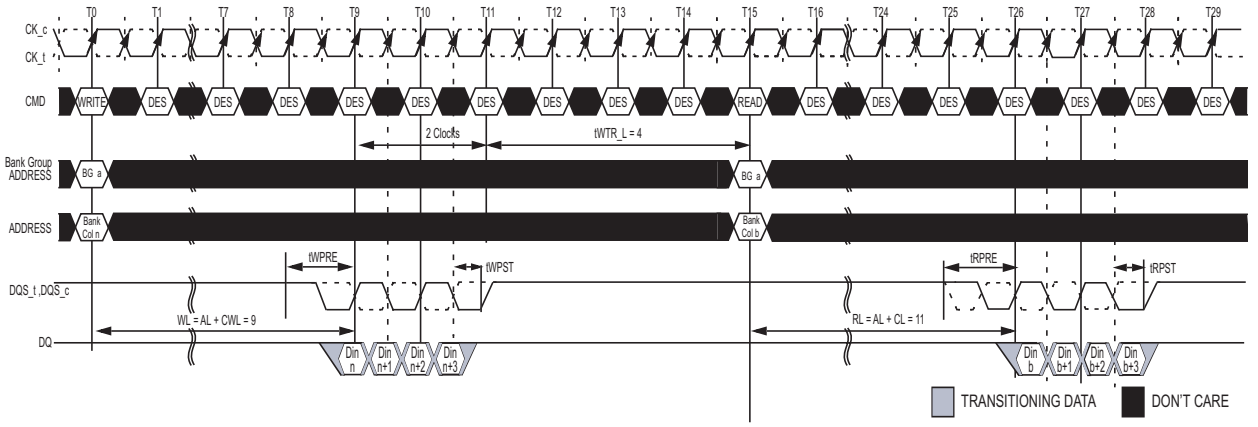
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0[A1:A0 = 1:0].

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

NOTE 6 The write timing parameter (tWTR_S) are referenced from the first rising clock edge after the last write data shown at T11.

WRITE (BC4)Fixed to READ (BC4)Fixed with 1tCK Preamble in Same Bank Group



NOTE 1 BC = 4, AL = 0, CWL = 9, CL = 11, Preamble = 1tCK

NOTE 2 DIN n = data-in to column n (or column b). DOUT b = data-out from column b.

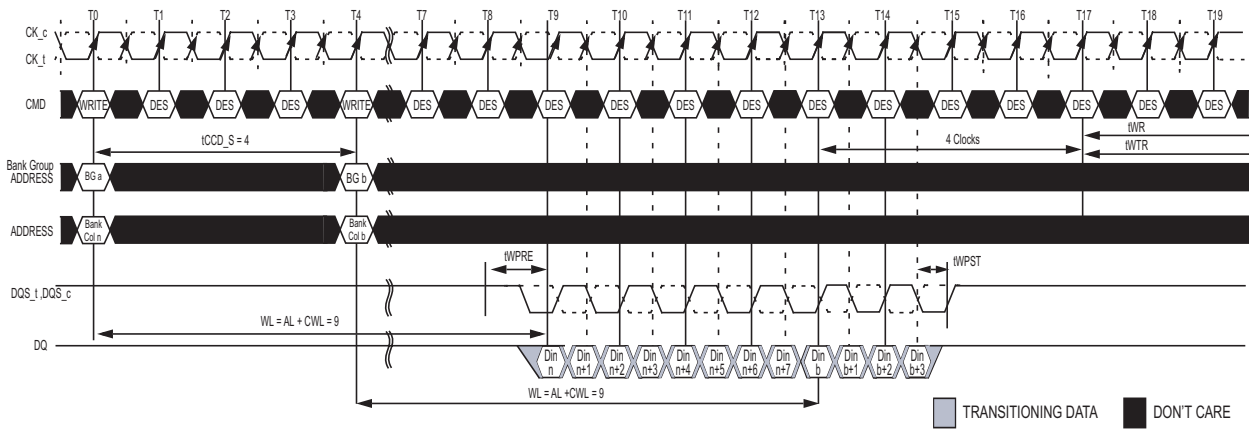
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0[A1:A0 = 1:0].

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

NOTE 6 The write timing parameter (tWTR_L) are referenced from the first rising clock edge after the last write data shown at T11.

WRITE (BL8) to WRITE (BC4) OTF with 1tCK Preamble in Different Bank Group



NOTE 1 BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble = 1tCK

NOTE 2 DIN n = data-in to column n (or column b). DOUT b = data-out from column b.

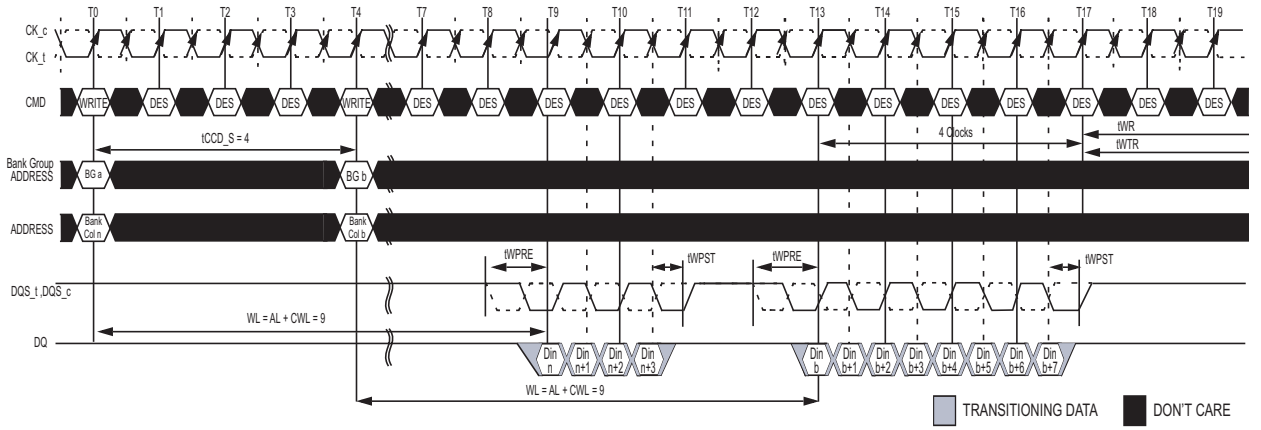
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by MR0[A1:A0 = 0:1] and A12 =1 during WRITE command at T0. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 =0 during WRITE command at T4.

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

NOTE 6 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17.

WRITE (BC4)OTF to WRITE (BL8) with 1tCK Preamble in Different Bank Group



NOTE 1 BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble = 1tCK

NOTE 2 DIN n (or b) = data-in to column n (or column b).

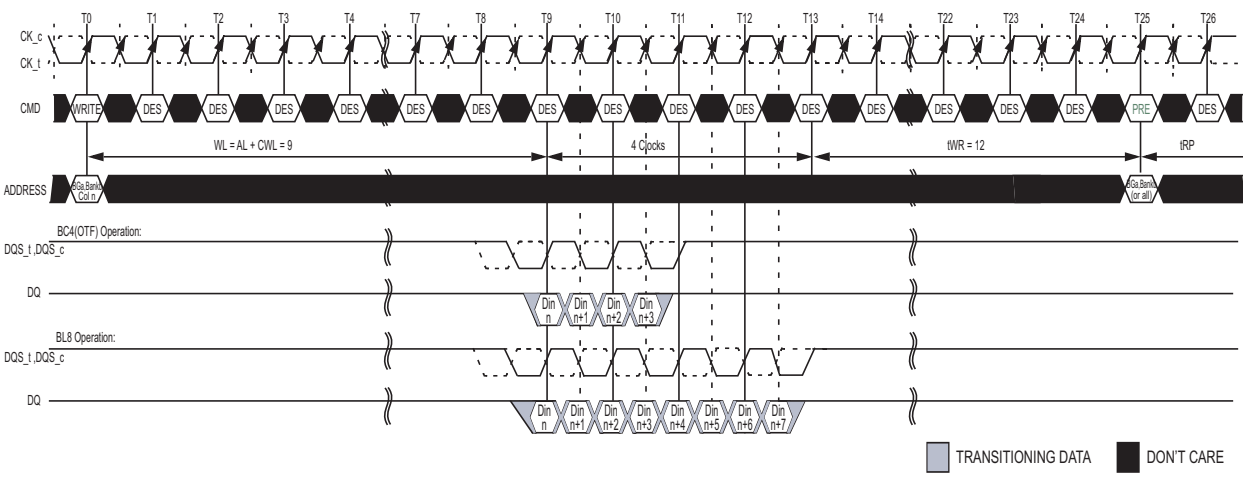
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0[A1:A0 = 0:1] and A12 =0 during WRITE command at T0. BL8 setting activated by MR0[A1:A0 = 0:1] and A12 =1 during WRITE command at T4.

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

NOTE 6 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17.

WRITE (BL8/BC4) OTF to PRECHARGE Operation with 1tCK Preamble



NOTE 1 BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble = 1tCK, tWR = 12

NOTE 2 DIN n = data-in to column n.

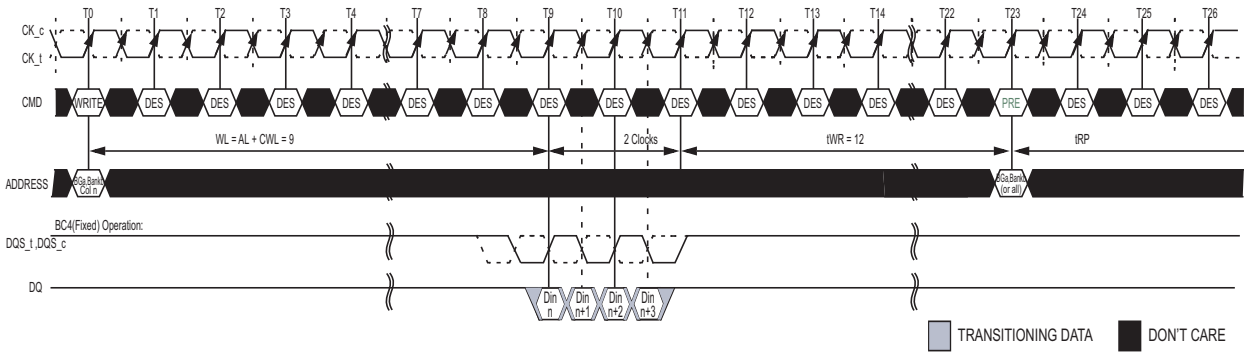
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0[A1:A0 = 0:1] and A12 =0 during WRITE command at T0. BL8 setting activated by MR0[A1:A0 = 0:0] or MR0[A1:0 = 01] and A12 =1 during WRITE command at T0.

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

NOTE 6 The write recovery time (tWR) is referenced from the first rising clock edge after the last write data shown at T13. tWR specifies the last burst write cycle until the precharge command can be issued to the same bank.

WRITE (BC4) Fixed to PRECHARGE Operation with 1tCK Preamble



NOTE 1 BC = 4, AL = 0, CWL = 9, Preamble = 1tCK, tWR = 12

NOTE 2 DIN n = data-in to column n.

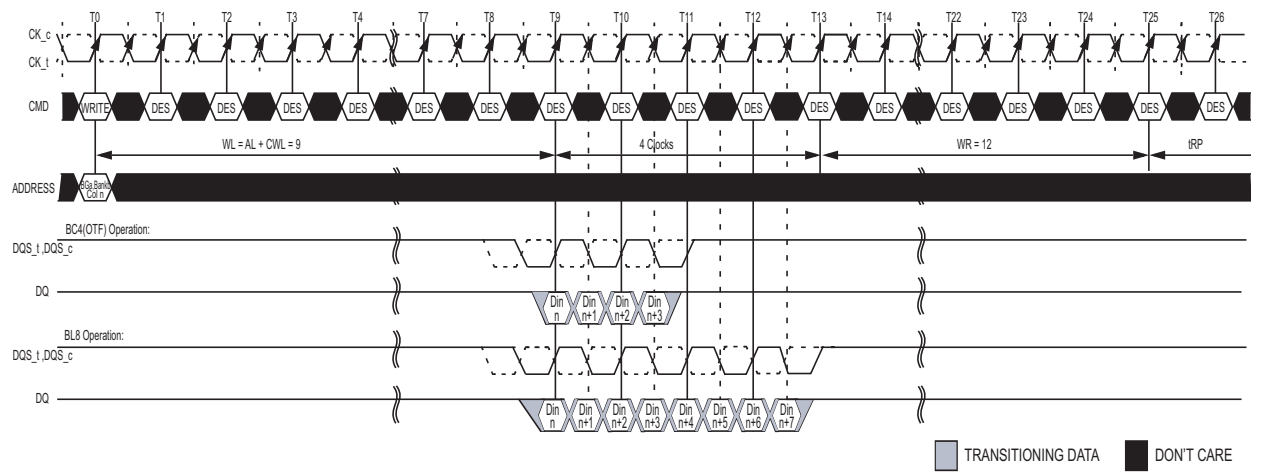
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0[A1:A0 = 1:0].

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

NOTE 6 The write recovery time (tWR) is referenced from the first rising clock edge after the last write data shown at T11. tWR specifies the last burst write cycle until the precharge command can be issued to the same bank.

WRITE (BL8/BC4) OTF with Auto PRECHARGE Operation and 1tCK Preamble



NOTE 1 BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble = 1tCK, WR = 12

NOTE 2 DIN n = data-in to column n.

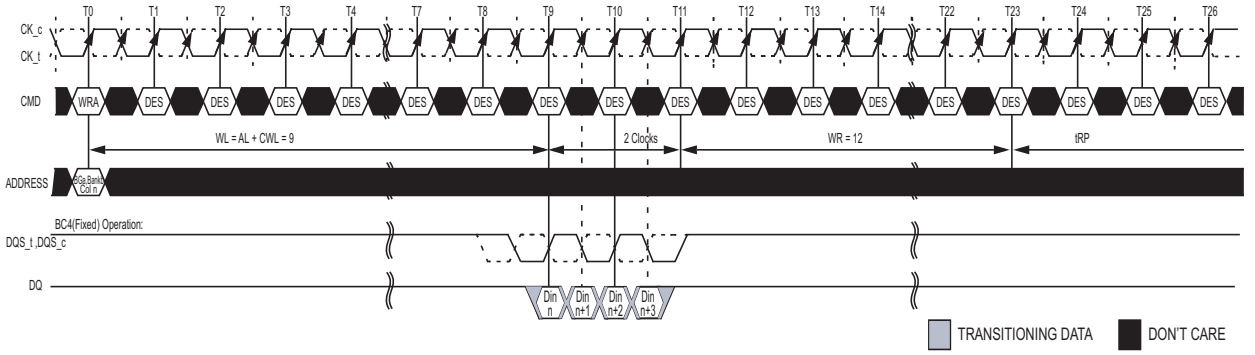
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0[A1:A0 = 0:1] and A12 =0 during WRITE command at T0. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 =1 during WRITE command at T0.

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

NOTE 6 The write recovery time (tWR) is referenced from the first rising clock edge after the last write data shown at T13. tWR specifies the last burst write cycle until the precharge command can be issued to the same bank.

WRITE (BC4) Fixed with Auto PRECHARGE Operation and 1tCK Preamble



NOTE 1 BC = 4, AL = 0, CWL = 9, Preamble = 1tCK, WR = 12

NOTE 2 DIN n = data-in to column n.

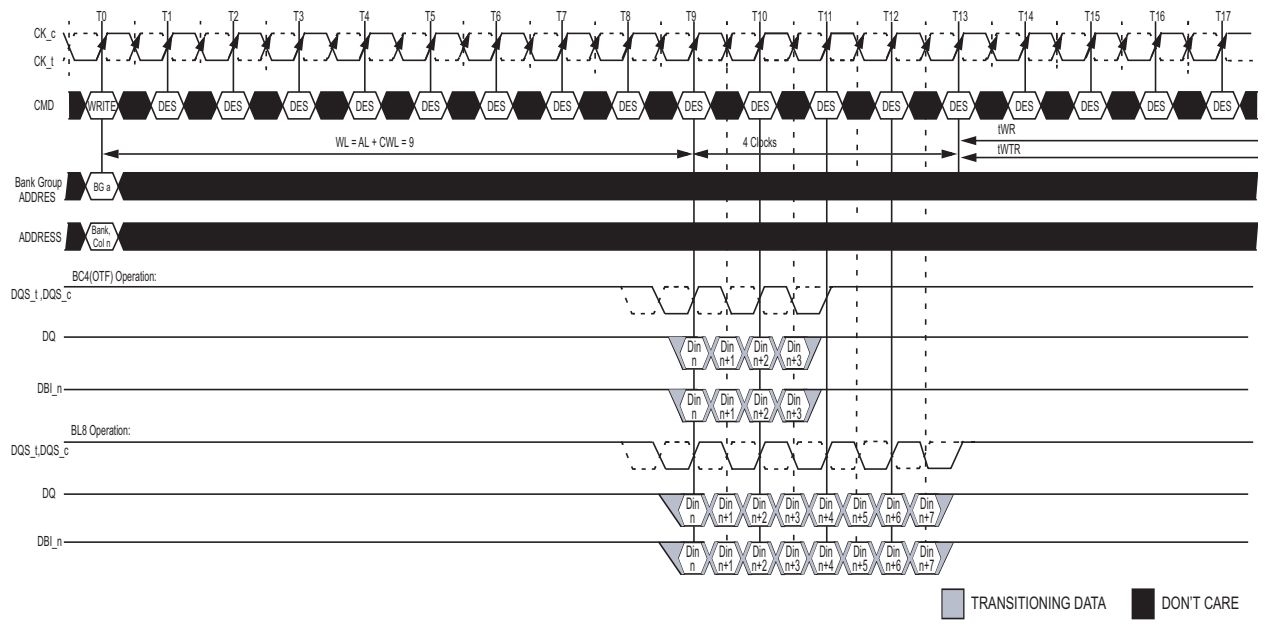
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0[A1:A0 = 1:0].

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

NOTE 6 The write recovery time (tWR) is referenced from the first rising clock edge after the last write data shown at T11. tWR specifies the last burst write cycle until the precharge command can be issued to the same bank.

WRITE (BL8/BC4) OTF with 1tCK Preamble and DBI



NOTE 1 BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble = 1tCK

NOTE 2 DIN n = data-in to column n.

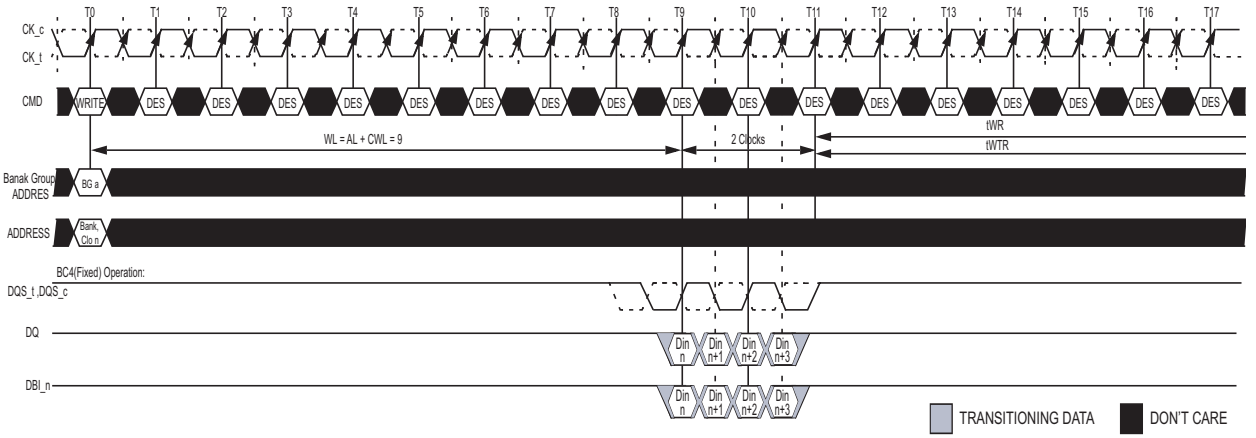
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0[A1:A0 = 0:1] and A12 =0 during WRITE command at T0. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 =1 during WRITE command at T0.

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Enable, CRC = Disable.

NOTE 6 The write recovery time (tWR_DBI) and write timing parameter (tWTR_DBI) are referenced from the first rising clock edge after the last write data shown at T13.

WRITE (BC4) Fixed with 1tCK Preamble and DBI



NOTE 1 BC = 4, AL = 0, CWL = 9, Preamble = 1tCK

NOTE 2 DIN n = data-in to column n.

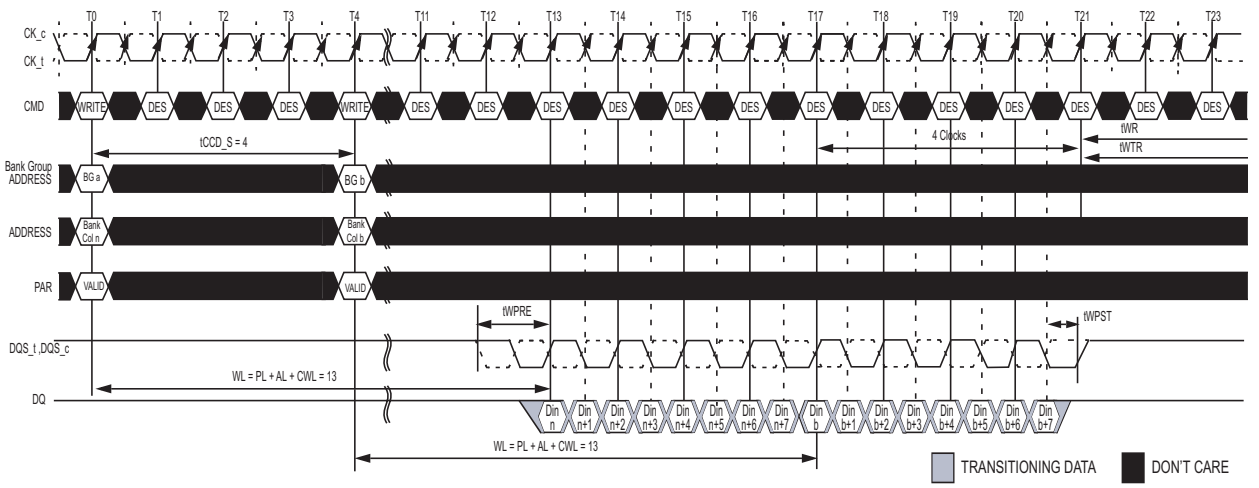
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0[A1:A0 = 1:0].

NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Enable, CRC = Disable.

NOTE 6 The write recovery time (tWR_DBI) and write timing parameter (tWTR_DBI) are referenced from the first rising clock edge after the last write data shown at T11.

Consecutive WRITE (BL8) with 1tCK Preamble and CA Parity in Different Bank Group



NOTE 1 BL = 8, AL = 0, CWL = 9, PL = 4, Preamble = 1tCK

NOTE 2 DIN n (or b) = data-in to column n(or column b).

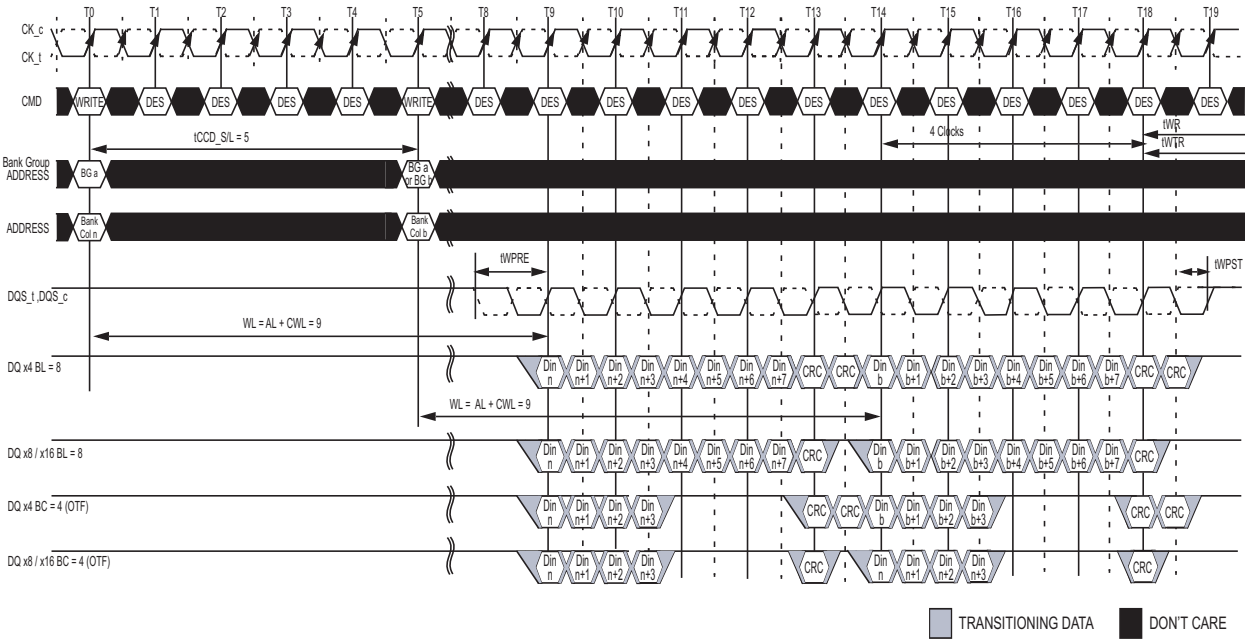
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 =1 during WRITE command at T0 and T4.

NOTE 5 CA Parity = Enable, CS to CA Latency = Disable, Write DBI = Disable.

NOTE 6 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T21.

Consecutive WRITE (BL8/BC4)OTF with 1tCK Preamble and Write CRC in Same or Different Bank Group



NOTE 1 BL = 8/BC = 4, AL = 0, CWL = 9, Preamble = 1tCK, tCCD_S/L = 5

NOTE 2 DIN n (or b) = data-in to column n(or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

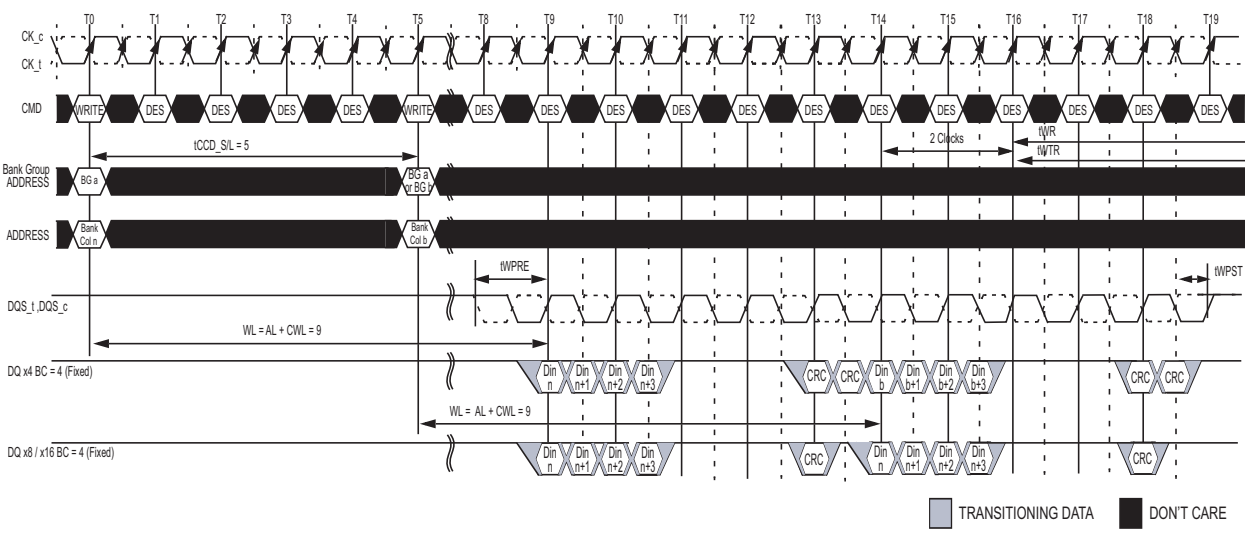
NOTE 4 BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during WRITE command at T0 and T5.

NOTE 5 BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T0 and T5.

NOTE 6 C/A Parity = Disable, CS to C/A Latency = Disable, Write DBI = Disable, Write CRC = Enable.

NOTE 7 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T18.

Consecutive WRITE (BC4)Fixed with 1tCK Preamble and Write CRC in Same or Different Bank Group



NOTE 1 BL = 8, AL = 0, CWL = 9, Preamble = 1tCK, tCCD_S/L = 5

NOTE 2 DIN n (or b) = data-in to column n(or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

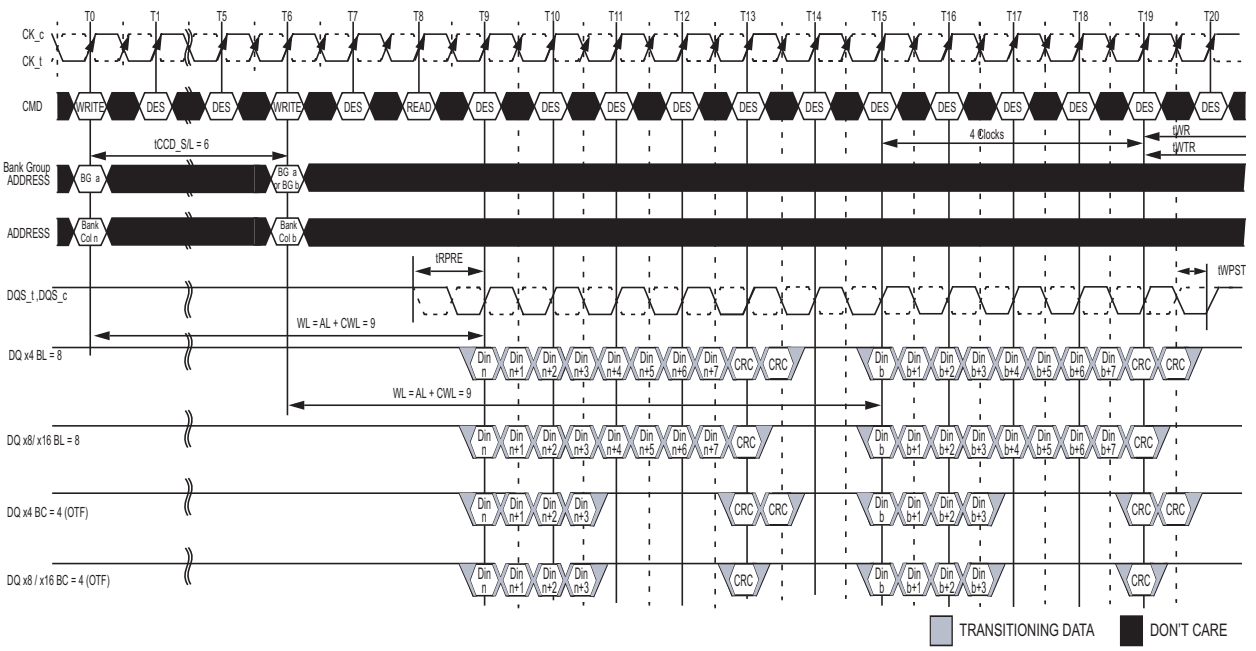
NOTE 4 BL8 setting activated by MR0[A1:A0 = 1:0] at T0 and T5.

NOTE 5 BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T0 and T5.

NOTE 6 C/A Parity = Disable, CS to C/A Latency = Disable, Write DBI = Disable, Write CRC = Enable.

NOTE 7 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T16.

Nonconsecutive WRITE (BL8/BC4)OTF with 1tCK Preamble and Write CRC in Same or Different Bank Group



NOTE 1 BL = 8, AL = 0, CWL = 9, Preamble = 1tCK, tCCD_S/L = 6

NOTE 2 DIN n (or b) = data-in to column n(or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

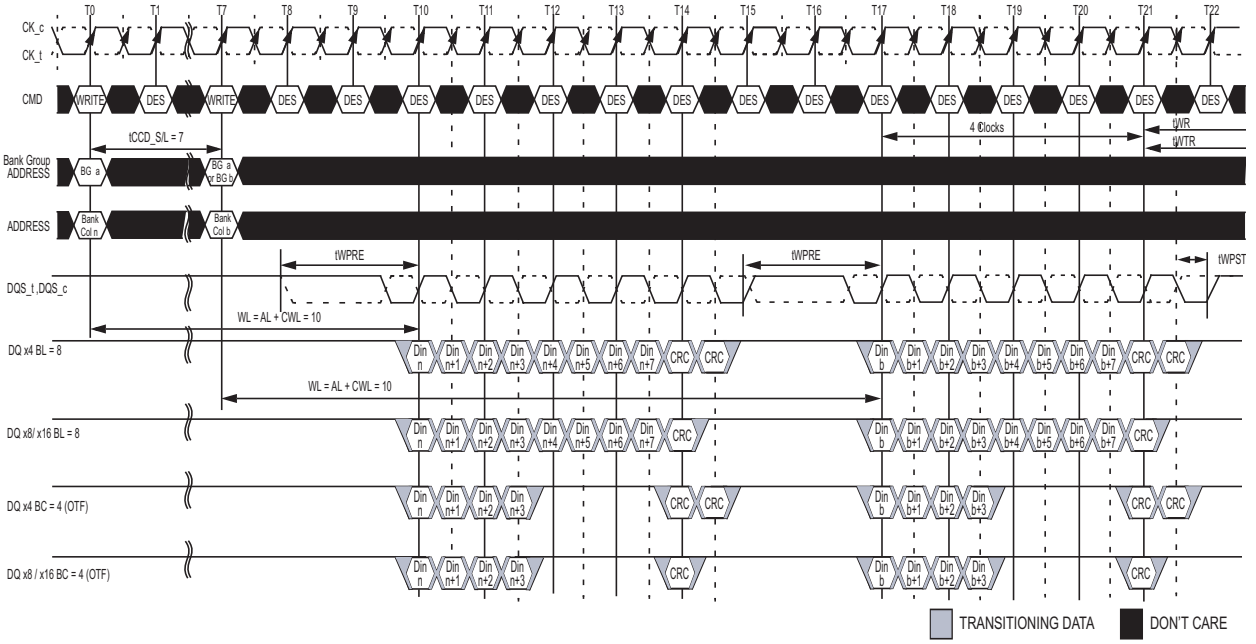
NOTE 4 BL8 setting activated by either MR0[A1A:0 = 0:0] or MR0[A1A:0 = 0:1] and A12 =1 during WRITE command at T0 and T6.

NOTE 5 BC4 setting activated by MR0[A1:A0 = 0:1] and A12 =0 during WRITE command at T0 and T6.

NOTE 6 C/A Parity = Disable, CS to C/A Latency = Disable, Write DBI = Disable, Write CRC = Enable.

NOTE 7 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T19.

Nonconsecutive WRITE (BL8/BC4)OTF with 2tCK Preamble and Write CRC in Same or Different Bank Group



NOTE 1 BL = 8, AL = 0, CWL = 9 + 1 = 10[9], Preamble = 2tCK, tCCD_S/L = 7

NOTE 2 DIN n (or b) = data-in to column n(or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 =1 during WRITE command at T0 and T7.

NOTE 5 BC4 setting activated by MR0[A1:A0 = 0:1] and A12 =0 during WRITE command at T0 and T7.

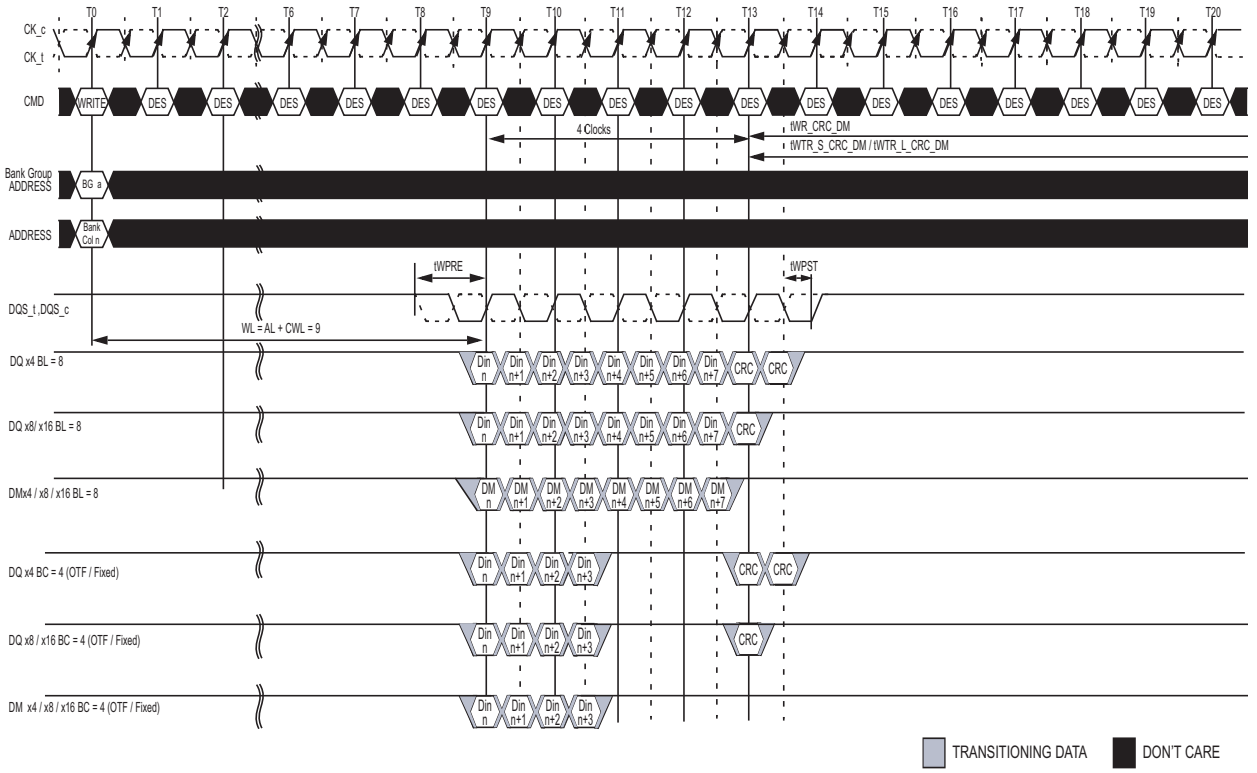
NOTE 6 C/A Parity = Disable, CS to C/A Latency = Disable, Write DBI = Disable, Write CRC = Enable.

NOTE 7 tCCD_S/L = 6 isn't allowed in 2tCK preamble mode.

NOTE 8 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T21.

NOTE 9 When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range. That means CWL = 9 is not allowed when operating in 2tCK Write Preamble Mode.

WRITE (BL8/BC4)OTF/Fixed with 1tCK Preamble and Write CRC and DM in Same or Different Bank Group



NOTE 1 BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble = 1tCK

NOTE 2 DIN n = data-in to column n.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0.

NOTE 5 BC4 setting activated by either MR0[A1:A0 = 1:0] or MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0.

NOTE 6 CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable, Write CRC = Enable, DM = Enable.

NOTE 7 The write recovery time (tWR_CRC_ DM) and write timing parameter (tWR_S_CRC_ DM/tWR_L_CRC_ DM) are referenced from the first rising clock edge after the last write data shown at T13.

ZQ Calibration Commands

ZQ Calibration command is used to calibrate DRAM Ron & ODT values. DDR4 SDRAM needs longer time to calibrate output driver and on-die termination circuits at initialization and relatively smaller time to perform periodic calibrations.

ZQCL command is used to perform the initial calibration during power-up initialization sequence. This command may be issued at any time by the controller depending on the system environment. ZQCL command triggers the calibration engine inside the DRAM and, once calibration is achieved, the calibrated values are transferred from the calibration engine to DRAM IO, which gets reflected as updated output driver and on-die termination values.

The first ZQCL command issued after reset is allowed a timing period of tZQinit to perform the full calibration and the transfer of values. All other ZQCL commands except the first ZQCL command issued after RESET are allowed a timing period of tZQoper.

ZQCS command is used to perform periodic calibrations to account for voltage and temperature variations. A shorter timing window is provided to perform the calibration and transfer of values as defined by timing parameter tZQCS. One ZQCS command can effectively correct a minimum of 0.5% (ZQ Correction) of RON and RTT impedance error within 128 nCK for all speed bins assuming the maximum sensitivities specified in the 'Output Driver Voltage and Temperature Sensitivity' and 'ODT Voltage and Temperature Sensitivity' tables. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters. One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{\text{ZQCorrection}}{(\text{TSens} \times \text{Tdriftrate}) + (\text{VSens} \times \text{Vdriftrate})}$$

Where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities.

For example, if TSens = 1.5% / ^{o}C, VSens = 0.15% / mV, Tdriftrate = 1 ^{o}C / sec and Vdriftrate = 15 mV / sec, then the interval between ZQCS commands is calculated as:

$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 \sim 128\text{ms}$$

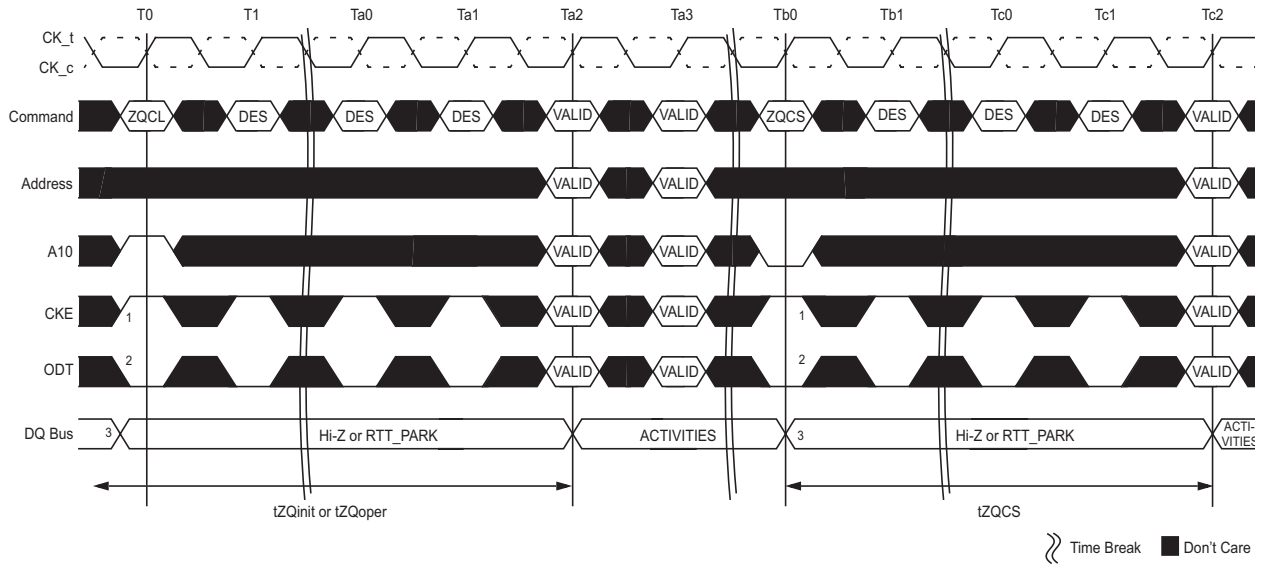
No other activities should be performed on the DRAM channel by the controller for the duration of tZQinit, tZQoper, or tZQCS. The quiet time on the DRAM channel allows accurate calibration of output driver and on-die termination values. Once DRAM calibration is achieved, the DRAM should disable ZQ current consumption path to reduce power.

All banks must be precharged and tRP met before ZQCL or ZQCS commands are issued by the controller. See 'Command Truth Table' for a description of the ZQCL and ZQCS commands.

ZQ calibration commands can also be issued in parallel to DLL lock time when coming out of self refresh. Upon Self-Refresh exit, DDR4 SDRAM will not perform an IO calibration without an explicit ZQ calibration command. The earliest possible time for ZQ Calibration command (short or long) after self refresh exit is XS, XS_Abort/ XS_FAST depending on operation mode.

In systems that share the ZQ resistor between devices, the controller must not allow any overlap of tZQoper, tZQinit, or tZQCS between the devices.

ZQ Calibration Timing



NOTE 1 CKE must be continuously registered high during the calibration procedure.

NOTE 2 During ZQ Calibration, ODT signal must be held LOW and DRAM continues to provide RTT_PARK.

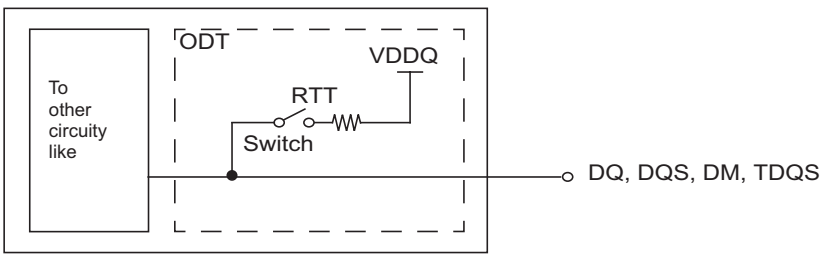
NOTE 3 All devices connected to the DQ bus should be high impedance or RTT_PARK during the calibration procedure.

On-Die Termination

ODT (On-Die Termination) is a feature of the DDR4 SDRAM that allows the DRAM to change termination resistance for each DQ, DQS, $\overline{DQS}$ and $\overline{DM}$ for x4 and x8 configuration (and TDQS, $\overline{TDQS}$ for X8 configuration, when enabled via A11=1 in MR1) via the ODT control pin or Write Command or Default Parking value with MR setting. For x16 configuration, ODT is applied to each UDQ, LDQ, UDQS, $\overline{UDQS}$, LDQS, $\overline{LDQS}$, UDM and $\overline{LDM}$ signal. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently change termination resistance for any or all DRAM devices. More details about ODT control modes and ODT timing modes can be found further down in this document.

The ODT feature is turned off and not supported in Self-Refresh mode. A simple functional representation of the DRAM ODT feature is shown in figure below.

Functional Representation of ODT



The switch is enabled by the internal ODT control logic, which uses the external ODT pin and Mode Register Setting and other control information, see below. The value of RTT is determined by the settings of Mode Register bits. The ODT pin will be ignored if the Mode Registers MR1 is programmed to disable RTT_NOM(MR1{A10,A9,A8}={0,0,0}) and in self-refresh mode.

ODT Mode Register and ODT State Table

The ODT Mode of DDR4 SDRAM has 4 states, Data Termination Disable, RTT_WR, RTT_NOM and RTT_PARK. And the ODT Mode is enabled if any of MR1{A10,A9,A8} or MR2 {A10:A9} or MR5 {A8:A6} are non zero. In this case, the value of RTT is determined by the settings of those bits.
After entering Self-Refresh mode, DRAM automatically disables ODT termination and set Hi-Z as termination state regardless of these setting.

Application: Controller can control each RTT condition with WR/RD command and ODT pin
- RTT_WR: The rank that is being written to provide termination regardless of ODT pin status (either HIGH or LOW)
- RTT_NOM: DRAM turns ON RTT_NOM if it sees ODT asserted (except ODT is disabled by MR1).
- RTT_PARK: Default parked value set via MR5 to be enabled and ODT pin is driven LOW.
- Data Termination Disable: DRAM driving data upon receiving READ command disables the termination after RL-X and stays off for a duration of BL/2 + X + Y clock cycles.
X is 2 for 1tCK and 3 for 2tCK preamble mode.
Y is 0 when CRC is disabled and 1 when it's enabled.
- The Termination State Table is shown in below table.

Those RTT values have priority as following.
1. Data Termination Disable
2. RTT_WR
3. RTT_NOM
4. RTT_PARK

which means if there is WRITE command along with ODT pin HIGH, then DRAM turns on RTT_WR not RTT_NOM, and also if there is READ command, then DRAM disables data termination regardless of ODT pin and goes into Driving

mode.

Termination State Table

RTT_PARK MR5{A8:A6}	RTT_NOM MR1 {A10:A9:A8}	ODT pin	DRAM termination state	Note
Enabled	Enabled	HIGH	RTT_NOM	1,2
		LOW	RTT_PARK	1,2
	Disabled	Don't care[3]	RTT_PARK	1,2
Disabled	Enabled	HIGH	RTT_NOM	1,2
		LOW	Hi-Z	1,2
	Disabled	Don't care[3]	Hi-Z	1,2

NOTE 1 When read command is executed, DRAM termination state will be Hi-Z for defined period independent of ODT pin and MR setting of RTT_PARK/RTT_NOM. This is described in section 1.2.3 ODT During Read.

NOTE 2 If RTT_WR is enabled, RTT_WR will be activated by Write command for defined period time independent of ODT pin and MR setting of RTT_PARK /RTT_NOM. This is described in Dynamic ODT section.

NOTE 3 If RTT_NOM MRS is disabled, ODT receiver power will be turned off to save power.

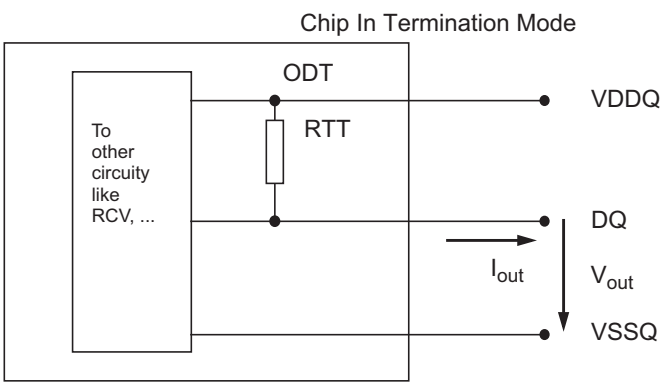
On-Die Termination effective resistance RTT is defined by MRS bits.

ODT is applied to the DQ, DM, DQS/$\overline{\text{DQS}}$ and TDQS/$\overline{\text{TDQS}}$ (x8 devices only) pins.

A functional representation of the on-die termination is shown in the figure below.

On Die Termination

$$RTT = \frac{VDDQ - Vout}{|\ I\,out\ |}$$



On die termination effective Rtt values supported are 240, 120, 80, 60, 48, 40, 34 ohms.

ODT Electrical Characteristics RZQ=240ohm +/-1% entire temperature operation range; after proper ZQ calibration

RTT	Vout	Min	Nom	Max	Unit	NOTE
240ohm	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ	1,2,3
	VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ	1,2,3
120ohm	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ	1,2,3
	VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ	1,2,3
80ohm	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ	1,2,3
	VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ	1,2,3
60ohm	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ	1,2,3
	VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ	1,2,3
48ohm	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ	1,2,3
	VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ	1,2,3
40ohm	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ	1,2,3
	VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ	1,2,3
34ohm	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ	1,2,3
	VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ	1,2,3
DQ-DQ Mismatch within byte	0.8* VDDQ	TBD		TBD	%	1,2,4

NOTE 1 The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.

NOTE 2 Pull-up ODT resistors are recommended to be calibrated at 0.8*VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5*VDDQ and 1.1*VDDQ.

NOTE 3 Measurement definition for RTT:tbd

NOTE 4 DQ to DQ mismatch within byte variation for a given component including DQS and $\overline{\text{DQS}}$ (characterized)

Synchronous ODT Mode

Synchronous ODT mode is selected whenever the DLL is turned on and locked. Based on the power-down definition, these modes are:

- Any bank active with CKE high
- Refresh with CKE high
- Idle mode with CKE high
- Active power down mode
- Precharge power down mode

In synchronous ODT mode, RTT_NOM will be turned on DODTLon clock cycles after ODT is sampled HIGH by a rising clock edge and turned off DODTLoff clock cycles after ODT is registered LOW by a rising clock edge. The ODT latency is tied to the Write Latency (WL = CWL + AL + PL) by: DODTLon = WL - 2; DODTLoff = WL - 2.
When operating in 2tCK Preamble Mode, The ODT latency must be 1 clock smaller than in 1tCK Preamble Mode; DODTLon =WL - 3; DODTLoff = WL - 3. (WL = CWL+AL+PL)

ODT Latency and Posted ODT

In Synchronous ODT Mode, the Additive Latency (AL) and the Parity Latency (PL) programmed into the Mode Register (MR1) applies to ODT Latencies as shown in table below. For details, refer to DDR4 SDRAM latency definitions.

Symbol	Parameter	1 tCK Preamble	2 tCK Preamble	Unit
DODTLon	Direct ODT turn on Latency	CWL+AL+PL-2CK	CWL+AL+PL-3CK	tCK
DODTLoff	Direct ODT turn off Latency	CWL+AL+PL-2CK	CWL+AL+PL-3CK	tCK
RODTLoff	Read command to internal ODT turn off Latency	CWL+AL+PL-2CK	CWL+AL+PL-3CK	tCK
RODTLon4	Read command to RTT_PARK turn on Latency in BC4	RODTLoff+4	RODTLoff+5	tCK
RODTLon8	Read command to RTT_PARK turn on Latency in BC4/BL8-OTF	RODTLoff+6	RODTLoff+7	tCK

NOTE 1 Applicable when WRITE CRC is disabled.

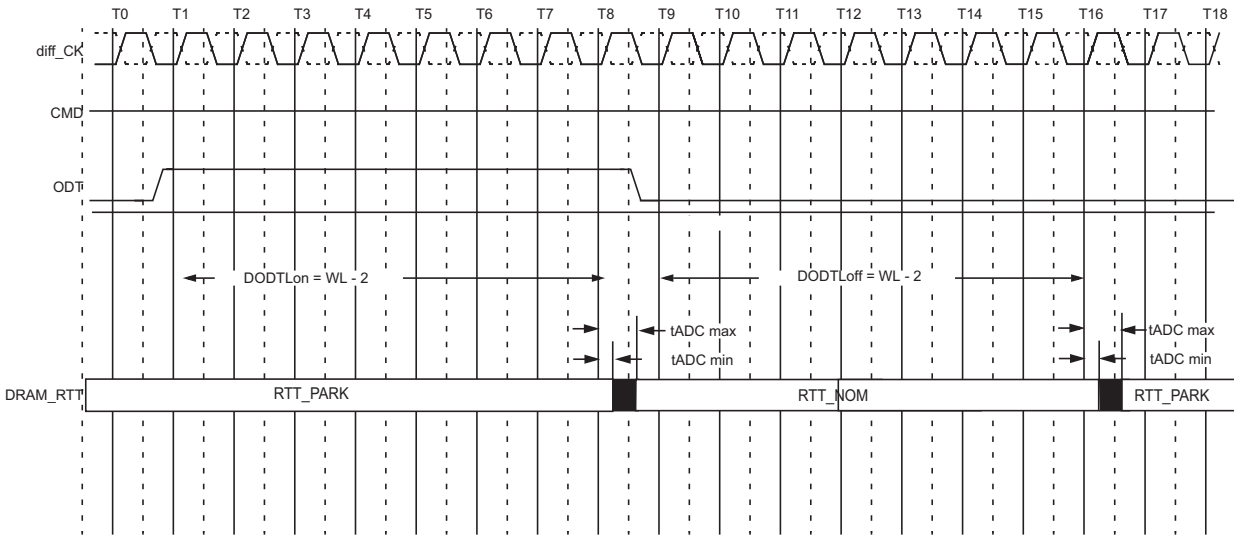
Timing Parameters

In synchronous ODT mode, the following timing parameters apply:

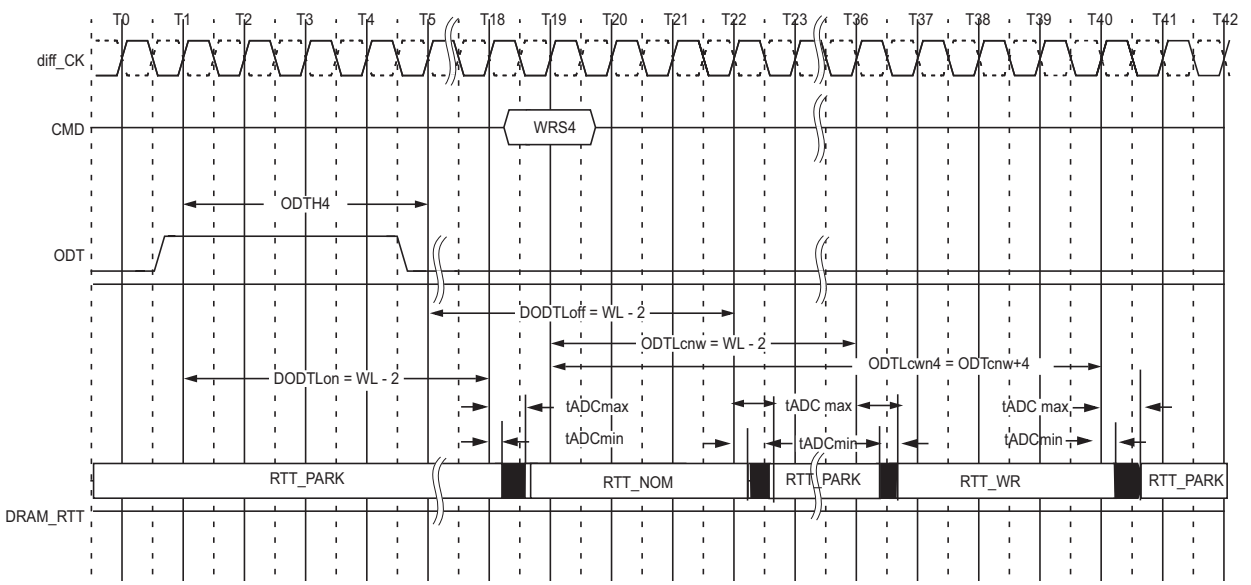
DODTLon, DODTLoff, RODTLoff, RODTLon4, RODTLon8, tADC,min,max.

tADC,min and tADC,max are minimum and maximum RTT change timing skew between different termination values. Those timing parameters apply to both the Synchronous ODT mode and the Data Termination Disable mode.
When ODT is asserted, it must remain HIGH until minimum ODTH4 (BL=4) or ODTH8 (BL=8) is satisfied. Additionally, depending on CRC or 2tCK preamble setting in MRS, ODTH should be adjusted.

Synchronous ODT Timing Example for CWL=9, AL=0, PL=0; DODTLon=WL-2=7; DODT-Loff=WL-2=7



Synchronous ODT example with BL=4, CWL=9, AL=10, PL=0; DODTLon/off=WL-2=17, ODTcnw=WL-2=17

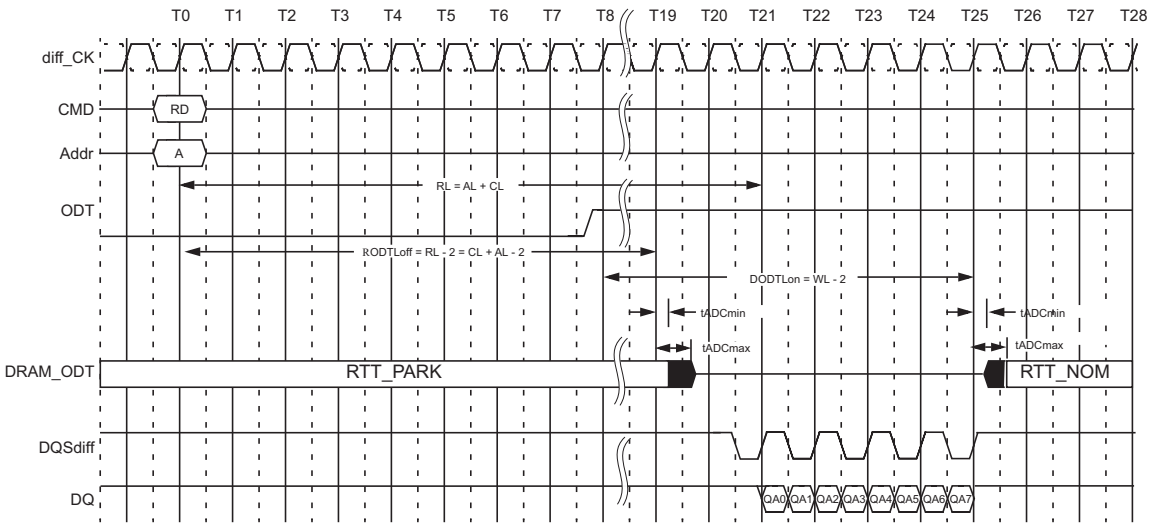


ODT must be held HIGH for at least ODTH4 after assertion (T1). ODTH is measured from ODT first registered HIGH to ODT firstregistered LOW, or from registration of Write command. Note that ODTH4 should be adjusted depending on CRC or 2tCK preamble setting.

ODT during Reads

As the DDR4 SDRAM can not terminate and drive at the same time. RTT may nominally not be enabled until the end of the postamble as shown in the example below. As shown in Figure 161 below at cycle T25, DRAM turns on the termination when it stops driving which is determined by tHZ. If DRAM stops driving early (i.e tHZ is early) then tADC,min timing may apply. If DRAM stopsdriving late (i.e tHZ is late) then DRAM complies with tADC,max timing.

Example: CL=11, PL=0; AL=CL-1=10; RL=AL+PL+CL=21; CWL=9; DODTLon=AL+CWL-2=17; DODTLoff=AL+CWL-2=17;1tCK preamble



Dynamic ODT

In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of theDDR4 SDRAM can be changed without issuing an MRS command. This requirement is supported by the “Dynamic ODT” feature asdescribed as follows:

Functional Description

The Dynamic ODT Mode is enabled if bit A[9] or A[10] of MR2 is set to ‘1’. The function is described as follows:

- Three RTT values are available: RTT_NOM, RTT_PARK and RTT_WR.
- The value for RTT_NOM is preselected via bits A[10:8] in MR1
- The value for RTT_PARK is preselected via bits A[8:6] in MR5
- The value for RTT_WR is preselected via bits A[10:9] in MR2
- During operation without commands, the termination is controlled as follows;
- Nominal termination strength RTT_NOM or RTT_PARK is selected.
- RTT_NOM on/off timing is controlled via ODT pin and latencies DODTLon and DODTLoff and RTT_PARK is on when ODT is LOW.
- When a write command (WR, WRA, WRS4, WRS8, WRAS4, WRAS8) is registered, and if Dynamic ODT is enabled, the termination is controlled as follows:
- A latency ODTLcnw after the write command, termination strength RTT_WR is selected.
- A latency ODTLcwn8 (for BL8, fixed by MRS or selected OTF) or ODTLcwn4 (for BC4, fixed by MRS or selected OTF) after thewrite command, termination strength RTT_WR is de-selected.
- 1 or 2 clocks will be added or subtracted into/from ODTLcwn8 and ODTLcwn4 depending on CRC and/or 2tCK preamble setting.

The following table shows latencies and timing parameters which are relevant for the on-die termination control in Dynamic ODT mode.

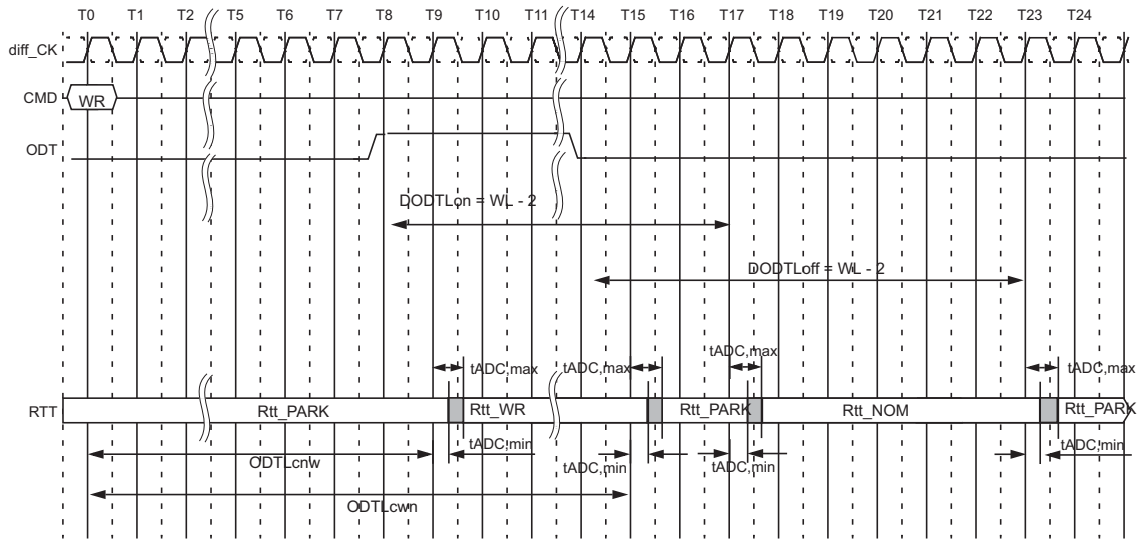
Latencies and timing parameters relevant for Dynamic ODT with 1tCK preamble mode and CRC disabled

Name and Description	Abbr.	Defined from	Define to	Definition for all DDR4 speed bins	Unit
ODT Latency for chang-ing from RTT_PARK/RTT_NOM to RTT_WR	ODTLcnw	Registering external write command	Change RTT strength from RTT_PARK/RTT_Nom to RTT_WR	ODTLcnw = WL - 2	tCK
ODT Latency for change from RTT_WR to RTT_PARK/RTT_Nom (BL = 4)	ODTLcwn4	Registering external write command	Change RTT strength from RTT_WR to RTT_PARK/ RTT_Nom	ODTLcwn4 = 4 + ODTLcnw	tCK
ODT Latency for change from RTT_WR to RTT_PARK/RTT_Nom (BL = 8)	ODTLcwn8	registering external write command	Change RTT strength from RTT_WR to RTT_PARK/ RTT_Nom	ODTLcwn8 = 6 + ODTLcnw	tCK(avg)
RTT change skew	tADC	ODTLcnw ODTLcwn	RTT valid	tADC(min) = 0.3 tADC(max) = 0.7	tCK(avg)

Latencies and timing parameters relevant for Dynamic ODT with 1 and 2tCK preamble mode and CRC en/disabled

	1tck Preamble		2tck Preamble		
Symbol	CRC off	CRC on	CRC off	CRC on	Unit
ODTLcnw	WL - 2	WL - 2	WL - 3	WL - 3	tCK
ODTLcwn4	ODTLcnw + 4	ODTLcnw + 7	ODTLcnw + 5	ODTLcnw + 8	
ODTLcwn8	ODTLcnw + 6	ODTLcnw + 7	ODTLcnw + 7	ODTLcnw + 8	

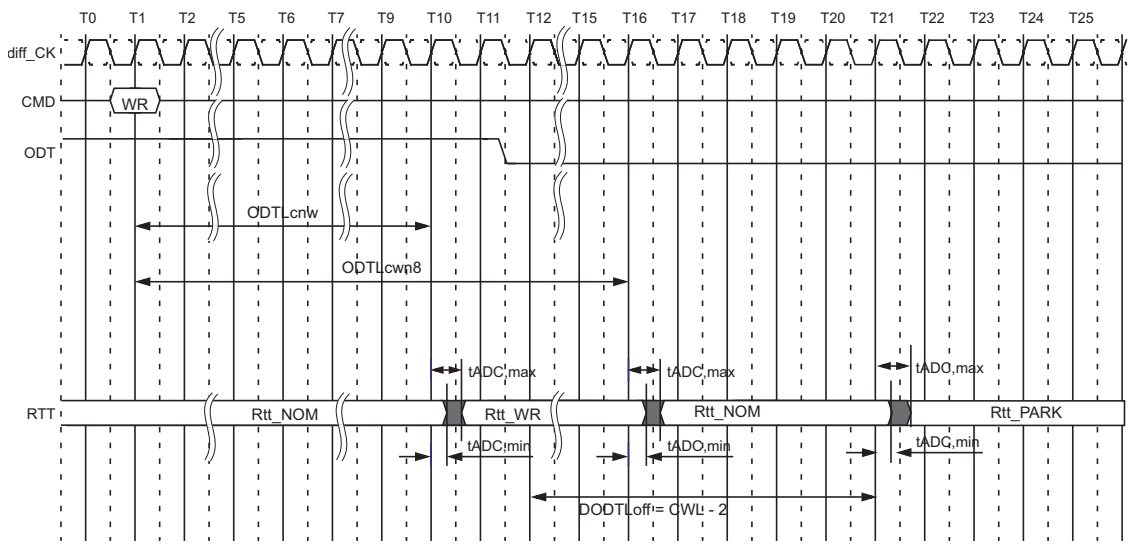
ODT timing (Dynamic ODT, 1tCK preamble, CL=14, CWL=11, BL=8, AL=0, CRC Disabled)



ODTLcnw = WL-2 (1tCK preamble), WL-3 (2tCK preamble)

If BC4 then ODTLcwn = WL+4 if CRC disabled or WL+5 if CRC enabled; If BL8 then ODTLcwn = WL+6 if CRC disabled or WL+7 if CRC enabled.

Dynamic ODT overlapped with Rtt_NOM (CL=14, CWL=11, BL=8, AL=0, CRC Disabled)



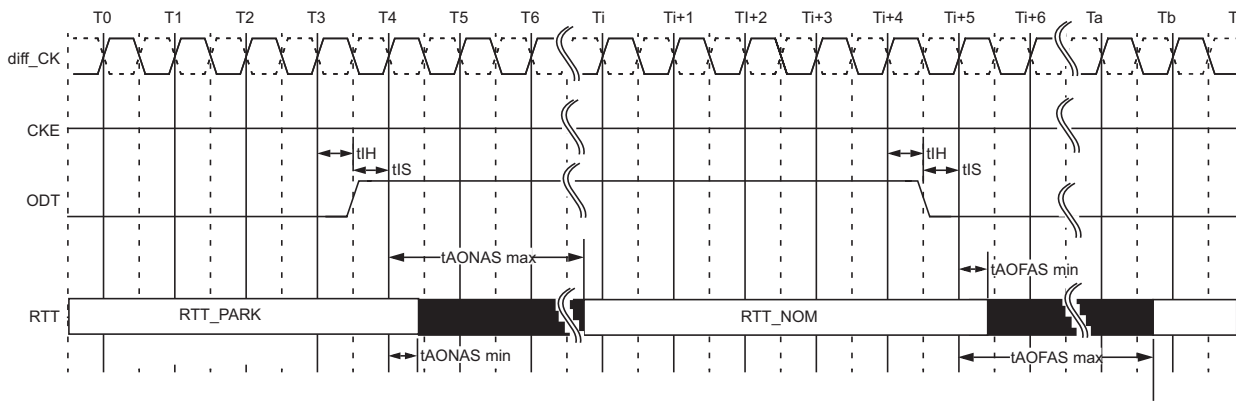
Behavior with WR command is issued while ODT being registered high.

Asynchronous ODT mode

Asynchronous ODT mode is selected when DLL is disabled by MR1 bit A0='0'b.
In asynchronous ODT timing mode, internal ODT command is not delayed by either the Additive latency (AL) or relative to the external ODT signal (RTT_NOM).
In asynchronous ODT mode, the following timing parameters apply tAONAS,min, max, tAOFAS,min,max.

Minimum RTT_NOM turn-on time (tAONASmin) is the point in time when the device termination circuit leaves RTT_PARK and ODT resistance begins to change.
Maximum RTT_NOM turn on time(tAONASmax) is the point in time when the ODT resistance is reached RTT_NOM.
tAONASmin and tAONASmax are measured from ODT being sampled high.
Minimum RTT_NOM turn-off time (tAOFASmin) is the point in time when the devices termination circuit starts to leave RTT_NOM.
Maximum RTT_NOM turn-off time (tAOFASmax) is the point in time when the on-die termination has reached RTT_PARK.
tAOFASmin and tAOFASmax are measured from ODT being sampled low.

Asynchronous ODT Timing on DDR4 SDRAM with DLL-off



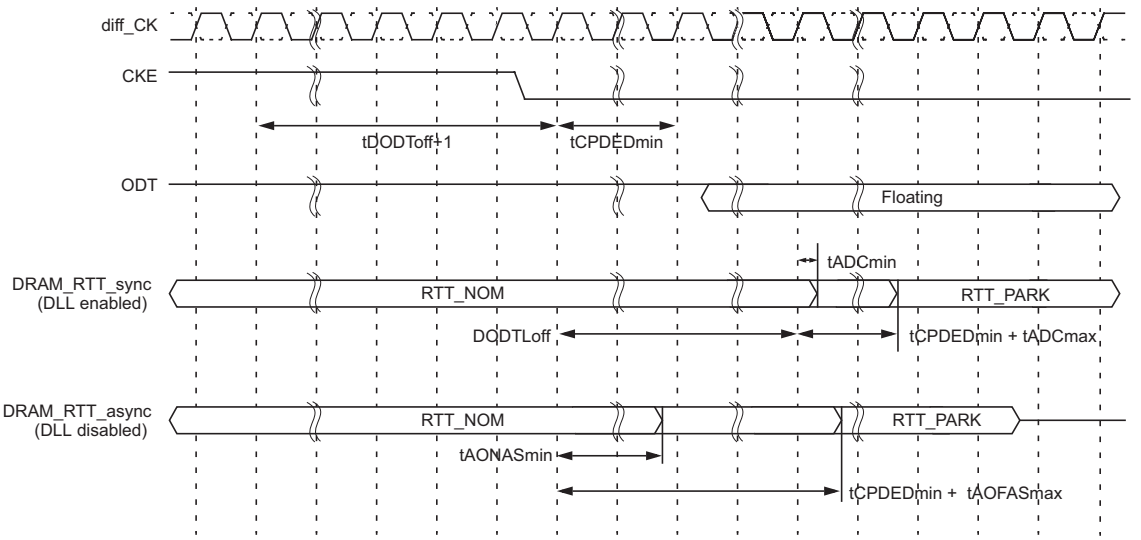
Asynchronous ODT Timing Parameters for all Speed Bins

Description	Symbol	min	max	Unit
Asynchronous RTT turn-on delay	tAONAS	1.0	9.0	ns
Asynchronous RTT turn-off delay	tAOFAS	1.0	9.0	ns

ODT buffer disabled mode for Power down

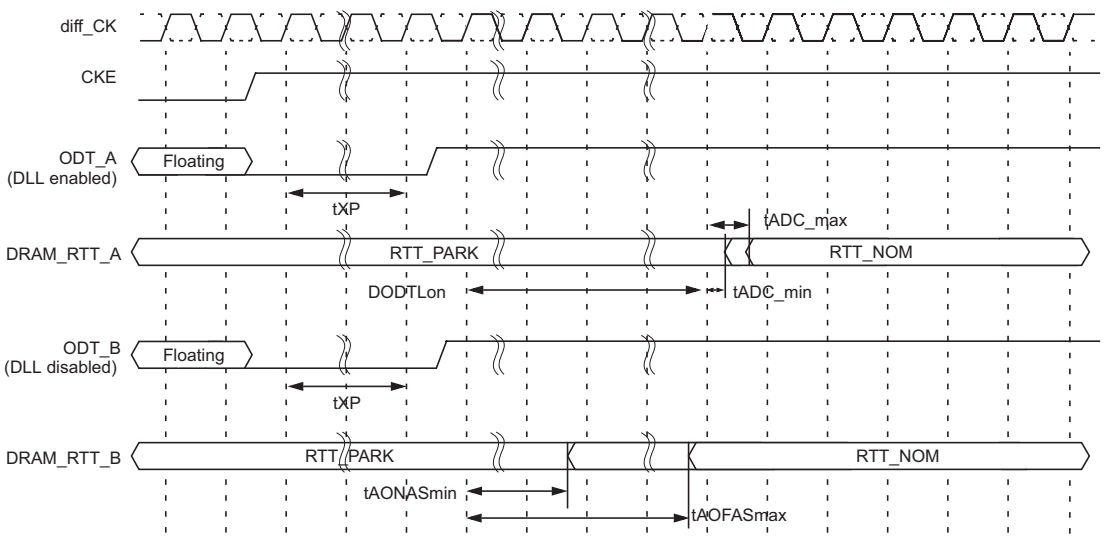
DRAM does not provide Rtt_NOM termination during power down when ODT input buffer deactivation mode is enabled in MR5 bit A5. To account for DRAM internal delay on CKE line to disable the ODT buffer and block the sampled output, the host controller must continuously drive ODT to either low or high when entering power down. The ODT signal may be floating after tCPDEDmin has expired. In this mode, RTT_NOM termination corresponding to sampled ODT at the input after CKE is first registered low (and tANPD before that) may not be provided. tANPD is equal to (WL-1) and is counted backwards from PDE.

ODT timing for power down entry with ODT buffer disable mode



When exit from power down, along with CKE being registered high, ODT input signal must be re-driven and maintained low until tXP is met.

ODT timing for power down exit with ODT buffer disable mode

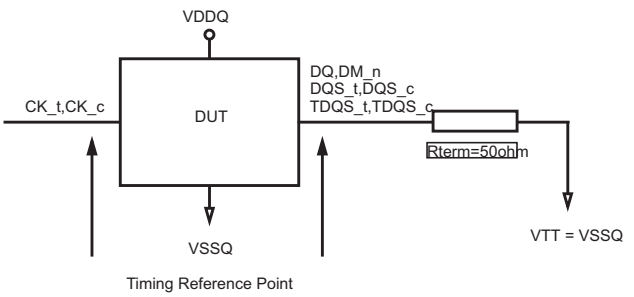


ODT Timing Definitions

Test Load for ODT Timings

Different than for timing measurements, the reference load for ODT timings is defined in figure below.

ODT Timing Reference Load



ODT Timing Definitions

Definitions for tADC, tAONAS and tAOFAS are provided in Table 60 and subsequent figures. Measurement reference settings areprovided in Table 61. tADC of Dynamic ODT case and Read Disable ODT case are represented by tADC of Direct ODTControl case.

Symbol	Begin Point Definition	End Point Definition
tADC	Rising edge of CK_t,CK_c defined by the end point of DODTLoff	Extrapolated point at VRTT_NOM
	Rising edge of CK_t,CK_c defined by the end point of DODTLon	Extrapolated point at VSSQ
	Rising edge of CK_t,CK_c defined by the end point of ODTLcnw	Extrapolated point at VRTT_NOM
	Rising edge of CK_t,CK_c defined by the end point of ODTLcwn4 or ODTLcwn8	Extrapolated point at VSSQ
tAONAS	Rising edge of CK_t,CK_c with ODT being first registered high	Extrapolated point at VSSQ
tAOFAS	Rising edge of CK_t,CK_c with ODT being first registered low	Extrapolated point at VRTT_NOM

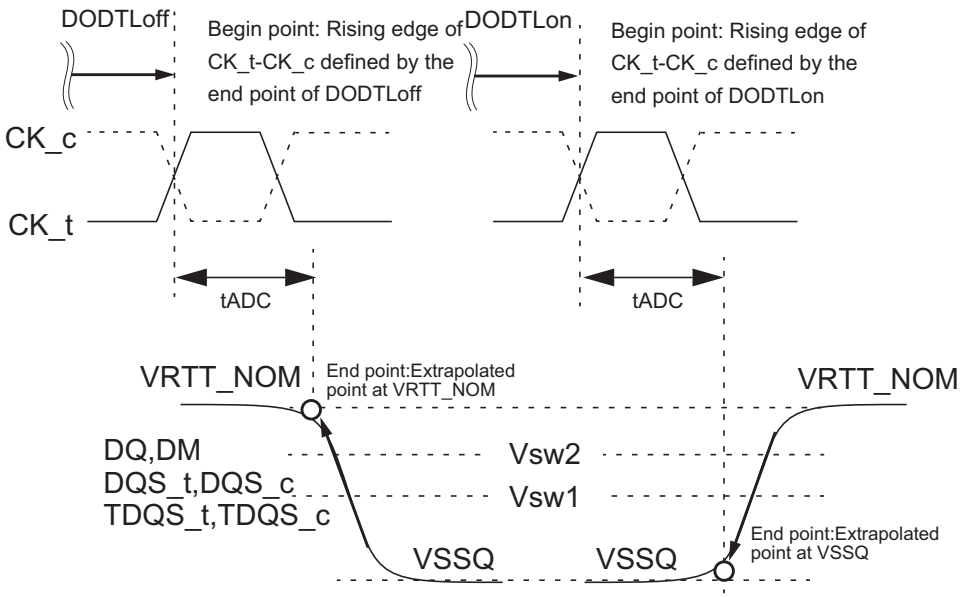
Reference Settings for ODT Timing Measurements

Measured Parameter	RTT_PARK	RTT_NOM	RTT_WR	Vsw1	Vsw2	Note
tADC	Disable	RZQ/7	-	0.20V	0.40V	1,2
	-	RZQ/7	Hi-Z	0.20V	0.40V	1,3
tAONAS	Disable	RZQ/7	-	0.20V	0.40V	1,2
tAOFAS	Disable	RZQ/7	-	0.20V	0.40V	1,2

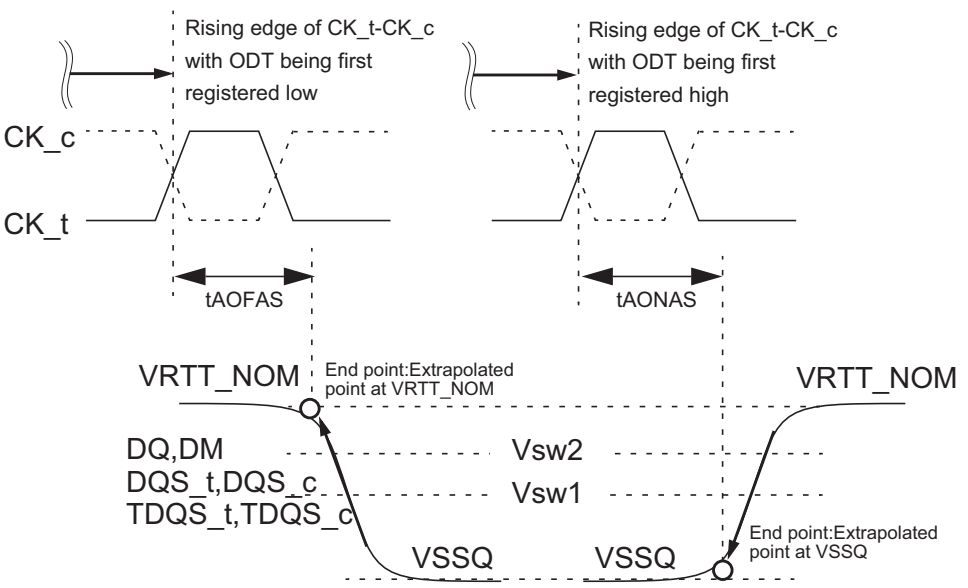
NOTE 1 MR setting is as follows.
- MR1 A10=1, A9=1, A8=1 (RTT_NOM_Setting)
- MR5 A8=0 , A7=0, A6=0 (RTT_PARK Setting)
- MR2 A11=0, A10=1, A9=1 (RTT_WR Setting)

NOTE 2 ODT state change is controlled by ODT pin.
NOTE 3 ODT state change is controlled by Write Command.

Definition of tADC



Definition of tAOFAS and tAONAS



Absolute Maximum Ratings

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
V_{DD}	Voltage on V_{DD} pin relative to Vss	-0.3 ~ 1.5	V	1,3
V_{DDQ}	Voltage on V_{DDQ} pin relative to Vss	-0.3 ~ 1.5	V	1,3
V_{PP}	Voltage on V_{PP} pin relative to Vss	-0.3 ~ 3	V	4
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	-0.3 ~ 1.5	V	1
T_{STG}	Storage Temperature	-55 to +100	°C	1,2

NOTE :

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. V_{DD} and V_{DDQ} must be within 300mV of each other at all times;and V_{REF} must be not greater than 0.6 x V_{DDQ}, When V_{DD} and V_{DDQ} are less than 500mV; V_{REF} may be equal to or less than 300mV.
4. VPP must be equal or greater than VDD/VDDQ at all times.

AC & DC Operating Conditions

Recommended DC Operating Conditions

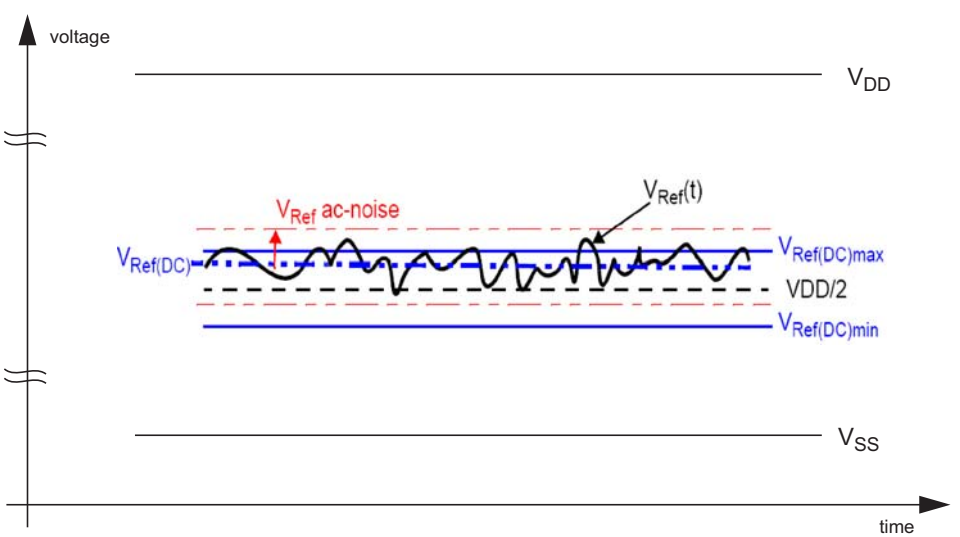
Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply voltage	1.14	1.2	1.26	V	1,2,3
VDDQ	Supply voltage for Output	1.14	1.2	1.26	V	1,2,3
VPP	Supply voltage for Output	2.375	2.5	2.75	V	3

NOTE :
1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. DC bandwidth is limited to 20MHz.

AC and DC Input Measurement Levels: VREF Tolerances

The DC-tolerance limits and ac-noise limits for the reference voltages VREFCA is illustrated in figure below. It shows a valid referencevoltage VREF(t) as a function of time. (VREF stands for VREFCA).
VREF(DC) is the linear average of VREF(t) over a very long period of time (e.g. 1 sec). This average has to meet the min/maxrequirement. Furthermore VREF(t) may temporarily deviate from VREF(DC) by no more than +/- 1% VDD.

Illustration of VREF(DC) tolerance and VREF AC-noise limits

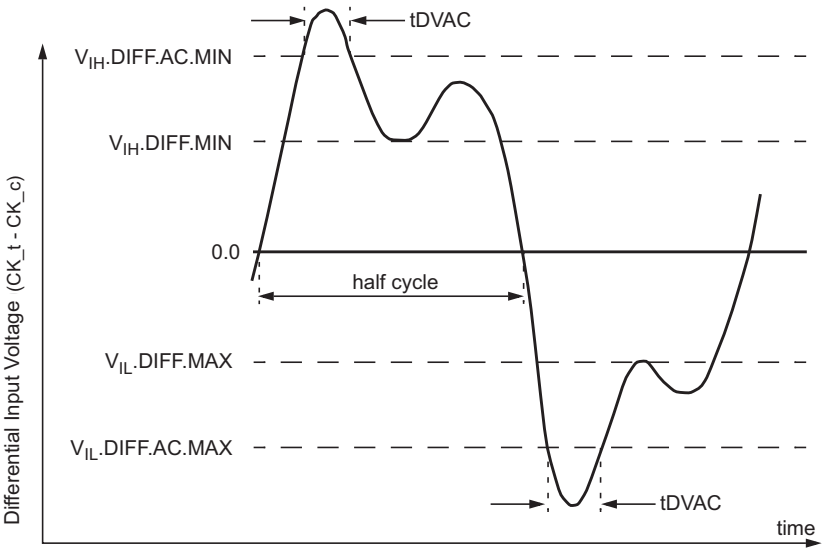


The voltage levels for setup and hold time measurements VIH(AC), VIH(DC), VIL(AC) and VIL(DC) are dependent on VREF. "VREF" shall be understood as VREF(DC), as defined in above figure.

This clarifies, that DC-variations of VREF affect the absolute voltage a signal has to reach to achieve a valid high or low level andtherefore the time to which setup and hold is measured. System timing and voltage budgets need to account for VREF(DC) deviationsfrom the optimum position within the data-eye of the input signals.
This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with VREFAC-noise. Timing and voltage effects due to AC-noise on VREF up to the specified limit (+/-1% of VDD) are included in DRAM timingsand their associated deratings.

AC and DC Logic Input Levels for Differential Signals CK, $\overline{CK}$

Definition of differential ac-swing and "time above ac-level" tDVAC



Note 1 Differential signal rising edge from VIL.DIFF.MAX to VIH.DIFF.MIN must be monotonic slope.
Note 2 Differential signal falling edge from VIH.DIFF.MIN to VIL.DIFF.MAX must be monotonic slope.

Differential AC and DC Input Levels

Symbol	Parameter	DDR4 -1600,1866,2133		DDR4 -2400,2666 & 3200		Units	Notes
		Min.	Max.	Min.	Max.		
VIHdiff	Differential input high	+0.2	NOTE 3	0.135	NOTE 3	V	1
VILdiff	Differential input low	NOTE 3	-0.2	NOTE 3	-0.135	V	1
VIHdiff(AC)	Differential input high AC	2 x (VIH(AC) - VREF)	NOTE 3	2 x (VIH(AC) - VREF)	NOTE 3	V	2
VILdiff(AC)	Differential input low AC	NOTE 3	2 x (VIL(AC) - VREF)	NOTE 3	2 x (VIL(AC) - VREF)	V	2

NOTE :

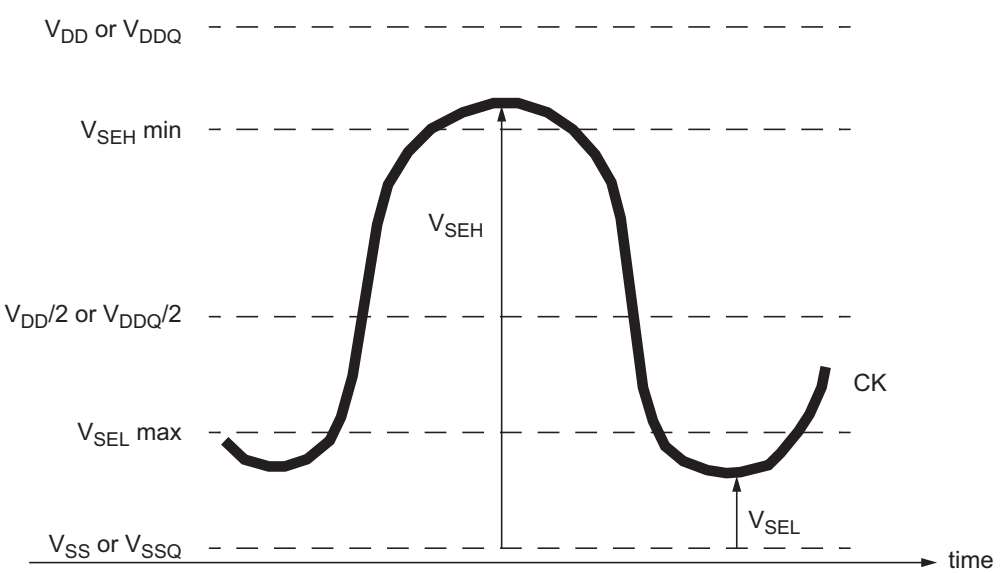
1. Used to define a differential signal slew-rate.
2. for CK - $\overline{CK}$ use VIH.CA/VIL.CA(AC) of address/command and VREFCA.
3. These values are not defined; however, the differential signals CK - $\overline{CK}$, need to be within the respective limits (VIH.CA(DC) max, VIL.CA(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

Allowed time before ringback (tDVAC) for CK - $\overline{CK}$

Slew Rate [V/ns]	tDVAC [ps] @ |VIH/Ldiff(AC)| = 200mV		tDVAC [ps] @ |VIH/Ldiff(AC)| = TBDmV	
	Min.	Max.	Min.	Max.
> 4.0	120	-	TBD	-
4.0	115	-	TBD	-
3.0	110	-	TBD	-
2.0	105	-	TBD	-
1.8	100	-	TBD	-
1.6	95	-	TBD	-
1.4	90	-	TBD	-
1.2	85	-	TBD	-
1.0	80	-	TBD	-
< 1.0	80	-	TBD	-

Single-ended requirements for differential signals CK, $\overline{CK}$

Each individual component of a differential signal (CK, $\overline{CK}$) has also to comply with certain requirements for single-ended signals.
CK and $\overline{CK}$ have to approximately reach VSEHmin / VSELmax (approximately equal to the ac-levels (VIH.CA(ac) / VIL.CA(ac)) for ADD/CMD signals) in every half-cycle.
Note that the applicable ac-levels for ADD/CMD might be different per speed-bin etc. E.g., if Different value than VIH.CA(AC100)/VIL.CA(AC100) is used for ADD/CMD signals, then these ac-levels apply also for the single-ended signals CK and $\overline{CK}$



Note that, while ADD/CMD signal requirements are with respect to VrefCA, the single-ended components of differential signals have a requirement with respect to VDD / 2; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSELmax, VSEHmin has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Single-ended levels for CK, $\overline{CK}$

Symbol	Parameter	DDR4-1600/1866/2133		DDR4-2400/2666/3200		Units	Notes
		Min.	Max.	Min.	Max.		
VSEH	Single-ended high-level for CK, $\overline{CK}$	(VDD/2) + 0.100	NOTE 3	TBD	NOTE 3	V	1,2
VSEL	Single-ended low-level for CK, $\overline{CK}$	NOTE 3	(VDD/2) - 0.100	NOTE 3	(VDD/2)- 0.095	V	1,2

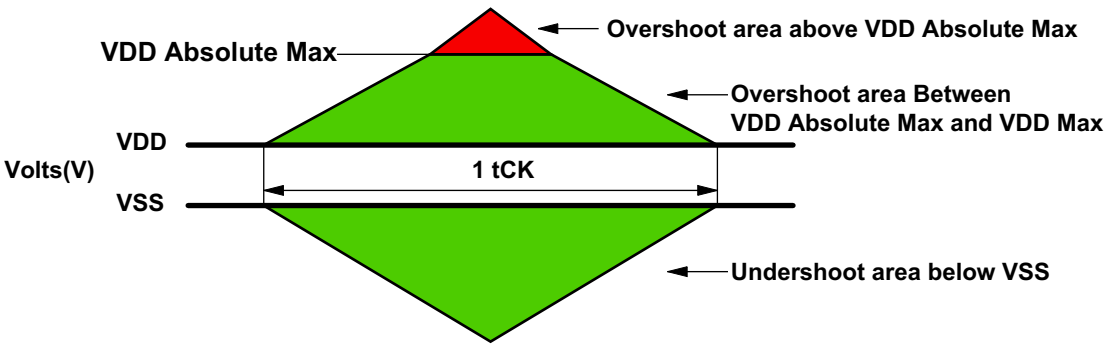
NOTE :

1. For CK, $\overline{CK}$ use VIH.CA/VIL.CA(AC) of address/command
2. VIH(AC)/VIL(AC) for address/command is based on VREFCA
3. These values are not defined, however the single-ended signals CK - $\overline{CK}$ need to be within the respective limits (VIH.CA(DC) max, VIL.CA(DC) min) for single-ended signals as well as the limitations for overshoot and undershoot.

AC overshoot/undershoot specification for Address, Command, and Control pins

Parameter	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-3200	unit
Maximum peak amplitude above VDD Absolute Max allowed for overshoot area	0.06	0.06	0.06	0.06	0.06	TBD	V
Delta value between VDD Absolute Max and VDD Max allowed for overshoot area	0.24	0.24	0.24	0.24	0.24	TBD	V
Maximum peak amplitude allowed for undershoot area	0.3	0.3	0.3	0.3	0.3	TBD	V
Maximum overshoot area per 1tCK Above Absolute Max	0.0083	0.0071	0.0062	0.0055	0.0055	TBD	V-ns
Maximum overshoot area per 1tCK Between Absolute Max and VDD Max	0.2550	0.2185	0.1914	0.1699	0.1699	TBD	V-ns
Maximum undershoot area per 1tCK Below VSS	0.2644	0.2265	0.1984	0.1762	0.1762	TBD	V-ns
(A0-A13,A17,BG0-BG1,BA0-BA1,$\overline{ACT}$,$\overline{RAS}$/A16,$\overline{CAS}$/A15,$\overline{WE}$/A14,$\overline{CS}$,CKE,ODT,C2-C0)							

Address, Command, and Control Overshoot and Undershoot Definition

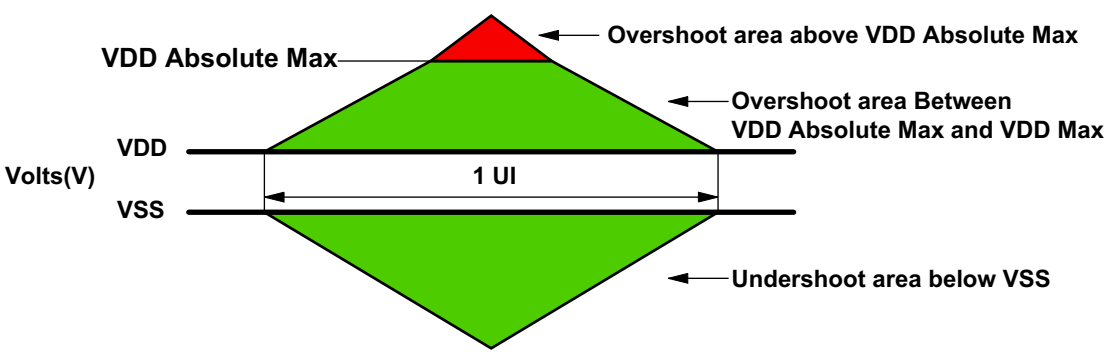


AC overshoot/undershoot specification for Clock

Parameter	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-3200	unit
Maximum peak amplitude above VDD Absolute Max allowed for overshoot area	0.06	0.06	0.06	0.06	0.06	TBD	V
Delta value between VDD Absolute Max and VDD Max allowed for overshoot area	0.24	0.24	0.24	0.24	0.24	TBD	V
Maximum peak amplitude allowed for undershoot area	0.3	0.3	0.3	0.3	0.3	TBD	V
Maximum overshoot area per 1UI Above Absolute Max	0.0038	0.0032	0.0028	0.0025	0.0025	TBD	V-ns
Maximum overshoot area per 1UI Between Absolute Max and VDD Max	0.1125	0.0964	0.0844	0.0750	0.0750	TBD	V-ns
Maximum undershoot area per 1UI Below VSS	0.1144	0.0980	0.0858	0.0762	0.0762	TBD	V-ns

(CK, $\overline{CK}$)

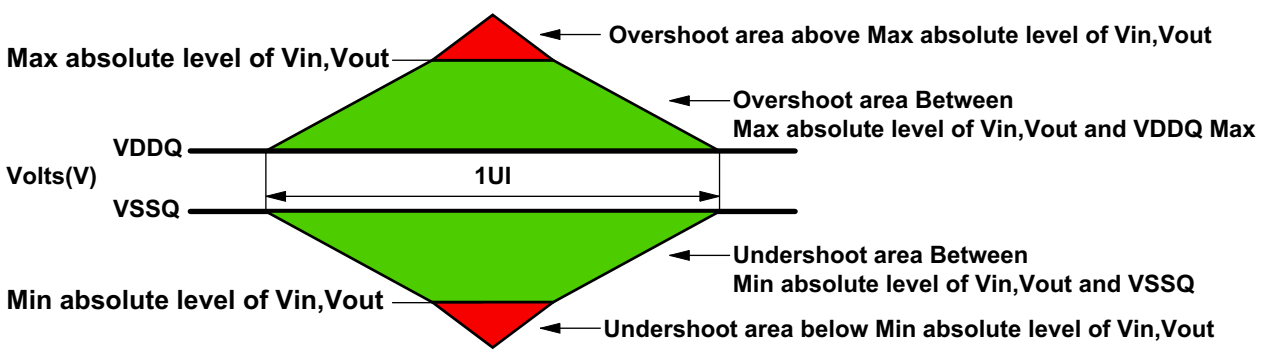
Clock Overshoot and Undershoot Definition



AC overshoot/undershoot specification for Data, Strobe and Mask

Parameter	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-3200	unit
Maximum peak amplitude above Max absolute level of Vin, Vout	0.16	0.16	0.16	0.16	0.16	TBD	V
Overshoot area Between Max Absolute level of Vin, Vout and VDDQ Max	0.24	0.24	0.24	0.24	0.24	TBD	V
Undershoot area Between Min absolute level of Vin, Vout and VSSQ	0.30	0.30	0.30	0.30	0.30	TBD	V
Maximum peak amplitude below Min absolute level of Vin, Vout	0.10	0.10	0.10	0.10	0.10	TBD	V
Maximum overshoot area per 1UI Above Max absolute level of Vin, Vout	0.0150	0.0129	0.0113	0.0100	0.0100	TBD	V-ns
Maximum overshoot area per 1UI Between Max absolute level of Vin, Vout and VDDQ Max	0.1050	0.0900	0.0788	0.0700	0.0700	TBD	V-ns
Maximum undershoot area per 1UI Between Min absolute level of Vin, Vout and VSSQ	0.1050	0.0900	0.0788	0.0700	0.0700	TBD	V-ns
Maximum undershoot area per 1UI Below Min absolute level of Vin, Vout	0.0150	0.0129	0.0113	0.0100	0.0100	TBD	V-ns
(DQ, DQS, $\overline{\text{DQS}}$, $\overline{\text{DM}}$, $\overline{\text{DBI}}$, TDQS, $\overline{\text{TDQS}}$)							

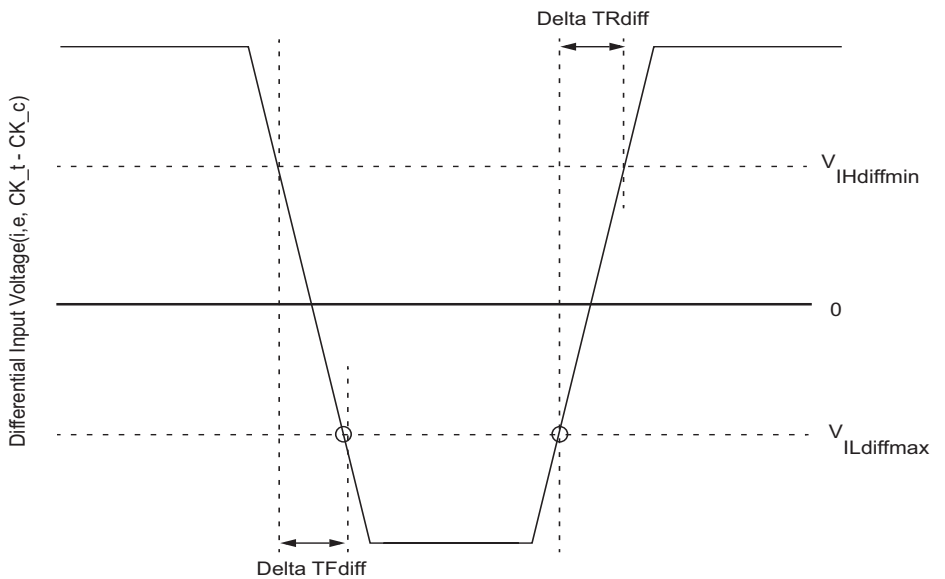
Data, Strobe and Mask Overshoot and Undershoot Definition



Slew Rate Definitions for Differential Input Signals (CK)

Description	Measured		Defined by
	From	To	
Differential input slew rate for rising edge (CK-$\overline{CK}$)	VILdiff (max)	VIHdiff (min)	VIHdiff (min) - VILdiff (max) / Delta TRdiff
Differential input slew rate for falling edge (CK-$\overline{CK}$)	VIHdiff (min)	VILdiff (max)	VIHdiff (min) - VILdiff (max) / Delta TFdiff

Differential Input Slew Rate Definition for CK, $\overline{CK}$

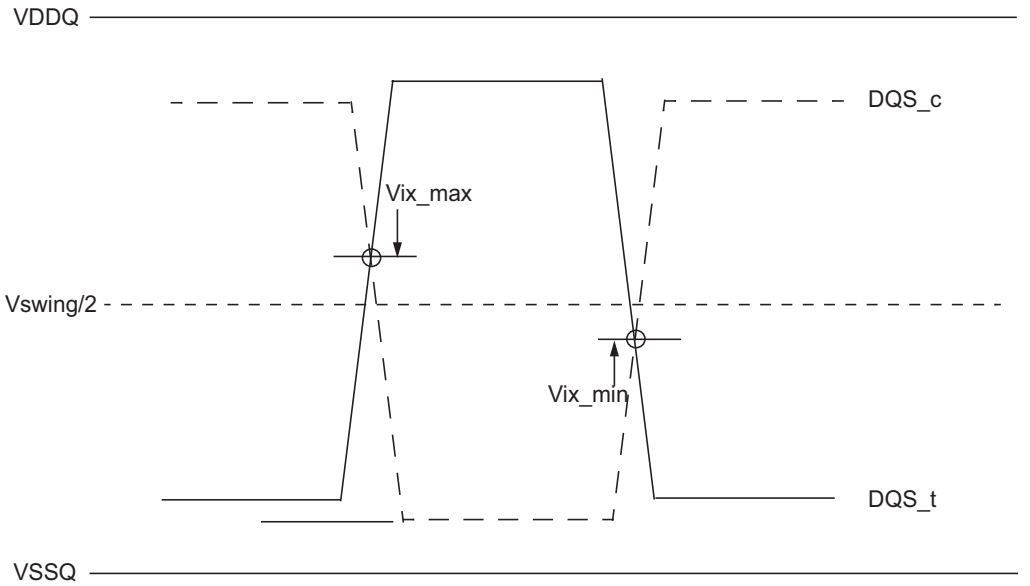


Cross point voltage for differential input signals (CK)

Symbol	Parameter	DDR4-1600/1866/2133/2400/2666/3200		Units	Notes
		Min.	Max.		
VIX(CK)	Differential Input Cross Point Voltage rela-tive to VDD/2 for CK, $\overline{CK}$	-120	120	mV	2
		-TBD	+TBD	mV	1

NOTE 1 Extended range for Vix is only allowed for clock and if single-ended clock input signals CK and $\overline{CK}$ are monotonic with a single-ended swing VSEL / VSEH of at least VDD/2 +/- TBD mV, and when the differential slew rate of CK - $\overline{CK}$ is larger than 3 V/ns. Refer to TBD for VSEL and VSEH standard values.
NOTE 2 The relation between Vix Min/Max and VSEL/VSEH should satisfy following.
(VDD/2) + Vix (Min) - VSEL >= 25mV
VSEH - ((VDD/2) + Vix (Max)) >= 25mV

Vix Definition (DQS)



Cross point voltage for differential input signals (DQS)

Symbol	Parameter	DDR4-1600/1866/2133		DDR4-2400/2666		Units	Notes
		Min.	Max.	Min.	Max.		
Vix_DQS_ratio	DQS Differential input crosspoint voltage ratio	-	25	-	25	%	1,2

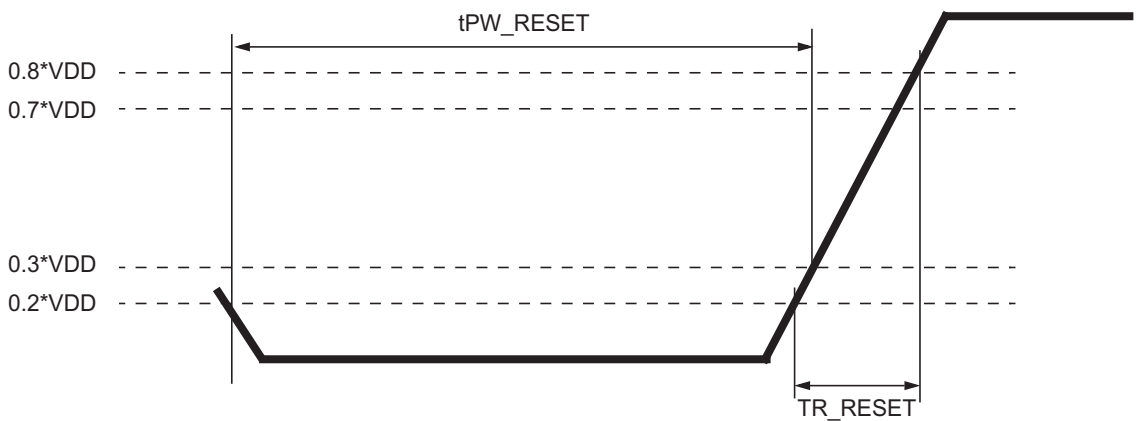
NOTE 1 Referenced to Vswing/2=avg 0.5(VDQS_t + VDQS_c) where the average is over tbd UI.
NOTE 2 Ratio of the Vix pk voltage divided by Vdiff_DQS : Vix_DQS_Ratio = 100* (Vix_DQS/Vdiff DQS pk-pk) where VdiffDQS pk-pk = 2*|VDQS - $\overline{\text{VDQS}}$| .

CMOS rail to rail Input Levels for $\overline{RESET}$

Parameter	Symbol	Min	Max	Unit	NOTE
AC Input High Voltage	VIH(AC)_RESET	0.8*VDD	VDD	V	6
DC Input High Voltage	VIH(DC)_RESET	0.7*VDD	VDD	V	2
DC Input Low Voltage	VIL(DC)_RESET	VSS	0.3*VDD	V	1
AC Input Low Voltage	VIL(AC)_RESET	VSS	0.2*VDD	V	7
Rising time	TR_RESET	-	1.0	ns	4
RESET pulse width	tPW_RESET	1.0	-	ns	3,5

NOTE 1 After $\overline{RESET}$ is registered LOW, $\overline{RESET}$ level shall be maintained below VIL(DC)_RESET during tPW_RESET, otherwise, SDRAM may not bereset.
NOTE 2 Once $\overline{RESET}$ is registered HIGH, $\overline{RESET}$ level must be maintained above VIH(DC)_RESET, otherwise, SDRAM operation will not beguaranteed until it is reset asserting $\overline{RESET}$ signal LOW.
NOTE 3 RESET is destructive to data contents.
NOTE 4 No slope reversal (ringback) requirement during its level transition from Low to High.
NOTE 5 This definition is applied only “Reset Procedure at Power Stable”.
NOTE 6 Overshoot might occur. It should be limited by the Absolute Maximum DC Ratings.
NOTE 7 Undershoot might occur. It should be limited by Absolute Maximum DC Ratings.

$\overline{RESET}$ Input Slew Rate Definition



AC & DC Logic input levels for single-ended signals

Single-ended AC & DC input levels for Command and Address

Symbol	Parameter	DDR4-1600/1866/2133/2400		DDR4-2666/3200		Units	Notes
		Min.	Max.	Min.	Max.		
V_{IHCA} (DC75)	DC input logic high	V_{REFCA} + 0.075	VDD	V_{REFCA} + 0.075	VDD	V	
V_{ILCA} (DC75)	DC input logic low	VSS	V_{REFCA} - 0.075	VSS	V_{REFCA} - 0.075	V	
V_{IHCA} (AC100)	AC input logic high	V_{REF} + 0.1	Note2	V_{REF} + 0.1	Note2	V	1
V_{ILCA} (AC100)	AC input logic low	Note2	V_{REF} - 0.175	Note2	V_{REF} - 0.175	V	1
V_{REFCA} (DC)	Reference voltage for ADD, CMD inputs	0.49 * VDD	0.51 * VDD	0.49 * VDD	0.51 * VDD	V	2,3

NOTE :
1. See “Overshoot and Undershoot Specifications”.
2. The AC peak noise on VREFCA may not allow VREFCA to deviate from VREFCA(DC) by more than ± 1% VDD (for reference : approx. ± 12mV).
3. For reference : approx. VDD/2 ± 12mV.

AC and DC output Measurement levels

Single-ended AC & DC output levels

Symbol	Parameter	DDR4-1600/1866/2133/2400/ 2666/3200	Units	Notes
VOH(DC)	DC output high measurement level (for IV curve linearity)	1.1 x VDDQ	V	
VOM(DC)	DC output mid measurement level (for IV curve linearity)	0.8 x VDDQ	V	
VOL(DC)	DC output low measurement level (for IV curve linearity)	0.5 x VDDQ	V	
VOH(AC)	AC output high measurement level (for output SR)	(0.7 + 0.15) x VDDQ	V	1
VOL(AC)	AC output low measurement level (for output SR)	(0.7 - 0.15) x VDDQ	V	1

NOTE :
1. The swing of ± 0.15 x VDDQ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7ohm and an effective test load of 50ohm to VTT = VDDQ.

Differential AC & DC Output Levels

Symbol	Parameter	DDR4-1600/1866/2133/ 2400/2666/3200	Units	Notes
VOHdiff(AC)	AC differential output high measurement level (for output SR)	+0.3 x VDDQ	V	1
VOLdiff(AC)	AC differential output low measurement level (for output SR)	-0.3 x VDDQ	V	1

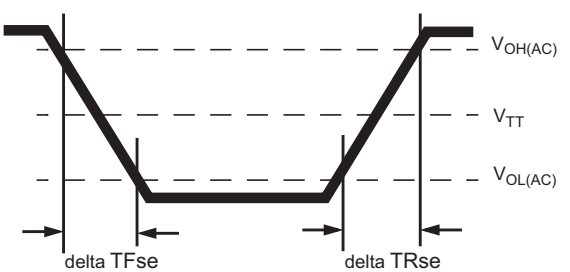
NOTE :
1. The swing of ± 0.3 x VDDQ is based on approximately 50% of the static differential output peak-to-peak swing with a driver impedance of RZQ/7ohm and an effective test load of 50ohm to VTT = VDDQ at each of the differential outputs.

Single-ended Output Slew Rate

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	VOL(AC)	VOH(AC)	$\frac{VOH(AC)-VOL(AC)}{Delta\ TRse}$
Single ended output slew rate for falling edge	VOH(AC)	VILdiff (max)	$\frac{VOH(AC)-VOL(AC)}{Delta\ TFse}$

NOTE :
1. Output slew rate is verified by design and characterization, and may not be subject to production test.

Single-ended Output Slew Rate Definition



Single-ended Output Slew Rate

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		DDR4-3200		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Single ended output slew rate	SRQse	4	9	4	9	4	9	4	9	4	9	TBD	TBD	V/ns

Description: SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
se: Single-ended Signals
For Ron = RZQ/7 setting

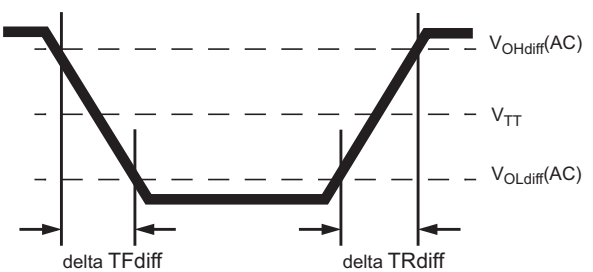
NOTE 1 In two cases, a maximum slew rate of 12 V/ns applies for a single DQ signal within a byte lane.
-Case 1 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e. they stay at either high or low).
-Case 2 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while allremaining DQ signals in the same byte lane are switching into the opposite direction (i.e. from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 9 V/ns applies.

Differential Output Slew Rate

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	VOLdiff(AC)	VOHdiff(AC)	VOHdiff(AC)-VOLdiff(AC) / Delta TRdiff
Differential output slew rate for falling edge	VOHdiff(AC)	VOLdiff(AC)	VOHdiff(AC)-VOLdiff(AC) / Delta TFdiff

NOTE :
1. Output slew rate is verified by design and characterization, and may not be subject to production test.

Differential Output Slew Rate Definition



Differential Output Slew Rate

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		DDR4-3200		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Differential output slew rate	SRQdiff	8	18	8	18	8	18	8	18	8	18	TBD	TBD	V/ns

Description: SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
diff: Differential Signals
For Ron = RZQ/7 setting

Speed Bin

DR4-1600 Speed Bins and Operations

Speed Bin				DDR4-1600		Unit	Notes
CL-nRCD-nRP				11-11-11			
Parameter			Symbol	Min	Max		
Internal read command to first data			tAA	13.75[14] (13.50)[5,12]	18.00	ns	
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 2nCK	tAA(min) + 2nCK	ns	
ACT to internal read or write delay time			tRCD	13.75 (13.50)[5,12]	-	ns	
PRE command period			tRP	13.75 (13.50)[5,12]	-	ns	
ACT to PRE command period			tRAS	35	9 x tREFI	ns	
ACT to ACT or REF command period			tRC	48.75 (46.50)[5,12]	-	ns	
	Normal	Read DBI					
CWL=9	CL=9	CL=11 (Optional)[5]	tCK(avg)	1.5 (Optional)[5,12]	1.6	ns	1,2,3,4,11,14
	CL=10	CL=12	tCK(avg)	Reserved		ns	1,2,3,11
CWL=9,11	CL=11	CL=13	tCK(avg)	1.25 (Optional)[5,12]	<1.5	ns	1,2,3,4,7
	CL=12	CL=14	tCK(avg)	1.25	<1.5	ns	1,2,3,7
Supported CL setting				9,11 ,12		nCK	13,14
Supported CL Settings with read DBI				11,13,14		nCK	
Supported CWL setting				9, 11,		nCK	

DDR4-1866 Speed Bins and Operations

Speed Bin				DDR4-1866		Unit	Notes
CL-nRCD-nRP				13-13-13			
Parameter			Symbol	Min	Max		
Internal read command to first data			tAA	13.92[14] (13.50)[5,12]	18.00	ns	
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 2nCK	tAA(min) + 2nCK	ns	
ACT to internal read or write delay time			tRCD	13.92 (13.50)[5,12]	-	ns	
PRE command period			tRP	13.92 (13.50)[5,12]	-	ns	
ACT to PRE command period			tRAS	34	9 x tREFI	ns	
ACT to ACT or REF command period			tRC	47.92 (47.50)[5,12]	-	ns	
	Normal	Read DBI					
CWL=9	CL=9	CL=11 (Optional)[5]	tCK(avg)	1.5 (Optional)[5,12]	1.6	ns	1,2,3,4,11,14
	CL=10	CL=12	tCK(avg)	Reserved		ns	1,2,3,11
CWL=9,11	CL=11	CL=13	tCK(avg)	1.25 (Optional)[5,12]	<1.5	ns	1,2,3,4,7
	CL=12	CL=14	tCK(avg)	1.25	<1.5	ns	1,2,3,7
CWL=10,12	CL=13	CL=15	tCK(avg)	1.071 (Optional)[5,12]	<1.25	ns	1,2,3,4,7
	CL=14	CL=16	tCK(avg)	1.071	<1.25	ns	1,2,3,7
Supported CL setting				9,11,12,13,14		nCK	13,14
Supported CL Settings with read DBI				11,13,14,15,16		nCK	
Supported CWL setting				9,10, 11,12		nCK	

DDR4-2133 Speed Bins and Operations

Speed Bin				DDR4-2133		Unit	Notes
CL-nRCD-nRP				15-15-15			
Parameter			Symbol	Min	Max		
Internal read command to first data			tAA	14.06[14] (13.50)[5,12]	18.00	ns	
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 3nCK	tAA(min) + 3nCK	ns	
ACT to internal read or write delay time			tRCD	14.06 (13.50)[5,12]	-	ns	
PRE command period			tRP	14.06 (13.50)[5,12]	-	ns	
ACT to PRE command period			tRAS	33	9 x tREFI	ns	
ACT to ACT or REF command period			tRC	47.06 (46.50)[5,12]	-	ns	
	Normal	Read DBI					
CWL=9	CL=9	CL=11 (Optional)[5]	tCK(avg)	1.5 (Optional)[5,12]	1.6	ns	1,2,3,4,11,14
	CL=10	CL=12	tCK(avg)	Reserved		ns	1,2,3,11
CWL=9,11	CL=11	CL=13	tCK(avg)	1.25 (Optional)[5,12]	<1.5	ns	1,2,3,4,7
	CL=12	CL=14	tCK(avg)	1.25	<1.5	ns	1,2,3,7
CWL=10,12	CL=13	CL=15	tCK(avg)	1.071 (Optional)[5,12]	<1.25	ns	1,2,3,4,7
	CL=14	CL=16	tCK(avg)	1.071	<1.25	ns	1,2,3,7
CWL=11,14	CL=14	CWL=17	tCK(avg)	Reserved		ns	1,2,3,4
	CL=15	CWL=18	tCK(avg)	0.938	< 1.071	ns	1,2,3,4
	CL=16	CWL=19	tCK(avg)	0.938	< 1.071	ns	1,2,3
Supported CL setting				9,11,12,13,14,15,16		nCK	13,14
Supported CL Settings with read DBI				11,13,14,15,16,18,19		nCK	
Supported CWL setting				9,10,11 ,12,14		nCK	

DDR4-2400 Speed Bins and Operations

Speed Bin				DDR4-2400		Unit	Notes
CL-nRCD-nRP				17-17-17			
Parameter			Symbol	Min	Max		
Internal read command to first data			tAA	14.16	18.00	ns	
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 3nCK	tAA(min) + 3nCK	ns	
ACT to internal read or write delay time			tRCD	14.16	-	ns	
PRE command period			tRP	14.16	-	ns	
ACT to PRE command period			tRAS	32	9 x tREFI	ns	
ACT to ACT or REF command period			tRC	46.16	-	ns	
	Normal	Read DBI					
CWL=9	CL=9	CL=11 (Optional)[5]	tCK(avg)	1.5 (Optional)[5,12]	1.6	ns	1,2,3,4,11
	CL=10	CL=12	tCK(avg)	Reserved		ns	1,2,3,4,11
CWL=9,11	CL=10	CL=12	tCK(avg)	Reserved		ns	4
	CL=11	CL=13	tCK(avg)	1.25	<1.5	ns	1,2,3,4,8
	CL=12	CL=14	tCK(avg)	1.25	<1.5	ns	1,2,3,8
CWL=10,12	CL=12	CL=14	tCK(avg)	Reserved		ns	4
	CL=13	CL=15	tCK(avg)	1.071	<1.25	ns	1,2,3,4,8
	CL=14	CL=16	tCK(avg)	1.071	<1.25	ns	1,2,3,8
CWL=11,14	CL=14	CWL=17	tCK(avg)	Reserved		ns	4
	CL=15	CWL=18	tCK(avg)	0.938	< 1.071	ns	1,2,3,4,8
	CL=16	CWL=19	tCK(avg)	0.938	< 1.071	ns	1,2,3,8
CWL=12,16	CL=15	CWL=18	tCK(avg)	Reserved		ns	1,2,3,4
	CL=16	CWL=19	tCK(avg)	0.833	< 0.938	ns	1,2,3,4
	CL=18	CWL=21	tCK(avg)	0.833	< 0.938	ns	1,2,3
Supported CL setting				9,11,12,13,14,15,16,18		nCK	13
Supported CL Settings with read DBI				11,13,14,15,16,18,19,21		nCK	
Supported CWL setting				9,10,11,12,14,16		nCK	

DDR4-2666 Speed Bins and Operations

Speed Bin				DDR4-2666		Unit	Notes
CL-nRCD-nRP				19-19-19			
Parameter			Symbol	Min	Max		
Internal read command to first data			tAA	14.25	18.00	ns	12
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 3nCK	tAA(min) + 3nCK	ns	12
ACT to internal read or write delay time			tRCD	14.25	-	ns	12
PRE command period			tRP	14.25	-	ns	12
ACT to PRE command period			tRAS	32	9 x tREFI	ns	12
ACT to ACT or REF command period			tRC	46.25	-	ns	12
	Normal	Read DBI					
CWL=9	CL=9	CL=11 (Optional)[5]	tCK(avg)	1.5 (Optional)[5,12]	1.6	ns	1,2,3,4,11
	CL=10	CL=12	tCK(avg)	Reserved		ns	1,2,3,4,11
CWL=9,11	CL=10	CL=12	tCK(avg)	Reserved		ns	4
	CL=11	CL=13	tCK(avg)	1.25	<1.5	ns	1,2,3,4,8
	CL=12	CL=14	tCK(avg)	1.25	<1.5	ns	1,2,3,8
CWL=10,12	CL=12	CL=14	tCK(avg)	Reserved		ns	4
	CL=13	CL=15	tCK(avg)	1.071	<1.25	ns	1,2,3,4,8
	CL=14	CL=16	tCK(avg)	1.071	<1.25	ns	1,2,3,8
CWL=11,14	CL=14	CWL=17	tCK(avg)	Reserved		ns	4
	CL=15	CWL=18	tCK(avg)	0.938	< 1.071	ns	1,2,3,4,8
	CL=16	CWL=19	tCK(avg)	0.938	< 1.071	ns	1,2,3,8
CWL=12,16	CL=15	CWL=18	tCK(avg)	Reserved		ns	1,2,3,4
	CL=16	CWL=19	tCK(avg)	0.833	< 0.937	ns	1,2,3,4
	CL=18	CWL=21	tCK(avg)	0.833	< 0.937	ns	1,2,3
CWL=12,16	CL=18	CWL=21	tCK(avg)	Reserved		ns	1,2,3,4
	CL=19	CWL=22	tCK(avg)	0.75	< 0.833	ns	1,2,3,4
	CL=20	CWL=23	tCK(avg)	0.75	< 0.833	ns	1,2,3
Supported CL setting				10,11,12,13,14,15,16,18, 19,20		nCK	16
Supported CL Settings with read DBI				12,13,14,15,16,18,19,21, 22,23		nCK	16
Supported CWL setting				9,10,11,12,14,16,18		nCK	16

Speed Bin Table Notes

Absolute Specification

- VDDQ = VDD = 1.20V +/- 0.06 V
- VPP = 2.5V +0.25/-0.125 V
- The values defined with above-mentioned table are DLL ON case.
- DDR4-1600, 1866, 2133 and 2400 Speed Bin Tables are valid only when Geardown Mode is disabled.

1. The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. ttCK(avg).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(avg) value (1.5, 1.25, 1.071, 0.938 or 0.833 ns) when calculating CL [nCK] = tAA [ns] / tCK(avg) [ns], rounding up to the next “Supported CL”, where tAA = 12.5ns and tCK(avg) = 1.3 ns should only be used for CL = 10 calculation.
3. tCK(avg).MAX limits: Calculate tCK(avg) = tAA.MAX / CL SELECTED and round the resulting tCK(avg) down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071 ns or 0.938 ns or 0.833 ns). This result is tCK(avg).MAX corresponding to CL SELECTED.
4. ‘Reserved’ settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.
6. Any DDR4-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any DDR4-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. Any DDR4-2400 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
9. Reserved for DDR4-2666 speed bin.
10. Reserved for DDR4-3200 speed bin.
11. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.
12. For devices supporting optional down binning to CL=9, CL=11 and CL=13, tAA/tRCD/tRPmin must be 13.5ns or lower. SPD settings must be programmed to match.For example, DDR4-1600K devices supporting down binning to 1333MT/s should program 13.5ns in SPD bytes for tAAmin (Byte 24), tRCDmin (Byte 25), and tRPmin (Byte 26).DDR4-1866M devices supporting down binning to 1333MT/s or DDR4-1600K should program 13.5ns in SPD bytes for tAAmin (Byte 24), tRCDmin (Byte 25), and tRPmin (Byte 26).DDR4-2133P devices supporting down binning to 1333MT/s or DDR4-1600K or DDR4-1866M should program 13.5ns in SPD bytes for tAAmin (Byte 24), tRCDmin (Byte 25), and tRPmin (Byte 26).tRCmin (Byte 27, 29) also should be programmed accordingly. For example, 48.5ns (tRASmin + tRPmin = 35ns+ 13.5ns) is set to supporting optional down binning CL=9 and CL=11.
13. CL number in parentheses, it means that these numbers are optional.
14. DDR4 SDRAM supports CL=9 as long as a system meets tAA(min).
15. Each speed bin lists the timing requirements that need to be supported in order for a given DRAM to be JEDEC compliant. JEDEC compliance does not require support for all speed bins within a given speed. JEDEC compliance requires meeting the parameters for a least one of the listed speed bins.
16. Supporting CL setting herewith is a reference base on JEDEC’s. Precise CL & tCK setting needs to follow where defined on speed compatible table in section “Operating frequence”, exceptional setting please confirm with NTC.CWL setting follow CL value in above table in section “Speed Bin”

IDD and IDDQ Specification Parameters and Test conditions

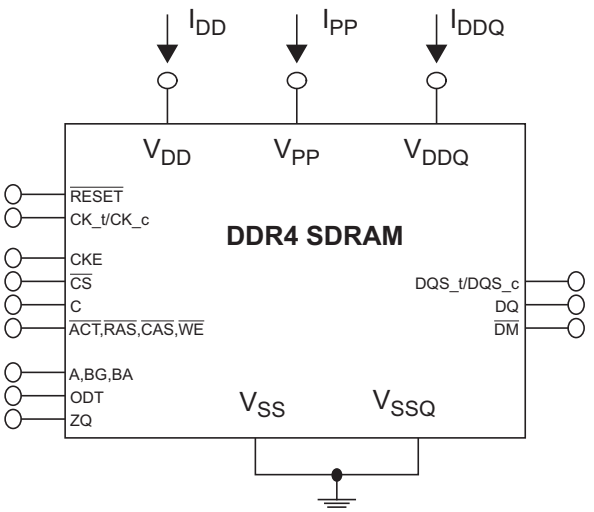
IDD, IPP and IDDQ Measurement Conditions

In this chapter, IDD, IPP and IDDQ measurement conditions such as test load and patterns are defined. The figure below shows the setup and test load for IDD, IPP and IDDQ measurements.

-IDD currents (such as IDD0, IDD0A, IDD1, IDD1A, IDD2N, IDD2NA, IDD2NL, IDD2NT, IDD2P, IDD2Q, IDD3N, IDD3NA, IDD3P, IDD4R, IDD4RA, IDD4W, IDD4WA, IDD5B, IDD5F2, IDD5F4, IDD6N, IDD6E, IDD6R, IDD6A, IDD7 and IDD8) are measured as time-averaged currents with all VDD balls of the DDR4 SDRAM under test tied together. Any IPP or IDDQ current is not included in IDD currents.
-IPP currents have the same definition as IDD except that the current on the VPP supply is measured.
-IDDQ currents (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR4 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.
Attention: IDDQ values cannot be directly used to calculate IO power of the DDR4 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 184. In DRAM module application, IDDQ cannot be measured separately since VDD and VDDQ are using one merged-power layer in Module PCB.

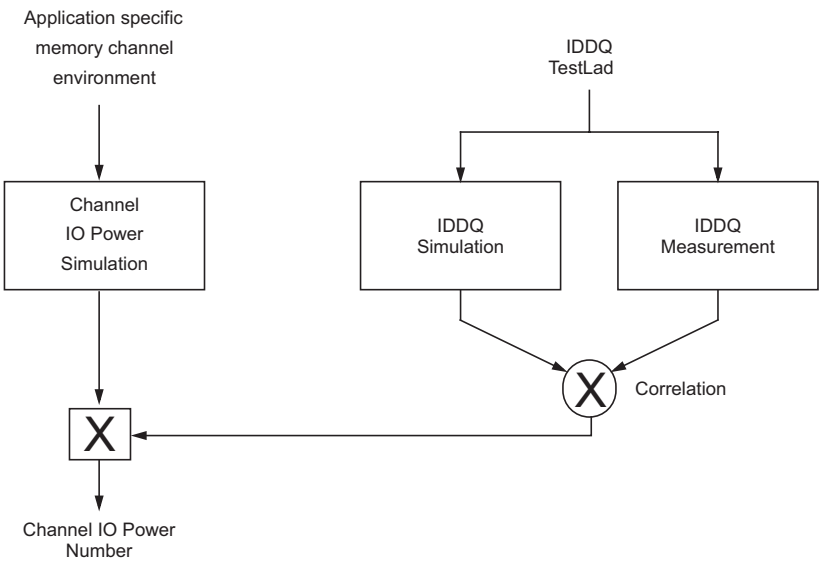
For IDD, IPP and IDDQ measurements, the following definitions apply:
-'0' and 'LOW' is defined as VIN <= VILAC(max).
-'1' and 'HIGH' is defined as VIN >= VIHAC(min).
-'MID-LEVEL' is defined as inputs are VREF = VDD / 2.
-Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns are provided in table below.
-Basic IDD, IPP and IDDQ Measurement Conditions are described.
-Detailed IDD, IPP and IDDQ Measurement-Loop Patterns are described.
-IDD Measurements are done after properly initializing the DDR4 SDRAM. This includes but is not limited to setting
RON = RZQ/7 (34 Ohm in MR1);
RTT_NOM = RZQ/6 (40 Ohm in MR1);
RTT_WR = RZQ/2 (120 Ohm in MR2);
RTT_PARK = Disable;
Qoff = 0B (Output Buffer enabled) in MR1;
TDQS_t disabled in MR1;
CRC disabled in MR2;
CA parity feature disabled in MR5;
Gear down mode disabled in MR3;
Read/Write DBI disabled in MR5;
DM disabled in MR5
-Attention: The IDD, IPP and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.
-Define D = {$\overline{CS}$, $\overline{ACT}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$} := {HIGH, LOW, LOW, LOW, LOW}
-Define D# = {$\overline{CS}$, $\overline{ACT}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$} := {HIGH, HIGH, HIGH, HIGH, HIGH}

Measurement Setup and Test Load for IDD, IPP and IDDQ Measurements



NOTE 1 DIMM level Output test load condition may be different from above.

Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement



Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns

Symbol		DDR4-2133	DDR4-2400	DDR4-2666	Unit
		15-15-15	17-17-17	19-19-19	
tCK		0.938	0.833	0.75	ns
CL		15	17	18	nCK
CWL		14	16	18	nCK
nRCD		15	17	18	nCK
nRC		51	56	62	nCK
nRAS		36	39	43	nCK
nRP		15	16	18	nCK
nFAW	x4	16	16	16	nCK
	x8	23	26	28	nCK
	x16	32	36	40	nCK
nRRDS	x4	4	4	4	nCK
	x8	4	4	4	nCK
	x16	6	7	8	nCK
nRRDL	x4	6	6	7	nCK
	x8	6	6	7	nCK
	x16	7	8	9	nCK
tCCD_S		4	4	4	nCK
tCCD_L		6	6	7	nCK
tWTR_S		3	3	4	nCK
tWTR_L		8	9	10	nCK
nRFC 2Gb		171	193		nCK
nRFC 4Gb		278	313	347	nCK
nRFC 8Gb		374	421	467	nCK
nRFC 16Gb		TBD	TBD	TBD	nCK

IDD Specifications

Conditions	Symbol	Data rate (Mbps)	IDD max.		Unit
			X8	X16	
Operating One Bank Active-Precharge Current (AL=0); CKE: High; External clock: On; tCK, nRC, nRAS, CL: see IDD timing Table; BL: 8[1]; AL: 0; $\overline{CS}$: High between ACT and PRE; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to IDD loop table; Data IO: VDDQ; $\overline{DM}$: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... (see IDD loop table); Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0; Pattern Details: see IDD loop table	IDD0	2133 2400 2666	80 95 105	90 96 110	mA
Operating One Bank Active-Precharge Current (AL=CL-1); AL = CL-1, Other conditions: see IDD0	IDD0A	2133 2400 2666	80 95 105	90 96 110	mA
Operating One Bank Active-Precharge IPP Current; Same condition with IDD0	IPP0	2133 2400 2666	4 4.5 5	6.5 7 8	mA
Operating One Bank Active-Read-Precharge Current (AL=0); CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: see IDD timing Table; BL: 8[1]; AL: 0; $\overline{CS}$: High between ACT, RD and PRE; Command, Address, Bank Group Address, Bank Address Inputs, Data IO: partially toggling according to IDD loop table; $\overline{DM}$: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... (see IDD loop table); Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: see IDD loop table	IDD1	2133 2400 2666	95 105 115	115 125 135	mA
Operating One Bank Active-Read-Precharge Current (AL=CL-1); AL = CL-1, Other conditions: see IDD1	IDD1A	2133 2400 2666	105 115 120	120 130 145	mA
Operating One Bank Active-Read-Precharge IPP Currentt; Same condition with IDD1	IPP1	2133 2400 2666	4 4.5 5	6 7 8	mA
Precharge Standby Current (AL=0); CKE: High; External clock: On; tCK, CL: see IDD timing Table; BL: 8[1]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to IDD loop table; Data IO: VDDQ; $\overline{DM}$: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: see IDD loop table	IDD2N	2133 2400 2666	68 68 68	70 70 70	mA
Precharge Standby Current (AL=CL-1); AL = CL-1, Other conditions: see IDD2N	IDD2NA	2133 2400 2666	68 68 68	70 70 70	mA
Precharge Standby IPP Current; Same condition with IDD2N	IPP2N	2133 2400 2666	2 2 2	2.5 2.5 2.5	mA
Precharge Standby ODT Current; CKE: High; External clock: On; tCK, CL: see IDD timing Table; BL: 8[1]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according toIDD loop table; Data IO: VSSQ; $\overline{DM}$: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: toggling according to IDD loop table; Pattern Details: see IDD loop table	IDD2NT	2133 2400 2666	100 110 120	115 125 135	mA

Conditions	Symbol	Data rate (Mbps)	IDD max.		Unit
			X8	X16	
Precharge Standby ODT IDDQ Current; Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current	IDDQ2NT	2133 2400 2666	6 6 6	8 8 8	mA
Precharge Standby Current with CAL enabled; Same definition like for IDD2N, CAL enabled[3]	IDD2NL	2133 2400 2666	32 35 38	32 36 40	mA
Precharge Standby Current with Gear Down mode enabled; Same definition like for IDD2N, Gear Down mode enabled[3]	IDD2NG	2133 2400 2666	64 66 70	66 68 72	mA
Precharge Standby Current with DLL disabled; Same definition like for IDD2N, DLL disabled[3]	IDD2ND	2133 2400 2666	64 66 70	66 68 72	mA
Precharge Standby Current with CA parity enabled; Same definition like for IDD2N, CA parity enabled[3]	IDD2N_par	2133 2400 2666	64 66 70	66 68 72	mA
Precharge Power-Down Current; CKE: Low; External clock: On; tCK, CL: see IDD timing Table; BL: 81; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; $\overline{DM}$: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0	IDD2P	2133 2400 2666	40 40 40	40 40 40	mA
Precharge Power-Down IPP Current; Same condition with IDD2P	IPP2P	2133 2400 2666	2 2 2	2.5 2.5 2.5	mA
Precharge Quiet Standby Current; CKE: High; External clock: On; tCK, CL: see IDD timing Table; BL: 81; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; $\overline{DM}$: stable at 1;Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0	IDD2Q	2133 2400 2666	46 48 50	46 48 50	mA
Active Standby Current; CKE: High; External clock: On; tCK, CL: see IDD timing Table; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to IDD loop table; Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: IDD loop table	IDD3N	2133 2400 2666	86 99 104	86 99 104	mA
Active Standby Current (AL=CL-1); AL = CL-1, Other conditions: see IDD3N	IDD3NA	2133 2400 2666	96 106 110	96 106 110	mA
Active Standby IPP Current; Same condition with IDD3N	IPP3N	2133 2400 2666	1.8 1.8 1.8	2 2 2	mA

Conditions	Symbol	Data rate (Mbps)	IDD max.		Unit
			X8	X16	
Active Power-Down Current; CKE: Low; External clock: On; tCK, CL: see IDD timing Table; BL: 81; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; $\overline{DM}$: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	IDD3P	2133 2400 2666	68 68 68	70 70 70	mA
Active Power-Down IPP Current; Same condition with IDD3P	IPP3P	2133 2400 2666	1.8 1.8 1.8	2 2 2	mA
Operating Burst Read Current; CKE: High; External clock: On; tCK, CL: see IDD timing Table; BL: 82; AL: 0; CS_n: High between RD; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to IDD loop table; Data IO: seamless read data burst with different data between one burst and the next one according to IDD loop table; $\overline{DM}$: stable at 1; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... (see IDD loop table); Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0; Pattern Details: see IDD loop table	IDD4R	2133 2400 2666	220 230 245	300 320 340	mA
Operating Burst Read Current (AL=CL-1); AL = CL-1, Other conditions: see IDD4R	IDD4RA	2133 2400 2666	225 245 260	320 335 355	mA
Operating Burst Read Current with Read DBI; Read DBI enabled[3], Other conditions: see IDD4R	IDD4RB	2133 2400 2666	200 215 230	260 285 300	mA
Operating Burst Read IPP Current; Same condition with IDD4R	IPP4R	2133 2400 2666	1.8 1.8 1.8	2 2 2	mA
Operating Burst Read IDDQ Current; Same definition like for IDD4R, however measuring IDDQ current instead of IDD current	IDDQ4R	2133 2400 2666	36 42 45	70 75 80	mA
Operating Burst Read IDDQ Current with Read DBI; Same definition like for IDD4RB, however measuring IDDQ current instead of IDD current	IDDQ4RB	2133 2400 2666	16 18 20	32 36 40	mA
Operating Burst Write Current; CKE: High; External clock: On; tCK, CL: see IDD timing Table; BL: 8[1]; AL: 0; $\overline{CS}$: High between WR; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to IDD loop table; Data IO: seamless write data burst with different data between one burst and the next one according to IDD loop table; $\overline{DM}$: stable at 1; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... (see IDD loop table); Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at HIGH; Pattern Details: see IDD loop table	IDD4W	2133 2400 2666	270 285 310	380 400 420	mA
Operating Burst Write Current (AL=CL-1); AL = CL-1, Other conditions: see IDD4W	IDD4WA	2133 2400 2666	285 305 320	380 410 430	mA
Operating Burst Write Current with Write DBI; Write DBI enabled[3], Other conditions: see IDD4W	IDD4WB	2133 2400 2666	270 290 310	390 415 430	mA

Conditions	Symbol	Data rate (Mbps)	IDD max.		Unit
			X8	X16	
Operating Burst Write Current with Write CRC; Write CRC enabled[3], Other conditions: see IDD4W	IDD4WC	2133 2400 2666	250 265 280	385 390 420	mA
Operating Burst Write Current with CA Parity; CA Parity enabled[3], Other conditions: see IDD4W	IDD4W_par	2133 2400 2666	250 270 290	355 375 395	mA
Operating Burst Write IPP Current; Same condition with IDD4W	IPP4W	2133 2400 2666	1.8 1.8 1.8	2 2 2	mA
Burst Refresh Current (1X REF); CKE: High; External clock: On; tCK, CL, nRFC: see IDD timing Table; BL: 8[1]; AL: 0; $\overline{CS}$: High between REF; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to IDD loop table; Data IO: VDDQ; $\overline{DM}$: stable at 1; Bank Activity: REF command every nRFC (see IDD loop table); Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0; Pattern Details: see IDD loop table	IDD5B	2133 2400 2666	215 220 230	220 230 240	mA
Burst Refresh Write IPP Current (1X REF); Same condition with IDD5B	IPP5B	2133 2400 2666	60 60 60	60 60 60	mA
Burst Refresh Current (2X REF); tRFC=tRFC_x2, Other conditions: see IDD5B	IDD5F2	2133 2400 2666	190 195 200	190 200 210	mA
Burst Refresh Write IPP Current (2X REF); Same condition with IDD5F2	IPP5F2	2133 2400 2666	40 40 40	42 42 42	mA
Burst Refresh Current (4X REF); tRFC=tRFC_x4, Other conditions: see IDD5B	IDD5F4	2133 2400 2666	150 155 160	155 165 175	mA
Burst Refresh Write IPP Current (4X REF); Same condition with IDD5F4	IPP5F4	2133 2400 2666	34 34 34	36 36 36	mA
Self Refresh Current: Normal Temperature Range; TCASE: 0 - 85'C; Low Power Array Self Refresh (LP ASR) : Normal[4]; CKE: Low; External clock: Off; CK and $\overline{CK}$: LOW; CL: see IDD timing Table; BL: 8[1]; AL: 0; $\overline{CS}$, Command, Address, Bank Group Address, Bank Address, Data IO: High; $\overline{DM}$: stable at 1; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: MID-LEVEL	IDD6N	2133 2400 2666	32 32 32	32 32 32	mA
Self Refresh IPP Current: Normal Temperature Range; Same condition with IDD6N	IPP6N	2133 2400 2666	5 5 5	6.5 6.5 6.5	mA
Self-Refresh Current: Extended Temperature Range; TCASE: 0 - 95'C; Low Power Array Self Refresh (LP ASR) : Extended[4]; CKE: Low; External clock: Off; CK and $\overline{CK}$: LOW; CL: see IDD timing Table; BL: 8[1]; AL: 0; $\overline{CS}$, Command, Address, Bank Group Address, Bank Address, Data IO: High; $\overline{DM}$:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: MID-LEVEL	IDD6E	2133 2400 2666	34 38 42	34 38 42	mA

Conditions	Symbol	Data rate (Mbps)	IDD max.		Unit
			X8	X16	
Self Refresh IPP Current: Extended Temperature Range; Same condition with IDD6E	IPP6E	2133 2400 2666	8 8 8	8 8 8	mA
Self-Refresh Current: Reduced Temperature Range; TCASE: 0 - 45'C; Low Power Array Self Refresh (LP ASR) : Reduced[4]; CKE: Low; External clock: Off; CK and $\overline{CK}$: LOW; CL: see IDD timing Table; BL: 8[1]; AL: 0; $\overline{CS}$, Command, Address, Bank Group Address, Bank Address, Data IO: High; $\overline{DM}$:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: MID-LEVEL	IDD6R	2133 2400 2666	24 26 28	24 26 28	mA
Self Refresh IPP Current: Reduced Temperature Range; Same condition with IDD6R	IPP6R	2133 2400 2666	4 4 4	5 5 5	mA
Auto Self-Refresh Current; TCASE: 0 - 95'C; Low Power Array Self Refresh (LP ASR) : Auto[4];Partial Array Self-Refresh (PASR): Full Array; CKE: Low; External clock: Off; CK and $\overline{CK}$: LOW; CL: see IDD timing Table; BL: 8[1]; AL: 0; $\overline{CS}$, Command, Address, Bank Group Address, Bank Address, Data IO: High; $\overline{DM}$:stable at 1; Bank Activity: Auto Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: MID-LEVEL	IDD6A	2133 2400 2666	26 28 32	26 28 32	mA
Auto Self-Refresh IPP Current; Same condition with IDD6A	IPP6A	2133 2400 2666	4.5 4.5 4.5	6.5 6.5 6.5	mA
Operating Bank Interleave Read Current; CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: see IDD timing Table; BL: 8[1]; AL: CL-1; $\overline{CS}$: High between ACT and RDA; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to IDD loop table; Data IO: read data bursts with different data between one burst and the next one according to IDD loop table; $\overline{DM}$: stable at 1; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing, see IDD loop table; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0; Pattern Details: IDD loop table	IDD7	2133 2400 2666	220 230 240	280 200 320	mA
Operating Bank Interleave Read IPP Current; Same condition with IDD7	IPP7	2133 2400 2666	28 28 28	38 38 38	mA
Maximum Power Down Current;	IDD8	2133 2400 2666	18 20 24	18 20 24	mA
Maximum Power Down Current; Same condition with IDD8	IPP8	2133 2400 2666	2 2 2	2 2 2	mA

NOTE 1 Burst Length: BL8 fixed by MRS: set MR0 [A1:0=00].
NOTE 2 Output Buffer Enable:
- set MR1 [A12 = 0] : Qoff = Output buffer enabled
- set MR1 [A2:1 = 00] : Output Driver Impedance Control = RZQ/7
RTT_NOM enable:
- set MR1 [A10:8 = 011] : RTT_NOM = RZQ/6
RTT_WR enable:
- set MR2 [A10:9 = 01] : RTT_WR = RZQ/2

RTT_PARK disable:
- set MR5 [A8:6 = 000]
NOTE 3 CAL enabled :
- set MR4 [A8:6 =010] : 2133MT/s
- set MR4 [A8:6 =011] : 2400MT/s
Gear Down mode enabled :
- set MR3 [A3 = 1] : 1/4 Rate
DLL disabled :
- set MR1 [A0 = 0]
CA parity enabled :
- set MR5 [A2:0 = 001] : 2133MT/s
- set MR5 [A2:0 = 010] : 2400MT/s
Read DBI enabled :
- set MR5 [A12 = 1]
Write DBI enabled :
- set :MR5 [A11 = 1]
NOTE 4 Low Power Array Self Refresh (LP ASR) :
- set MR2 [A7:6 = 00] : Normal
- set MR2 [A7:6 = 01] : Reduced Temperature range
- set MR2 [A7:6 = 10] : Extended Temperature range
- set MR2 [A7:6 = 11] : Auto Self Refresh

Input/Output Capacitance

Silicon pad I/O Capacitance

Symbol	Parameter	DDR4-1600/1866/2133		DDR4-2400/2666		DDR4-2933/3200		Units	NOTE
		Min	Max	Min	Max	Min	Max		
C_{IO}	Input/output capacitance	0.55	1.4	0.55	1.4	TBD	TBD	pF	1,2,3
C_{DIO}	Input/output capacitance delta	-0.1	0.1	-0.1	0.1	TBD	TBD	pF	1,2,3,11
C_{DDQS}	Input/output capacitance delta DQS and $\overline{DQS}$	-	0.05	-	0.05	TBD	TBD	pF	1,2,3,5
C_{CK}	Input capacitance, CK and $\overline{CK}$	0.2	0.8	0.2	0.7	TBD	TBD	pF	1,3
C_{DCK}	Input capacitance delta CK and $\overline{CK}$	-	0.05	-	0.05	TBD	TBD	pF	1,3,4
C_I	Input capacitance(CTRL, ADD, CMD pins only)	0.2	0.8	0.2	0.7	TBD	TBD	pF	1,3,6
C_{DI_CTRL}	Input capacitance delta(All CTRL pins only)	-0.1	0.1	-0.1	0.1	TBD	TBD	pF	1,3,7,8
$C_{DI\_ADD\_CMD}$	Input capacitance delta(All ADD/CMD pins only)	-0.1	0.1	-0.1	0.1	TBD	TBD	pF	1,2,9,10
C_{ALERT}	Input/output capacitance of $\overline{ALERT}$	0.5	1.5	0.5	1.5	TBD	TBD	pF	1,3
C_{ZQ}	Input/output capacitance of ZQ	-	2.3	-	2.3	TBD	TBD	pF	1,3,12
C_{TEN}	Input/output capacitance of TEN	0.5	2.3	0.5	2.3	TBD	TBD	pF	1,3,13

NOTE 1 This parameter is not subject to production test. It is verified by design and characterization. The silicon only capacitance is validated by de-embedding the package L & C parasitic. The capacitance is measured with VDD, VDDQ, VSS, VSSQ applied with all other signal pins floating. Measurement procedure tbd.
NOTE 2 DQ, DM, DQS, $\overline{DQS}$, TDQS, $\overline{TDQS}$. Although the DM, TDQS and $\overline{TDQS}$ pins have different functions, the loading matches DQ and DQS.
NOTE 3 This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here.
NOTE 4 Absolute value CK-$\overline{CK}$
NOTE 5 Absolute value of CIO(DQS)-CIO($\overline{DQS}$)
NOTE 6 C_I applies to ODT, CS, CKE, A0-A17, BA0-BA1, BG0-BG1, $\overline{RAS}$/A16, $\overline{CAS}$/A15, $\overline{WE}$/A14, $\overline{ACT}$ and PAR.
NOTE 7 C_{DI_CTRL} applies to ODT, $\overline{CS}$ and CKE
NOTE 8 C_{DI_CTRL} = CI(CTRL)-0.5*(CI(CLK_T)+CI(CLK_C))
NOTE 9 $C_{DI\_ADD\_CMD}$ applies to, A0-A17, BA0-BA1, BG0-BG1,$\overline{RAS}$/A16, $\overline{CAS}$/A15, $\overline{WE}$/A14, $\overline{ACT}$ and PAR.
NOTE 10 $C_{DI\_ADD\_CMD}$ = CI(ADD_CMD)-0.5*(CI(CLK_T)+CI(CLK_C))
NOTE 11 C_{DIO} = CIO(DQ,DM)-0.5*(CIO(DQS_T)+CIO($\overline{DQS}$_C))
NOTE 12 Maximum external load capacitance on ZQ pin: tbd pF.
NOTE 13 TEN pin may be DRAM internally pulled low through a weak pull-down resistor to VSS. In this case CTEN might not be valid and system shall verify TEN signal with Vendor specific information.

DRAM package electrical specifications

Symbol	Parameter	DDR4-1600/1866 /2133		DDR4-2400/2666 /3200		Units	NOTE
		Min	Max	Min	Max		
Z_{IO}	Input/output Zpkg	45	85	45	85	Ω	1,2,3,4,5,10,11
T_{dIO}	Input/output Pkg Delay	14	42	14	42	ps	1,2,3,4,5,11
L_{io}	Input/Output Lpkg	-	3.3	-	3.3	nH	11,12
C_{io}	Input/Output Cpkg	-	0.78	-	0.78	pF	11,13
Z_{IO} DQS	DQS, $\overline{DQS}$ Zpkg	45	85	45	85	Ω	1,2,5,10,11
T_{dIO} DQS	DQS, $\overline{DQS}$ Pkg Delay	14	42	14	42	ps	1,2,5,10,11
L_{io} DQS	DQS, $\overline{DQS}$ Lpkg	-	3.3	-	3.3	nH	11,12
C_{io} DQS	DQS, $\overline{DQS}$ Cpkg	-	0.78	-	0.78	pF	11,13
DZ_{DIO} DQS	Delta Zpkg DQS, $\overline{DQS}$	-	10	-	10	Ω	1,2,5,7,10
DT_{dDIO} DQS	Delta Delay DQS, $\overline{DQS}$	-	5	-	5	ps	1,3,5,7,10
$Z_{I\ CTRL}$	Input- CTRL pins Zpkg	50	90	50	90	Ω	1,2,5,9,10,11
T_{dI_CTRL}	Input- CTRL pins Pkg Delay	14	42	14	42	ps	1,3,5,9,10,11
$L_{i\ CTRL}$	nput CTRL Lpkg	-	3.4	-	3.4	nH	11,12
$C_{i\ CTRL}$	Input CTRL Cpkg	-	0.7	-	0.7	pF	11,13
Z_{IADD} CMD	Input- CMD ADD pins Zpkg	50	90	50	90	Ω	1,2,5,8,10,11
T_{dIADD} CMD	Input- CMD ADD pins Pkg Delay	14	45	14	45	ps	1,3,5,8,10,11
L_i ADD CMD	Input CMD ADD Lpkg	-	3.6	-	3.6	nH	11,12
C_i ADD CMD	Input CMD ADD Cpkg	-	0.74	-	0.74	pF	11,13
Z_{CK}	CK, $\overline{CK}$ Zpkg	50	90	50	90	Ω	1,2,5,10,11
T_{dCK}	CK, $\overline{CK}$ Pkg Delay	14	45	14	42	ps	1,3,5,10,11
L_i CLK	Input CLK Lpkg	-	3.4	-	3.4	nH	11,12
C_i CLK	Input CLK Cpk	-	0.7	-	0.7	pF	11,13
DZ_{DCK}	Delta Zpkg CK, $\overline{CK}$	-	10	-	10	Ω	1,2,5,6,10
DT_{dCK}	Delta Delay CK, $\overline{CK}$	-	5	-	5	ps	1,3,5,6,10
Z_O ZQ	ZQ Zpkg	40	100	-	100	Ω	1,2,5,10,11
T_{dO} ZQ	ZQ Delay	20	90	20	90	ps	1,3,5,10,11
Z_O ALERT	ALERT Zpkg	40	100	40	100	Ω	1,2,5,10,11
T_{dO} ALERT	ALERT Delay	20	55	20	55	ps	1,3,5,10,11

NOTE 1 This parameter is not subject to production test. It is verified by design and characterization. The package parasitic(L & C) are validated using package only samples. The capacitance is measured with VDD, VDDQ, VSS, VSSQ shorted with all other signal pins floating. The inductance is measured with VDD, VDDQ, VSS and VSSQ shorted and all other signal pins shorted at the die side(not pin). Measurement procedure TBD.
NOTE 2 Package only impedance (Zpkg) is calculated based on the Lpkg and Cpkg total for a given pin where:

Zpkg (total per pin) = $\sqrt{Lpkg / Cpkg}$

NOTE 3 Package only delay(Tpkg) is calculated based on Lpkg and Cpkg total for a given pin where:

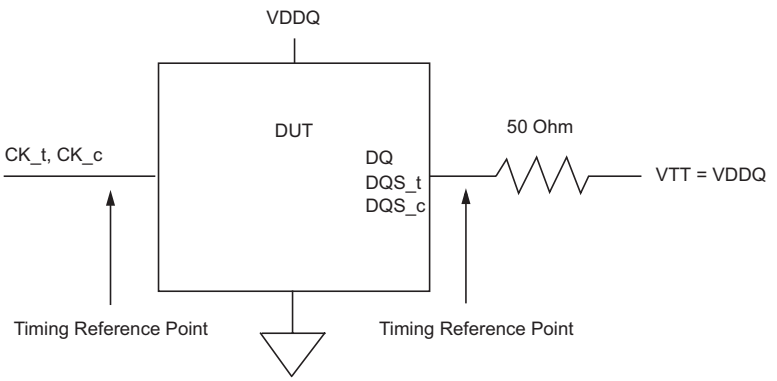
Tdpkg (total per pin) = $\sqrt{Lpkg \times Cpkg}$

NOTE 4 Z & Td IO applies to DQ, $\overline{DM}$, DQS, $\overline{DQS}$, TDQS and $\overline{TDQS}$.
NOTE 5 This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here.
NOTE 6 Absolute value of ZCK-$\overline{ZCK}$ for impedance(Z) or absolute value of TdCK-$\overline{TdCK}$ for delay(Td).
NOTE 7 Absolute value of ZIO(DQS)-ZIO($\overline{DQS}$) for impedance(Z) or absolute value of TdIO(DQS)-TdIO($\overline{DQS}$) for delay(Td).
NOTE 8 ZI & Td ADD CMD applies to A0-A13,A17, $\overline{ACT}$, BA0-BA1, BG0-BG1, $\overline{RAS}$/A16, $\overline{CAS}$/A15, $\overline{WE}$/A14 and $\overline{PAR}$.
NOTE 9 ZI & Td CTRL applies to ODT, $\overline{CS}$ and CKE.
NOTE 10 This table applies to monolithic X4 and X8 devices.
NOTE 11 Package implementations shall meet spec if the Zpkg and Pkg Delay fall within the ranges shown, and the maximum Lpkg and Cpkg do not exceed the maximum values shown.
NOTE 12 It is assumed that Lpkg can be approximated as Lpkg = Zo x Td.
NOTE 13 It is assumed that Cpkg can be approximated as Cpkg = Td / Zo.

Electrical Characteristics & AC Timing

Reference Load for AC Timing and Output Slew Rate

The effective reference load of 50 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.
It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.



tREFI

Average periodic Refresh interval (tREFI) of DDR4 SDRAM is defined as shown in the table.

tREFI by device density

Parameter	Symbol		2Gb	4Gb	8Gb	16Gb	Units
Average periodic refresh interval	tREFI	0°C ≤ Tc ≤ 85°C	7.8	7.8	7.8	TBD	μs
		85°C < Tc ≤ 95°C	3.9	3.9	3.9	TBD	μs

Timing Parameters by Speed Grade

Timing Parameters by Speed Bin for DDR4-1600 and DDR4-1866

Speed		DDR4-1600		DDR4-1866		Unit	Note
Parameter	Symbol	Min	Max	Min	Max		
Clock Timing							
Minimum Clock Cycle Time (DLL off mode)	t_{CK} (DLL-off)	8	20	8	20	ns	22
Average Clock Period	t_{CK}(avg)	1.25	<1.5	1.071	<1.25	ns	
Average high pulse width	t_{CH}(avg)	0.48	0.52	0.48	0.52	t_{CK}(avg)	
Average low pulse width	t_{CL}(avg)	0.48	0.52	0.48	0.52	t_{CK}(avg)	
Absolute Clock Period	t_{CK}(abs)	Min: tCK(avg)min+tJIT(per)min_tot Max: tCK(avg)max+ tJIT(per)max_tot				t_{CK}(avg)	
Absolute clock HIGH pulse width	t_{CH}(abs)	0.45	-	0.45	-	t_{CK}(avg)	23
Absolute clock LOW pulse width	t_{CL}(abs)	0.45	-	0.45	-	t_{CK}(avg)	24
Clock Period Jitter- total	JIT(per)_tot	-63	63	-54	54	ps	25
Clock Period Jitter- deterministic	JIT(per)_dj	-31	31	-27	27	ps	26
Clock Period Jitter during DLL locking period	t_{JIT}(per, lck)	-50	50	-43	43	ps	
Cycle to Cycle Period Jitter	t_{JIT}(cc)_total	-	125	-	107	ps	25
Cycle to Cycle Period Jitter deterministic	t_{JIT}(cc)_dj	TBD		TBD		ps	26
Cycle to Cycle Period Jitter during DLL locking period	t_{JIT}(cc, lck)	-	100	-	86	ps	
Duty Cycle Jitter	tJIT(duty)	TBD	TBD	TBD	TBD	ps	
Cumulative error across 2 cycles	t_{ERR}(2per)	-92	92	-79	79	ps	
Cumulative error across 3 cycles	t_{ERR}(2per)	-109	109	-94	94	ps	
Cumulative error across 4 cycles	t_{ERR}(2per)	-121	121	-104	104	ps	
Cumulative error across 4 cycles	t_{ERR}(2per)	-131	131	-112	112	ps	
Cumulative error across 6 cycles	t_{ERR}(2per)	-139	139	-119	119	ps	
Cumulative error across 7 cycles	t_{ERR}(2per)	-145	145	-124	124	ps	
Cumulative error across 8 cycles	t_{ERR}(2per)	-151	151	-129	129	ps	
Cumulative error across 9 cycles	t_{ERR}(2per)	-156	156	-134	134	ps	
Cumulative error across 10 cycles	t_{ERR}(2per)	-160	160	-137	137	ps	
Cumulative error across 11 cycles	t_{ERR}(2per)	-164	164	-141	141	ps	
Cumulative error across 12 cycles	t_{ERR}(2per)	-168	168	-137	137	ps	
Cumulative error across 13 cycles	t_{ERR}(2per)	-172	172	-147	147	ps	
Cumulative error across 14 cycles	t_{ERR}(2per)	-175	175	-150	150	ps	
Cumulative error across 15 cycles	t_{ERR}(2per)	-178	178	-152	152	ps	
Cumulative error across 16 cycles	t_{ERR}(2per)	-180	180	-155	155	ps	
Cumulative error across 17 cycles	t_{ERR}(2per)	-183	183	-157	157	ps	
Cumulative error across 18 cycles	t_{ERR}(2per)	-185	185	-159	159	ps	
Cumulative error across n = 13, 14 . . .49, 50 cycles	t_{ERR}(nper)	tERR(nper)min = ((1 + 0.68ln(n)) * tJIT(per)_total min) tERR(nper)max = ((1 + 0.68ln(n)) * tJIT(per)_total max)				ps	

Speed		DDR4-1600		DDR4-1866		Unit	Note
Parameter	Symbol	Min	Max	Min	Max		
Command and Address setup time to CK, $\overline{CK}$ referenced to Vih(ac) / Vil(ac) levels	t_{IS}(base)	115	-	100	-	ps	
Command and Address setup time to CK, $\overline{CK}$ referenced to Vref levels	t_{IS}(Vref)	215	-	200	-	ps	
Command and Address hold time to CK, $\overline{CK}$ referenced to Vih(dc) / Vil(dc) levels	t_{IH}(base)	140	-	125	-	ps	
Command and Address hold time to CK, $\overline{CK}$ referenced to Vref levels	t_{IH}(Vref)	215	-	200	-	ps	
Control and Address Input pulse width for each input	t_{IPW}	600	-	525	-	ps	
Command and Address Timing							
$\overline{CAS}$ to $\overline{CAS}$ command delay for same bank	t_{CCD_L}	Max(5nCK, 6.250ns)	-	Max(5nCK, 6.25ns)	-	nCK	
$\overline{CAS}$ to $\overline{CAS}$ command delay for different bank group	t_{CCD_S}	4	-	4	-	nCK	
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	$t_{RRD\_S(2K)}$	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	nCK	
ACTIVATE to ACTIVATE Command delay to different bank group for 1KB page size	$t_{RRD\_S(1K)}$	Max(4nCK, 3.7ns)	-	Max(4nCK, 3.3ns)	-	nCK	
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	$t_{RRD\_S(1/2K)}$	Max(4nCK, 3.7ns)	-	Max(4nCK, 3.3ns)	-	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	$t_{RRD\_L(2K)}$	Max(4nCK, 6.4ns)	-	Max(4nCK, 6.4ns)	-	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	$t_{RRD\_L(2K)}$	Max(4nCK, 5.3ns)	-	Max(4nCK, 4.9ns)	-	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	$t_{RRD\_L(1/2K)}$	Max(4nCK, 5.3ns)	-	Max(4nCK, 4.9ns)	-	nCK	
Four activate window for 2KB page size	t_{FAW_2K}	Max(28nCK, 35ns)	-	Max(28nCK, 30ns)	-	ns	
Four activate window for 1KB page size	t_{FAW_1K}	Max(20nCK, 25ns)	-	Max(20nCK, 23ns)	-	ns	
Four activate window for 1/2KB page size	$t_{FAW\_1/2K}$	Max(16nCK, 20ns)	-	Max(16nCK, 17ns)	-	ns	
Delay from start of internal write transaction to internal read command for different bank group	t_{WTR_S}	max(2nCK, 2.5ns)	-	max(2nCK, 2.5ns)	-		1,2,e
Delay from start of internal write transaction to internal read command for same bank group	t_{WTR_L}	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-		1
Internal READ Command to PRECHARGE Command delay	t_{RTP}	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-		
WRITE recovery time	t_{WR}	15	-	15	-	ns	1
Write recovery time when CRC and DM are enabled	$t_{WR\_CRC\_DM}$	t_{WR}+max(5nCK,3.75ns)	-	t_{WR}+max(5nCK,3.75ns)	-	ns	1,26

Speed		DDR4-1600		DDR4-1866		Unit	Note
Parameter	Symbol	Min	Max	Min	Max		
delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled	$t_{WTR\_S\_CRC\_DM}$	t_{WTR_S}+max(5nCK,3.75ns)	-	t_{WTR_S}+max(5nCK,3.75ns)	-	ns	2,29
delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	$t_{WTR\_L\_CRC\_DM}$	t_{WTR_L}+max(5nCK,3.75ns)	-	t_{WTR_L}+max(5nCK,3.75ns)	-	ns	3,30
DLL locking time	t_{DLLK}	597	-	597	-	nCK	
Mode Register Set command cycle time	t_{MRD}	8	-	8	-	nCK	
Mode Register Set command update delay	t_{MOD}	max(24nCK, 15ns)	-	max(24nCK, 15ns)	-		
Multi-Purpose Register Recovery Time	t_{MPRR}	1	-	1	-	nCK	33
Multi Purpose Register Write Recovery Time	t_{WR_MPR}	t_{MOD} (min)+ AL + PL	-	t_{MOD} (min)+ AL + PL	-		
Auto precharge write recovery + precharge time	$t_{DAL(min)}$	Programmed WR + roundup (tRP / tCK(avg))				nCK	
$\overline{CS}$ to Command Address Latency							
$\overline{CS}$ to Command Address Latency	t_{CAL}	Max(3nCK, 3.748ns)	-	Max(3nCK, 3.748ns)	-	nCK	
DRAM Data Timing							
DQS,$\overline{DQS}$ to DQ skew, per group, per access	t_{DQSQ}	-	0.16	-	0.16	t_{CK}(avg)/2	13,18
DQS,$\overline{DQS}$ to DQ Skew deterministic, per group, per access	t_{DQSQ}	-	0.16	-	0.16	t_{CK}(avg)/2	13,16,18
DQ output hold time from DQS,$\overline{DQS}$	t_{QH}	0.76	-	0.76	-	t_{CK}(avg)/2	13,17,18
DQ output hold time deterministic from DQS,$\overline{DQS}$	t_{QH}	0.76	-	0.76	-	UI	14,16,18
DQS,$\overline{DQS}$ to DQ Skew total, per group, per access; DBI enabled	t_{DQSQ}	-	0.16	-	0.16	UI	13,19
DQ output hold time total from DQS,$\overline{DQS}$; DBI enabled	t_{QH}	0.76	-	0.76	-	UI	13,19
DQ to DQ offset , per group, per access referenced to DQS,$\overline{DQS}$	t_{DQSQ}	-	0.16	-	0.16	UI	15,16
Data Strobe Timing							
DQS,$\overline{DQS}$ differential READ Preamble (2 clock preamble)	t_{RPRE}	0.9	TBD	0.9	TBD	nCK	
DQS,$\overline{DQS}$ differential READ Postamble	t_{RPST}	TBD	TBD	TBD	TBD	nCK	
DQS,$\overline{DQS}$ differential output high time	t_{QSH}	0.4	-	0.4	-	nCK	21
DQS,$\overline{DQS}$ differential output low time	t_{QSL}	0.4	-	0.4	-	nCK	20
DQS,$\overline{DQS}$ differential WRITE Preamble	t_{WPRE}	0.9	-	0.9	-	nCK	
DQS,$\overline{DQS}$ differential WRITE Postamble	t_{WPST}	TBD	TBD	TBD	TBD	nCK	
DQS and $\overline{DQS}$ low-impedance time	t_{LZ}(DQS)	-450	225	-390	195	ps	

Speed		DDR4-1600		DDR4-1866		Unit	Note
Parameter	Symbol	Min	Max	Min	Max		
DQS and $\overline{DQS}$ high-impedance time (Referenced from RL+BL/2)	t_{HZ}(DQS)	-	180	-	150	ps	
DQS,$\overline{DQS}$ differential input low pulse width	t_{DQSL}	0.46	0.54	0.46	0.54	nCK	
DQS,$\overline{DQS}$ differential input high pulse width	t_{DQSH}	0.46	0.54	0.46	0.54	nCK	
DQS,$\overline{DQS}$ rising edge to CK,$\overline{CK}$ rising edge (1 clock preamble)	t_{DQSS}	-0.27	0.27	-0.27	0.27	nCK	
DQS,$\overline{DQS}$ falling edge setup time to CK,$\overline{CK}$	t_{DSS}	0.18	-	0.18	-	nCK	
DQS,$\overline{DQS}$ falling edge hold time from CK,$\overline{CK}$	t_{DSH}	0.18	-	0.18	-	nCK	
MPSM Timing							
Command path disable delay upon MPSM entry	t_{MPED}	Min: t_{MOD}(min) +t_{CPDED}(min)					
Valid clock requirement after MPSM entry	t_{CKMPE}	Min: t_{MOD}(min) +t_{CPDED}(min)					
Valid clock requirement before MPSM exit	t_{CKMPX}	Min: t_{CKSRX}(min)					
Exit MPSM to commands not requiring a locked DLL	t_{XMP}	TBD	-	TBD	-		
Exit MPSM to commands requiring a locked DLL	t_{XMPDLL}	Min: t_{XMP}(min) + t_{XSDLL}(min)					
CS setup time to CKE	t_{MPX_S}	TBD	-	TBD	-		
CS hold time to CKE	t_{MPX_H}	TBD	-	TBD	-		
Calibration Timing							
Power-up and RESET calibration time	t_{ZQinit}	1024	-	1024	-	nCK	
Normal operation Full calibration time	t_{ZQoper}	512	-	512	-	nCK	
Normal operation Short calibration time	t_{ZQCS}	128	-	128	-	nCK	
Reset/Self Refresh Timing							
Exit Reset from CKE HIGH to a valid command	t_{XPR}	Max: max(5nCK,t_{RFC}(min)+10ns)					
Exit Self Refresh to commands not requiring a locked DLL	t_{XS}	Min: t_{RFC}(min)+10ns					
SRX to commands not requiring a locked DLL in Self Refresh ABORT	$t_{XS\_ABORT(min)}$	Min: t_{RFC4}(min)+10ns					
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	$t_{XS\_FAST(min)}$	Min: t_{RFC4}(min)+10ns					
Exit Self Refresh to commands requiring a locked DLL	t_{XSDLL}	Min: t_{DLLK}(min)					
Minimum CKE low width for Self refresh entry to exit timing	t_{CKESR}	Min: t_{CKE}(min)+1nCK					
Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled	t_{CKESR_PAR}	Min: t_{CKE}(min)+1nCK+PL					
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	t_{CKSRE}	Min: max(5nCK,10ns)					

Speed		DDR4-1600		DDR4-1866		Unit	Note
Parameter	Symbol	Min	Max	Min	Max		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	t_{CKSRE_PAR}	Min: max(5nCK,10ns)+PL					
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	t_{CKSRX}	Min: max(5nCK,10ns)					
Power Down Timing							
Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	t_{XP}	Min: max(4nCK,6ns)					
CKE minimum pulse width	t_{CKE}	Min: max (3nCK,5ns)					31,32
Command pass disable delay	t_{CPDED}	4	-	4	-	nCK	
Power Down Entry to Exit Timing	t_{PD}	t_{CKE}(min)	$9xt_{REFI}$	t_{CKE}(min)	$9xt_{REFI}$		6
Timing of ACT command to Power Down entry	$t_{ACTPDEN}$	1	-	1	-	nCK	7
Timing of PRE or PREA command to Power Down entry	t_{PRPDEN}	1	-	1	-	nCK	7
Timing of RD/RDA command to Power Down entry	t_{RDPDEN}	RL+4+1	-	RL+4+1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	t_{WRPDEN}	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	$t_{WRAPDEN}$	WL+4+WR+1	-	WL+4+WR+1	-	nCK	5
Timing of WR command to Power Down entry (BC4MRS)	$t_{WRPBC4DEN}$	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	$t_{WRAPBC4DEN}$	WL+2+WR+1	-	WL+2+WR+1	-	nCK	5
Timing of REF command to Power Down entry	$t_{REFPDEN}$	1	-	1	-	nCK	7
Timing of MRS command to Power Down entry	$t_{MRSPDEN}$	t_{MOD}(min)	-	t_{MOD}(min)	-	ps	
PDA Timing							
Mode Register Set command cycle time in PDA mode	t_{MRD_PDA}	max(16nCK, 10ns)		max(16nCK, 10ns)			
Mode Register Set command update delay in PDA mode	t_{MOD_PDA}	t_{MOD}					
ODT Timing							
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	t_{AONAS}	1.0	9.0	1.0	9.0	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	t_{AOFAS}	1.0	9.0	1.0	9.0	ns	
RTT dynamic change skew	t_{ADC}	0.3	0.7	0.3	0.7	t_{CK}(avg)	
Write Leveling Timing							

Speed		DDR4-1600		DDR4-1866			
Parameter	Symbol	Min	Max	Min	Max	Unit	Note
First DQS/$\overline{DQS}$ rising edge after write leveling mode is programmed	t_{WLMRD}	40	-	40	-	nCK	
DQS/$\overline{DQS}$ delay after write leveling mode is programmed	$t_{WLDQSEN}$	25	-	25	-	nCK	
Write leveling setup time from rising CK/$\overline{CK}$ crossing to rising DQS/$\overline{DQS}$ crossing	t_{WLS}	0.13	-	0.13	-	t_{CK}(avg)	
Write leveling hold time from rising CK/$\overline{CK}$ crossing to rising DQS/$\overline{DQS}$ crossing	t_{WLH}	0.13	-	0.13	-	t_{CK}(avg)	
Write leveling output delay	t_{WLO}	0	9.5	0	9.5	ns	
Write leveling output error	t_{WLOE}	0	2	0	2	ns	
CA Parity Timing							
Commands not guaranteed to be executed during this time	$t_{PAR\_UNKNOWN}$	-	PL	-	PL		
Delay from errant command to $\overline{ALERT}$ assertion	$t_{PAR\_ALERT\_ON}$	-	PL+6ns	-	PL+6ns		
Pulse width of $\overline{ALERT}$ signal when asserted	$t_{PAR\_ALERT\_PW}$	48	96	56	112	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	$t_{PAR\_ALERT\_RSP}$	-	43	-	50	nCK	
Parity Latency	PL	4		4		nCK	
CRC Error Timing							
CRC error to $\overline{ALERT}$ latency	t_{CRC_ALERT}	3	13	3	13	ns	
CRC $\overline{ALERT}$ pulse width	CRC_ALERT_PW	6	10	6	10	nCK	
Geardown timing							
Exit RESET from CKE HIGH to a valid MRS geardown (T2/Reset)	t_{XPR_GEAR}	-		-			
CKE High Assert to Gear Down Enable time(T2/CKE)	t_{XS_GEAR}	-		-			
MRS command to Sync pulse time(T3)	t_{SYNC_GEAR}	-	-	-	-		27
Sync pulse to First valid command(T4)	t_{CMD_GEAR}	-		-			27
Geardown setup time	t_{GEAR_setup}	-	-	-	-	nCK	
Geardown hold time	t_{GEAR_hold}	-	-	-	-	nCK	
t_{REFI}							
t_{RFC1} (min)	2Gb	160	-	160	-	ns	
	4Gb	260	-	260	-	ns	
	8Gb	350	-	350	-	ns	
	16Gb	TBD	-	TBD	-	ns	

Speed		DDR4-1600		DDR4-1866			
Parameter	Symbol	Min	Max	Min	Max	Unit	Note
t_{RFC2} (min)	2Gb	110	-	110	-	ns	
	4Gb	160	-	160	-	ns	
	8Gb	260	-	260	-	ns	
	16Gb	TBD	-	TBD	-	ns	
t_{RFC4} (min)	2Gb	90	-	90	-	ns	
	4Gb	110	-	110	-	ns	
	8Gb	160	-	160	-	ns	
	16Gb	TBD	-	TBD	-	ns	

Timing Parameters by Speed Bin for DDR4-2133 and DDR4-2400

Speed		DDR4-2133		DDR4-2400		Unit	Note
Parameter	Symbol	Min	Max	Min	Max		
Clock Timing							
Minimum Clock Cycle Time (DLL off mode)	t_{CK} (DLL-off)	8	20	8	20	ns	22
Average Clock Period	t_{CK}(avg)	0.938	<1.071	0.833	<0.938	ns	
Average high pulse width	t_{CH}(avg)	0.48	0.52	0.48	0.52	t_{CK}(avg)	
Average low pulse width	t_{CL}(avg)	0.48	0.52	0.48	0.52	t_{CK}(avg)	
Absolute Clock Period	t_{CK}(abs)	Min: tCK(avg)min+tJIT(per)min_tot Max: tCK(avg)max+ tJIT(per)max_tot				t_{CK}(avg)	
Absolute clock HIGH pulse width	t_{CH}(abs)	0.45	-	0.45	-	t_{CK}(avg)	23
Absolute clock LOW pulse width	t_{CL}(abs)	0.45	-	0.45	-	t_{CK}(avg)	24
Clock Period Jitter- total	JIT(per)_tot	-47	47	-42	42	ps	25
Clock Period Jitter- deterministic	JIT(per)_dj	-23	23	-21	21	ps	26
Clock Period Jitter during DLL locking period	t_{JIT}(per, lck)	-38	38	-33	33	ps	
Cycle to Cycle Period Jitter	t_{JIT}(cc)_total	-	94	-	83	ps	25
Cycle to Cycle Period Jitter deterministic	t_{JIT}(cc)_dj	TBD		TBD		ps	26
Cycle to Cycle Period Jitter during DLL locking period	t_{JIT}(cc, lck)	-	75	-	67	ps	
Duty Cycle Jitter	tJIT(duty)	TBD	TBD	TBD	TBD	ps	
Cumulative error across 2 cycles	t_{ERR}(2per)	-69	69	-61	61	ps	
Cumulative error across 3 cycles	t_{ERR}(2per)	-82	82	-73	73	ps	
Cumulative error across 4 cycles	t_{ERR}(2per)	-91	91	-81	81	ps	
Cumulative error across 4 cycles	t_{ERR}(2per)	-98	98	-87	87	ps	
Cumulative error across 6 cycles	t_{ERR}(2per)	-104	104	-92	92	ps	
Cumulative error across 7 cycles	t_{ERR}(2per)	-109	109	-97	97	ps	
Cumulative error across 8 cycles	t_{ERR}(2per)	-113	113	-101	101	ps	
Cumulative error across 9 cycles	t_{ERR}(2per)	-117	117	-104	104	ps	
Cumulative error across 10 cycles	t_{ERR}(2per)	-120	120	-107	107	ps	
Cumulative error across 11 cycles	t_{ERR}(2per)	-123	123	-110	110	ps	
Cumulative error across 12 cycles	t_{ERR}(2per)	-126	126	-112	112	ps	
Cumulative error across 13 cycles	t_{ERR}(2per)	-129	129	-114	114	ps	
Cumulative error across 14 cycles	t_{ERR}(2per)	-131	131	-116	116	ps	
Cumulative error across 15 cycles	t_{ERR}(2per)	-133	133	-118	118	ps	
Cumulative error across 16 cycles	t_{ERR}(2per)	-135	135	-120	120	ps	
Cumulative error across 17 cycles	t_{ERR}(2per)	-137	137	-122	122	ps	
Cumulative error across 18 cycles	t_{ERR}(2per)	-139	139	-124	124	ps	
Cumulative error across n = 13, 14 . . .49, 50 cycles	t_{ERR}(nper)	tERR(nper)min = ((1 + 0.68ln(n)) * tJIT(per)_total min) tERR(nper)max = ((1 + 0.68ln(n)) * tJIT(per)_total max)				ps	
Command and Address setup time to CK, $\overline{CK}$ referenced to Vih(ac) / Vil(ac) levels	t_{IS}(base)	80	-	62	-	ps	

Speed		DDR4-2133		DDR4-2400			
Parameter	Symbol	Min	Max	Min	Max	Unit	Note
Command and Address setup time to CK, $\overline{CK}$ referenced to Vref levels	t_{IS}(Vref)	180	-	162	-	ps	
Command and Address hold time to CK, $\overline{CK}$ referenced to Vih(dc) / Vil(dc) levels	t_{IH}(base)	105	-	87	-	ps	
Command and Address hold time to CK, $\overline{CK}$ referenced to Vref levels	t_{IH}(Vref)	180	-	162	-	ps	
Control and Address Input pulse width for each input	t_{IPW}	460	-	410	-	ps	
Command and Address Timing							
$\overline{CAS}$ to $\overline{CAS}$ command delay for same bank	t_{CCD_L}	Max(5nCK, 5.625ns)	-	Max(5nCK, 5ns)	-	nCK	
$\overline{CAS}$ to $\overline{CAS}$ command delay for different bank group	t_{CCD_S}	4	-	4	-	nCK	
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	$t_{RRD\_S(2K)}$	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	nCK	
ACTIVATE to ACTIVATE Command delay to different bank group for 1KB page size	$t_{RRD\_S(1K)}$	Max(4nCK, 3.7ns)	-	Max(4nCK, 3.3ns)	-	nCK	
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	$t_{RRD\_S(1/2K)}$	Max(4nCK, 3.7ns)	-	Max(4nCK, 3.3ns)	-	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	$t_{RRD\_L(2K)}$	Max(4nCK, 6.4ns)	-	Max(4nCK, 6.4ns)	-	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	$t_{RRD\_L(2K)}$	Max(4nCK, 5.3ns)	-	Max(4nCK, 4.9ns)	-	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	$t_{RRD\_L(1/2K)}$	Max(4nCK, 5.3ns)	-	Max(4nCK, 4.9ns)	-	nCK	
Four activate window for 2KB page size	t_{FAW_2K}	Max(28nCK, 30ns)	-	Max(28nCK, 30ns)	-	ns	
Four activate window for 1KB page size	t_{FAW_1K}	Max(20nCK, 21ns)	-	Max(20nCK, 21ns)	-	ns	
Four activate window for 1/2KB page size	$t_{FAW\_1/2K}$	Max(16nCK, 15ns)	-	Max(16nCK, 13ns)	-	ns	
Delay from start of internal write transaction to internal read command for different bank group	t_{WTR_S}	max(2nCK, 2.5ns)	-	max(2nCK, 2.5ns)	-		1,2,e
Delay from start of internal write transaction to internal read command for same bank group	t_{WTR_L}	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-		1
Internal READ Command to PRECHARGE Command delay	t_{RTP}	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-		
WRITE recovery time	t_{WR}	15	-	15	-	ns	1
Write recovery time when CRC and DM are enabled	$t_{WR\_CRC\_DM}$	t_{WR}+max(5nCK,3.75ns)	-	t_{WR}+max(5nCK,3.75ns)	-	ns	1,26

Speed		DDR4-2133		DDR4-2400		Unit	Note
Parameter	Symbol	Min	Max	Min	Max		
delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled	$t_{WTR\_S\_CRC\_DM}$	t_{WTR_S}+max(5nCK,3.75ns)	-	t_{WTR_S}+max(5nCK,3.75ns)	-	ns	2,29
delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	$t_{WTR\_L\_CRC\_DM}$	t_{WTR_L}+max(5nCK,3.75ns)	-	t_{WTR_L}+max(5nCK,3.75ns)	-	ns	3,30
DLL locking time	t_{DLLK}	768	-	768	-	nCK	
Mode Register Set command cycle time	t_{MRD}	8	-	8	-	nCK	
Mode Register Set command update delay	t_{MOD}	max(24nCK, 15ns)	-	max(24nCK, 15ns)	-		
Multi-Purpose Register Recovery Time	t_{MPRR}	1	-	1	-	nCK	33
Multi Purpose Register Write Recovery Time	t_{WR_MPR}	t_{MOD} (min)+ AL + PL	-	t_{MOD} (min)+ AL + PL	-		
Auto precharge write recovery + precharge time	$t_{DAL(min)}$	Programmed WR + roundup (tRP / tCK(avg))				nCK	
$\overline{CS}$ to Command Address Latency							
$\overline{CS}$ to Command Address Latency	t_{CAL}	Max(3nCK, 3.748ns)	-	Max(3nCK, 3.748ns)	-	nCK	
DRAM Data Timing							
DQS,$\overline{DQS}$ to DQ skew, per group, per access	t_{DQSQ}	-	TBD	-	TBD	t_{CK}(avg)/2	13,18
DQS,$\overline{DQS}$ to DQ Skew deterministic, per group, per access	t_{DQSQ}	-	TBD	-	TBD	t_{CK}(avg)/2	13,16,18
DQ output hold time from DQS,$\overline{DQS}$	t_{QH}	TBD	-	TBD	-	t_{CK}(avg)/2	13,17,18
DQ output hold time deterministic from DQS,$\overline{DQS}$	t_{QH}	TBD	-	TBD	-	UI	14,16,18
DQS,$\overline{DQS}$ to DQ Skew total, per group, per access; DBI enabled	t_{DQSQ}	-	TBD	-	TBD	UI	13,19
DQ output hold time total from DQS,$\overline{DQS}$; DBI enabled	t_{QH}	TBD	-	TBD	-	UI	13,19
DQ to DQ offset , per group, per access referenced to DQS,$\overline{DQS}$	t_{DQSQ}	TBD	TBD	TBD	TBD	UI	15,16
Data Strobe Timing							
DQS,$\overline{DQS}$ differential READ Preamble (2 clock preamble)	t_{RPRE}	0.9	TBD	0.9	TBD	nCK	
DQS,$\overline{DQS}$ differential READ Postamble	t_{RPST}	TBD	TBD	TBD	TBD	nCK	
DQS,$\overline{DQS}$ differential output high time	t_{QSH}	0.4	-	0.4	-	nCK	21
DQS,$\overline{DQS}$ differential output low time	t_{QSL}	0.4	-	0.4	-	nCK	20
DQS,$\overline{DQS}$ differential WRITE Preamble	t_{WPRE}	0.9	-	0.9	-	nCK	
DQS,$\overline{DQS}$ differential WRITE Postamble	t_{WPST}	TBD	TBD	TBD	TBD	nCK	
DQS and $\overline{DQS}$ low-impedance time	t_{LZ}(DQS)	-360	180	-300	150	ps	

Speed		DDR4-2133		DDR4-2400			
Parameter	Symbol	Min	Max	Min	Max	Unit	Note
DQS and $\overline{DQS}$ high-impedance time (Referenced from RL+BL/2)	t_{HZ}(DQS)	-	180	-	150	ps	
DQS,$\overline{DQS}$ differential input low pulse width	t_{DQSL}	0.46	0.54	0.46	0.54	nCK	
DQS,$\overline{DQS}$ differential input high pulse width	t_{DQSH}	0.46	0.54	0.46	0.54	nCK	
DQS,$\overline{DQS}$ rising edge to CK,$\overline{CK}$ rising edge (1 clock preamble)	t_{DQSS}	-0.27	0.27	-0.27	0.27	nCK	
DQS,$\overline{DQS}$ falling edge setup time to CK,$\overline{CK}$	t_{DSS}	0.18	-	0.18	-	nCK	
DQS,$\overline{DQS}$ falling edge hold time from CK,$\overline{CK}$	t_{DSH}	0.18	-	0.18	-	nCK	
MPSM Timing							
Command path disable delay upon MPSM entry	t_{MPED}	Min: t_{MOD}(min) +t_{CPDED}(min)					
Valid clock requirement after MPSM entry	t_{CKMPE}	Min: t_{MOD}(min) +t_{CPDED}(min)					
Valid clock requirement before MPSM exit	t_{CKMPX}	Min: t_{CKSRX}(min)					
Exit MPSM to commands not requiring a locked DLL	t_{XMP}	TBD	-	TBD	-		
Exit MPSM to commands requiring a locked DLL	t_{XMPDLL}	Min: t_{XMP}(min) + t_{XSDLL}(min)					
CS setup time to CKE	t_{MPX_S}	TBD	-	TBD	-		
CS hold time to CKE	t_{MPX_H}	TBD	-	TBD	-		
Calibration Timing							
Power-up and RESET calibration time	t_{ZQinit}	1024	-	1024	-	nCK	
Normal operation Full calibration time	t_{ZQoper}	512	-	512	-	nCK	
Normal operation Short calibration time	t_{ZQCS}	128	-	128	-	nCK	
Reset/Self Refresh Timing							
Exit Reset from CKE HIGH to a valid command	t_{XPR}	Max: max(5nCK,t_{RFC}(min)+10ns)					
Exit Self Refresh to commands not requiring a locked DLL	t_{XS}	Min: t_{RFC}(min)+10ns					
SRX to commands not requiring a locked DLL in Self Refresh ABORT	$t_{XS\_ABORT(min)}$	Min: t_{RFC4}(min)+10ns					
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	$t_{XS\_FAST(min)}$	Min: t_{RFC4}(min)+10ns					
Exit Self Refresh to commands requiring a locked DLL	t_{XSDLL}	Min: t_{DLLK}(min)					
Minimum CKE low width for Self refresh entry to exit timing	t_{CKESR}	Min: t_{CKE}(min)+1nCK					
Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled	t_{CKESR_PAR}	Min: t_{CKE}(min)+1nCK+PL					
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	t_{CKSRE}	Min: max(5nCK,10ns)					

Speed		DDR4-2133		DDR4-2400		Unit	Note
Parameter	Symbol	Min	Max	Min	Max		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	t_{CKSRE_PAR}	Min: max(5nCK,10ns)+PL					
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	t_{CKSRX}	Min: max(5nCK,10ns)					
Power Down Timing							
Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	t_{XP}	Min: max(4nCK,6ns)					
CKE minimum pulse width	t_{CKE}	Min: max (3nCK,5ns)					31,32
Command pass disable delay	t_{CPDED}	4	-	4	-	nCK	
Power Down Entry to Exit Timing	t_{PD}	t_{CKE}(min)	9xt_{REFI}	t_{CKE}(min)	9xt_{REFI}		6
Timing of ACT command to Power Down entry	$t_{ACTPDEN}$	2	-	2	-	nCK	7
Timing of PRE or PREA command to Power Down entry	t_{PRPDEN}	2	-	2	-	nCK	7
Timing of RD/RDA command to Power Down entry	t_{RDPDEN}	RL+4+1	-	RL+4+1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	t_{WRPDEN}	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	$t_{WRAPDEN}$	WL+4+WR+1	-	WL+4+WR+1	-	nCK	5
Timing of WR command to Power Down entry (BC4MRS)	$t_{WRPBC4DEN}$	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	$t_{WRAPBC4DEN}$	WL+2+WR+1	-	WL+2+WR+1	-	nCK	5
Timing of REF command to Power Down entry	$t_{REFPDEN}$	2	-	1	-	nCK	7
Timing of MRS command to Power Down entry	$t_{MRSPDEN}$	t_{MOD}(min)	-	t_{MOD}(min)	-	ps	
PDA Timing							
Mode Register Set command cycle time in PDA mode	t_{MRD_PDA}	max(16nCK, 10ns)		max(16nCK, 10ns)			
Mode Register Set command update delay in PDA mode	t_{MOD_PDA}	t_{MOD}					
ODT Timing							
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	t_{AONAS}	1.0	9.0	1.0	9.0	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	t_{AOFAS}	1.0	9.0	1.0	9.0	ns	
RTT dynamic change skew	t_{ADC}	0.3	0.7	0.3	0.7	t_{CK}(avg)	
Write Leveling Timing							

Speed		DDR4-2133		DDR4-2400			
Parameter	Symbol	Min	Max	Min	Max	Unit	Note
First DQS/$\overline{DQS}$ rising edge after write leveling mode is programmed	t_{WLMRD}	40	-	40	-	nCK	
DQS/$\overline{DQS}$ delay after write leveling mode is programmed	$t_{WLDQSEN}$	25	-	25	-	nCK	
Write leveling setup time from rising CK/$\overline{CK}$ crossing to rising DQS/$\overline{DQS}$ crossing	t_{WLS}	0.13	-	0.13	-	t_{CK}(avg)	
Write leveling hold time from rising CK/$\overline{CK}$ crossing to rising DQS/$\overline{DQS}$ crossing	t_{WLH}	0.13	-	0.13	-	t_{CK}(avg)	
Write leveling output delay	t_{WLO}	0	9.5	0	9.5	ns	
Write leveling output error	t_{WLOE}	0	2	0	2	ns	
CA Parity Timing							
Commands not guaranteed to be executed during this time	$t_{PAR\_UNKNOWN}$	-	PL	-	PL		
Delay from errant command to $\overline{ALERT}$ assertion	$t_{PAR\_ALERT\_ON}$	-	PL+6ns	-	PL+6ns		
Pulse width of $\overline{ALERT}$ signal when asserted	$t_{PAR\_ALERT\_PW}$	64	128	72	114	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	$t_{PAR\_ALERT\_RSP}$	-	57	-	64	nCK	
Parity Latency	PL	4		5		nCK	
CRC Error Timing							
CRC error to $\overline{ALERT}$ latency	t_{CRC_ALERT}	3	13	3	13	ns	
CRC $\overline{ALERT}$ pulse width	CRC_ALERT_PW	6	10	6	10	nCK	
Geardown timing							
Exit RESET from CKE HIGH to a valid MRS geardown (T2/Reset)	t_{XPR_GEAR}	-		-			
CKE High Assert to Gear Down Enable time(T2/CKE)	t_{XS_GEAR}	-		-			
MRS command to Sync pulse time(T3)	t_{SYNC_GEAR}	-	-	-	-		27
Sync pulse to First valid command(T4)	t_{CMD_GEAR}	-		-			27
Geardown setup time	t_{GEAR_setup}	-	-	-	-	nCK	
Geardown hold time	t_{GEAR_hold}	-	-	-	-	nCK	
t_{REFI}							
t_{RFC1} (min)	2Gb	160	-	160	-	ns	
	4Gb	260	-	260	-	ns	
	8Gb	350	-	350	-	ns	
	16Gb	TBD	-	TBD	-	ns	

Speed		DDR4-2133		DDR4-2400			
Parameter	Symbol	Min	Max	Min	Max	Unit	Note
t_{RFC2} (min)	2Gb	110	-	110	-	ns	
	4Gb	160	-	160	-	ns	
	8Gb	260	-	260	-	ns	
	16Gb	TBD	-	TBD	-	ns	
t_{RFC4} (min)	2Gb	90	-	90	-	ns	
	4Gb	110	-	110	-	ns	
	8Gb	160	-	160	-	ns	
	16Gb	TBD	-	TBD	-	ns	

Timing Parameters by Speed Bin for DDR4-2666 and DDR4-3200

Speed		DDR4-2666		DDR4-3200			
Parameter	Symbol	Min	Max	Min	Max	Unit	Note
Clock Timing							
Minimum Clock Cycle Time (DLL off mode)	t_{CK} (DLL-off)	8	20	8	-	ns	22
Average Clock Period	t_{CK}(avg)	0.750	<0.833	0.625	<0.750	ns	
Average high pulse width	t_{CH}(avg)	0.48	0.52	0.48	0.52	t_{CK}(avg)	
Average low pulse width	t_{CL}(avg)	0.48	0.52	0.48	0.52	t_{CK}(avg)	
Absolute Clock Period	t_{CK}(abs)	Min: tCK(avg)min+tJIT(per)min_tot Max: tCK(avg)max+ tJIT(per)max_tot				t_{CK}(avg)	
Absolute clock HIGH pulse width	t_{CH}(abs)	0.45	-	0.45	-	t_{CK}(avg)	23
Absolute clock LOW pulse width	t_{CL}(abs)	0.45	-	0.45	-	t_{CK}(avg)	24
Clock Period Jitter- total	JIT(per)_tot	-38	38	-0.1	0.1	ps	25
Clock Period Jitter- deterministic	JIT(per)_dj	-19	19	TBD	TBD	ps	26
Clock Period Jitter during DLL locking period	t_{JIT}(per, lck)	-30	30	TBD	TBD	ps	
Cycle to Cycle Period Jitter	t_{JIT}(cc)_total	-	75	-	TBD	ps	25
Cycle to Cycle Period Jitter deterministic	t_{JIT}(cc)_dj	TBD		TBD		ps	26
Cycle to Cycle Period Jitter during DLL locking period	t_{JIT}(cc, lck)	-	60	-	TBD	ps	
Duty Cycle Jitter	tJIT(duty)	TBD	TBD	TBD	TBD	ps	
Cumulative error across 2 cycles	t_{ERR}(2per)	-55	55	TBD	TBD	ps	
Cumulative error across 3 cycles	t_{ERR}(2per)	-66	66	TBD	TBD	ps	
Cumulative error across 4 cycles	t_{ERR}(2per)	-73	73	TBD	TBD	ps	
Cumulative error across 5 cycles	t_{ERR}(2per)	-78	78	TBD	TBD	ps	
Cumulative error across 6 cycles	t_{ERR}(2per)	-83	83	TBD	TBD	ps	
Cumulative error across 7 cycles	t_{ERR}(2per)	-87	87	TBD	TBD	ps	
Cumulative error across 8 cycles	t_{ERR}(2per)	-91	91	TBD	TBD	ps	
Cumulative error across 9 cycles	t_{ERR}(2per)	-94	94	TBD	TBD	ps	
Cumulative error across 10 cycles	t_{ERR}(2per)	-96	96	TBD	TBD	ps	
Cumulative error across 11 cycles	t_{ERR}(2per)	-99	99	TBD	TBD	ps	
Cumulative error across 12 cycles	t_{ERR}(2per)	-101	101	TBD	TBD	ps	
Cumulative error across 13 cycles	t_{ERR}(2per)	-103	103	TBD	TBD	ps	
Cumulative error across 14 cycles	t_{ERR}(2per)	-104	104	TBD	TBD	ps	
Cumulative error across 15 cycles	t_{ERR}(2per)	-106	106	TBD	TBD	ps	
Cumulative error across 16 cycles	t_{ERR}(2per)	-108	108	TBD	TBD	ps	
Cumulative error across 17 cycles	t_{ERR}(2per)	-110	110	TBD	TBD	ps	
Cumulative error across 18 cycles	t_{ERR}(2per)	-112	112	TBD	TBD	ps	

Speed		DDR4-2666		DDR4-3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max		
Cumulative error across n = 13, 14 . . .49, 50 cycles	t_{ERR}(nper)	tERR(nper)min = ((1 + 0.68ln(n)) * tJIT(per)_total min) tERR(nper)max = ((1 + 0.68ln(n)) * tJIT(per)_total max)				ps	
Command and Address setup time to CK, $\overline{CK}$ referenced to Vih(ac) / Vil(ac) levels	t_{IS}(base)	55	-	TBD	-	ps	
Command and Address setup time to CK, $\overline{CK}$ referenced to Vref levels	t_{IS}(Vref)	145	-	TBD	-	ps	
Command and Address hold time to CK, $\overline{CK}$ referenced to Vih(dc) / Vil(dc) levels	t_{IH}(base)	80	-	TBD	-	ps	
Command and Address hold time to CK, $\overline{CK}$ referenced to Vref levels	t_{IH}(Vref)	145	-	TBD	-	ps	
Control and Address Input pulse width for each input	t_{IPW}	385	-	TBD	-	ps	
Command and Address Timing							
$\overline{CAS}$ to $\overline{CAS}$ command delay for same bank	t_{CCD_L}	max(5 nCK,5ns)	-	TBD	-	nCK	
$\overline{CAS}$ to $\overline{CAS}$ command delay for different bank group	t_{CCD_S}	4	-	TBD	-	nCK	
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	$t_{RRD\_S(2K)}$	Max(4nCK,5.3ns)	-	TBD	-	nCK	
ACTIVATE to ACTIVATE Command delay to different bank group for 1KB page size	$t_{RRD\_S(1K)}$	Max(4nCK,3ns)	-	TBD	-	nCK	
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	$t_{RRD\_S(1/2K)}$	Max(4nCK,3ns)	-	TBD	-	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	$t_{RRD\_L(2K)}$	Max(4nCK,6.4ns)	-	TBD	-	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	$t_{RRD\_L(1K)}$	Max(4nCK,4.9ns)	-	TBD	-	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	$t_{RRD\_L(1/2K)}$	Max(4nCK,4.9ns)	-	TBD	-	nCK	
Four activate window for 2KB page size	t_{FAW_2K}	Max(28nCK,30ns)	-	TBD	-	ns	
Four activate window for 1KB page size	t_{FAW_1K}	Max(20nCK,21ns)	-	TBD	-	ns	
Four activate window for 1/2KB page size	$t_{FAW\_1/2K}$	Max(16nCK,12ns)	-	TBD	-	ns	
Delay from start of internal write transaction to internal read command for different bank group	t_{WTR_S}	Max(2nCK,2.5ns)	-	TBD	-		1,2,e
Delay from start of internal write transaction to internal read command for same bank group	t_{WTR_L}	Max(4nCK,7.5ns)	-	TBD	-		1
Internal READ Command to PRECHARGE Command delay	t_{RTP}	Max(4nCK,7.5ns)	-	TBD	-		
WRITE recovery time	t_{WR}	15	-	TBD	-	ns	1

Speed		DDR4-2666		DDR4-3200			
Parameter	Symbol	Min	Max	Min	Max	Unit	Note
Write recovery time when CRC and DM are enabled	$t_{WR\_CRC\_DM}$	tWR+Max(5nCK,3.75ns)	-	TBD	-	ns	1,26
delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled	$t_{WTR\_S\_CRC\_DM}$	tWTR_S+max(5nCK,3.75ns)	-	TBD	-	ns	2,29
delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	$t_{WTR\_L\_CRC\_DM}$	tWTR_L+max(5nCK,3.75ns)	-	TBD	-	ns	3,30
DLL locking time	t_{DLLK}	1024	-	TBD	-	nCK	
Mode Register Set command cycle time	t_{MRD}	8	-	TBD	-	nCK	
Mode Register Set command update delay	t_{MOD}	Max(24nCK,15ns)	-	TBD	-		
Multi-Purpose Register Recovery Time	t_{MPRR}	1	-	TBD	-	nCK	33
Multi Purpose Register Write Recovery Time	t_{WR_MPR}	tMOD(min)+AL+PL	-	TBD	-		
Auto precharge write recovery + precharge time	$t_{DAL(min)}$	Programmed WR + roundup (tRP / tCK(avg))				nCK	
$\overline{CS}$ to Command Address Latency							
$\overline{CS}$ to Command Address Latency	t_{CAL}	Max(3nCK,3.748ns)	-	TBD	-	nCK	
DRAM Data Timing							
DQS,$\overline{DQS}$ to DQ skew, per group, per access	t_{DQSQ}	-	0.18	-	TBD	t_{CK}(avg)/2	13,18
DQ output hold time from DQS,$\overline{DQS}$	t_{QH}	0.74	-	TBD	-	t_{CK}(avg)/2	13,17,18
DQ output hold time deterministic from DQS,$\overline{DQS}$	t_{QH}	TBD	-	TBD	-	UI	14,16,18
DQS,$\overline{DQS}$ to DQ Skew total, per group, per access; DBI enabled	t_{DQSQ}	-	TBD	-	TBD	UI	13,19
DQ output hold time total from DQS,$\overline{DQS}$; DBI enabled	t_{QH}	TBD	-	TBD	-	UI	13,19
DQ to DQ offset , per group, per access referenced to DQS,$\overline{DQS}$	t_{DQSQ}	TBD	TBD	TBD	TBD	UI	15,16
Data Strobe Timing							
DQS,$\overline{DQS}$ differential READ Preamble (1 clock preamble)	t_{RPRE}	0.9	TBD	TBD	TBD	nCK	
DQS,$\overline{DQS}$ differential READ Postamble	t_{RPST}	10.33	TBD	TBD	TBD	nCK	
DQS,$\overline{DQS}$ differential output high time	t_{QSH}	0.4	TBD	TBD	TBD	nCK	21
DQS,$\overline{DQS}$ differential output low time	t_{QSL}	0.4	TBD	TBD	TBD	nCK	20
DQS,$\overline{DQS}$ differential WRITE Preamble	t_{WPRE}	0.9	TBD	TBD	TBD	nCK	
DQS,$\overline{DQS}$ differential WRITE Postamble	t_{WPST}	0.33	TBD	TBD	TBD	nCK	
DQS and $\overline{DQS}$ low-impedance time	t_{LZ}(DQS)	-310	170	TBD	TBD	ps	

Speed		DDR4-2666		DDR4-3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max		
DQS and $\overline{DQS}$ high-impedance time (Referenced from RL+BL/2)	t_{HZ}(DQS)	-	170	TBD	TBD	ps	
DQS,$\overline{DQS}$ differential input low pulse width	t_{DQSL}	0.46	0.54	TBD	TBD	nCK	
DQS,$\overline{DQS}$ differential input high pulse width	t_{DQSH}	0.46	0.54	TBD	TBD	nCK	
DQS,$\overline{DQS}$ rising edge to CK,$\overline{CK}$ rising edge (1 clock preamble)	t_{DQSS}	-0.27	0.27	TBD	TBD	nCK	
DQS,$\overline{DQS}$ falling edge setup time to CK,$\overline{CK}$	t_{DSS}	0.18	-	TBD	TBD	nCK	
DQS,$\overline{DQS}$ falling edge hold time from CK,$\overline{CK}$	t_{DSH}	0.18	-	TBD	TBD	nCK	
MPSM Timing							
Command path disable delay upon MPSM entry	t_{MPED}	tMOD(min)+tCPDED(min)					
Valid clock requirement after MPSM entry	t_{CKMPE}	tMOD(min)+tCPDED(min)					
Valid clock requirement before MPSM exit	t_{CKMPX}	tCKSRX(min)					
Exit MPSM to commands not requiring a locked DLL	t_{XMP}	tXS(min)	-	TBD	-		
Exit MPSM to commands requiring a locked DLL	t_{XMPDLL}	tXMP(min)+tXSDLL(min)					
CS setup time to CKE	t_{MPX_S}	tISmin+tIH-min	-	TBD	-		
CS hold time to CKE	t_{MPX_H}	TBD	-	TBD	-		
Calibration Timing							
Power-up and RESET calibration time	t_{ZQinit}	1024	-	TBD	-	nCK	
Normal operation Full calibration time	t_{ZQoper}	512	-	TBD	-	nCK	
Normal operation Short calibration time	t_{ZQCS}	128	-	TBD	-	nCK	
Reset/Self Refresh Timing							
Exit Reset from CKE HIGH to a valid command	t_{XPR}	Max(5nCK,tRFC(min)+10ns)					
Exit Self Refresh to commands not requiring a locked DLL	t_{XS}	tRFC(min)+10ns					
SRX to commands not requiring a locked DLL in Self Refresh ABORT	$t_{XS\_ABORT(min)}$	Min: t_{RFC4}(min)+10ns					
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	$t_{XS\_FAST(min)}$	Min: t_{RFC4}(min)+10ns					
Exit Self Refresh to commands requiring a locked DLL	t_{XSDLL}	tDLLK(min)					
Minimum CKE low width for Self refresh entry to exit timing	t_{CKESR}	tCKE(min)+1nck					
Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled	t_{CKESR_PAR}	Min: t_{CKE}(min)+1nCK+PL					
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	t_{CKSRE}	Max:(5nCK,10ns)					

Speed		DDR4-2666		DDR4-3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	t_{CKSRE_PAR}	Max:(5nCK,10ns)+P:L					
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	t_{CKSRX}	max(snck,10ns)					
Power Down Timing							
Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	t_{XP}	max(4nCK,6ns)					
CKE minimum pulse width	t_{CKE}	max(3nCK,5ns)					31,32
Command pass disable delay	t_{CPDED}	4	-	TBD	-	nCK	
Power Down Entry to Exit Timing	t_{PD}	tCKE(min)	-	TBD	-		6
Timing of ACT command to Power Down entry	$t_{ACTPDEN}$	2	-	TBD	-	nCK	7
Timing of PRE or PREA command to Power Down entry	t_{PRPDEN}	2	-	TBD	-	nCK	7
Timing of RD/RDA command to Power Down entry	t_{RDPDEN}	RL+4+1	-	TBD	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	t_{WRPDEN}	WL+4+(tWR/tCK(avg)	-	TBD	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	$t_{WRAPDEN}$	WL+4+WR+1	-	TBD	-	nCK	5
Timing of WR command to Power Down entry (BC4MRS)	$t_{WRPBC4DEN}$	WL+2+(tWR/tCK(avg)	-	TBD	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	$t_{WRAPBC4DEN}$	WL+2+WR+1	-	TBD	-	nCK	5
Timing of REF command to Power Down entry	$t_{REFPDEN}$	2	-	TBD	-	nCK	7
Timing of MRS command to Power Down entry	$t_{MRSPDEN}$	tMOD(min)	-	TBD	-	ps	
PDA Timing							
Mode Register Set command cycle time in PDA mode	t_{MRD_PDA}	max(16nCKm,10ns)	-	TBD	-		
Mode Register Set command update delay in PDA mode	t_{MOD_PDA}	tMOD					
ODT Timing							
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	t_{AONAS}	1	9	TBD	TBD	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	t_{AOFAS}	1	9	TBD	TBD	ns	
RTT dynamic change skew	t_{ADC}	0.28	0.72	TBD	TBD	t_{CK}(avg)	
Write Leveling Timing							

Speed		DDR4-2666		DDR4-3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max		
First DQS/$\overline{DQS}$ rising edge after write leveling mode is programmed	t_{WLMRD}	40	-	TBD	TBD	nCK	
DQS/$\overline{DQS}$ delay after write leveling mode is programmed	$t_{WLDQSEN}$	25	-	TBD	TBD	nCK	
Write leveling setup time from rising CK/$\overline{CK}$ crossing to rising DQS/$\overline{DQS}$ crossing	t_{WLS}	0.13	-	TBD	TBD	t_{CK}(avg)	
Write leveling hold time from rising CK/$\overline{CK}$ crossing to rising DQS/$\overline{DQS}$ crossing	t_{WLH}	0.13	-	TBD	TBD	t_{CK}(avg)	
Write leveling output delay	t_{WLO}	0	9.5	TBD	TBD	ns	
Write leveling output error	t_{WLOE}	0	2	0	2	ns	
CA Parity Timing							
Commands not guaranteed to be executed during this time	$t_{PAR\_UNKNOWN}$	-	PL	-	TBD		
Delay from errant command to $\overline{ALERT}$ assertion	$t_{PAR\_ALERT\_ON}$	-	PL+6ns	-	TBD		
Pulse width of $\overline{ALERT}$ signal when asserted	$t_{PAR\_ALERT\_PW}$	80	160	TBD	TBD	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	$t_{PAR\_ALERT\_RSP}$	-	71	TBD	TBD	nCK	
Parity Latency	PL	5		TBD		nCK	
CRC Error Timing							
CRC error to $\overline{ALERT}$ latency	t_{CRC_ALERT}	3	13	TBD	TBD	ns	
CRC $\overline{ALERT}$ pulse width	CRC_ALERT_PW	6	10	TBD	TBD	nCK	
Geardown timing							
Exit RESET from CKE HIGH to a valid MRS geardown (T2/Reset)	t_{XPR_GEAR}	t_{XPR}		t_{XPR}			
CKE High Assert to Gear Down Enable time(T2/CKE)	t_{XS_GEAR}	t_{XS}		t_{XS}			
MRS command to Sync pulse time(T3)	t_{SYNC_GEAR}	t_{MOD}(min)+4nCK	-	t_{MOD}(min)+4nCK	-		27
Sync pulse to First valid command(T4)	t_{CMD_GEAR}	t_{MOD}		t_{MOD}			27
Geardown setup time	t_{GEAR_setup}	2	-	2	-	nCK	
Geardown hold time	t_{GEAR_hold}	2	-	2	-	nCK	
t_{REFI}							
t_{RFC1} (min)	2Gb	160	-	160	-	ns	
	4Gb	260	-	260	-	ns	
	8Gb	350	-	350	-	ns	
	16Gb	TBD	-	TBD	-	ns	

Speed		DDR4-2666		DDR4-3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max		
t_{RFC2} (min)	2Gb	110	-	110	-	ns	
	4Gb	160	-	160	-	ns	
	8Gb	260	-	260	-	ns	
	16Gb	TBD	-	TBD	-	ns	
t_{RFC4} (min)	2Gb	90	-	90	-	ns	
	4Gb	110	-	110	-	ns	
	8Gb	160	-	160	-	ns	
	16Gb	TBD	-	TBD	-	ns	

NOTE 1 Start of internal write transaction is defined as follows :

For BL8 (Fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL.

For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL.

For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL.

NOTE 2 A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled.

NOTE 3 Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.

NOTE 4 tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR/tCK to the next integer.

NOTE 5 WR in clock cycles as programmed in MR0.

NOTE 6 tREFI depends on TOPER.

NOTE 7 CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.

NOTE 8 For these parameters, the DDR4 SDRAM device supports tnPARAM[nCK]=RU{tPARAM[ns]/tCK(avg)[ns]}, which is in clock cycles assuming all inputclock jitter specifications are satisfied.

NOTE 9 When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.

NOTE 10 When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.

NOTE 11 When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.

NOTE 12 The max values are system dependent.

NOTE 13 DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are tbd.

NOTE 14 The deterministic component of the total timing. Measurement method tbd.

NOTE 15 DQ to DQ static offset relative to strobe per group. Measurement method tbd.

NOTE 16 This parameter will be characterized and guaranteed by design.

NOTE 17 When the device is operated with the input clock jitter, this parameter needs to be derated by the actual tjit(per)_total of the input clock. (output deratings are relative to the SDRAM input clock). Example tbd.

NOTE 18 DRAM DBI mode is off.

NOTE 19 DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.

NOTE 20 tQSL describes the instantaneous differential output low pulse width on DQS - $\overline{\text{DQS}}$, as measured from on falling edge to the next consecutive rising edge.

NOTE 21 tQSH describes the instantaneous differential output high pulse width on DQS - $\overline{\text{DQS}}$, as measured from on falling edge to the next consecutive rising edge.

NOTE 22 There is no maximum cycle time limit besides the need to satisfy the refresh interval tREFI.

NOTE 23 tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge .

NOTE 24 tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.

NOTE 25 Total jitter includes the sum of deterministic and random jitter terms for a specified BER. BER target and measurement method are tbd.

NOTE 26 The deterministic jitter component out of the total jitter. This parameter is characterized and gauranteed by design.

NOTE 27 This parameter has to be even number of clocks.

NOTE 28 When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.

NOTE 29 When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.

NOTE 30 When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.

NOTE 31 After CKE is registered LOW, CKE signal level shall be maintained below VILDC for tCKE specification (Low pulse width).

NOTE 32 After CKE is registered HIGH, CKE signal level shall be maintained above VIHDC for tCKE specification (

HIGH pulse width).

NOTE 33 Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.

NOTE 34 Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.

NOTE 35 This parameter must keep consistency with Speed-Bin Tables.

NOTE 36 DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.

NOTE 37 applied when DRAM is in DLL on mode.

NOTE 38 Assume no jitter on input clock signals to the DRAM

NOTE 39 Value is only valid for RONNOM =34 ohms

NOTE 40 1tCK toggle mode with setting MR4:A11 to 0

NOTE 41 2tCK toggle mode with setting MR4:A11 to 1, which is valid for DDR4-2400/2666 speed grade.

NOTE 42 1tCK mode with setting MR4:A12 to 0

NOTE 43 2tCK mode with setting MR4:A12 to 1, which is valid for DDR4-2400/2666 speed grade.

NOTE 44 The maximum read preamble is bounded by tLZ(DQS)min on the left side and tDQSCK(max) on the right side. See Clock to Data Strobe Relationship --- “Clock to Data Strobe Relationship”. Boundary of DQS Low-Z occur one cycle earlier in 2tCK toggle mode which is illustrated in Read Preamble ---- “Read Preamble”.

NOTE 45 DQ falling signal middle-point of transferring from High to Low to first rising edge of DQS diff-signal cross-point

NOTE 46 last falling of DQS diff-signal cross-point to DQ rising signal middle-point of transferring from Low to High

NOTE 47 VrefDQ value must be set to either its midpoint or Vcent_DQ(midpoint) in order to capture DQ0 or DQL0 low level for entering PDA mode.

NOTE 48 The maximun read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side. See Clock to Data Strobe Relationship

NOTE 49 Reference level of DQ output signal is specified with a midpoint as a widest part of Output signal eye which should be approximately 0.7*VDDQ as center level of the static signle-ended output peak-to-peak swing with a driver impedance of 34 ohms and an effective test load of 50 ohms to VTT =VDDQ

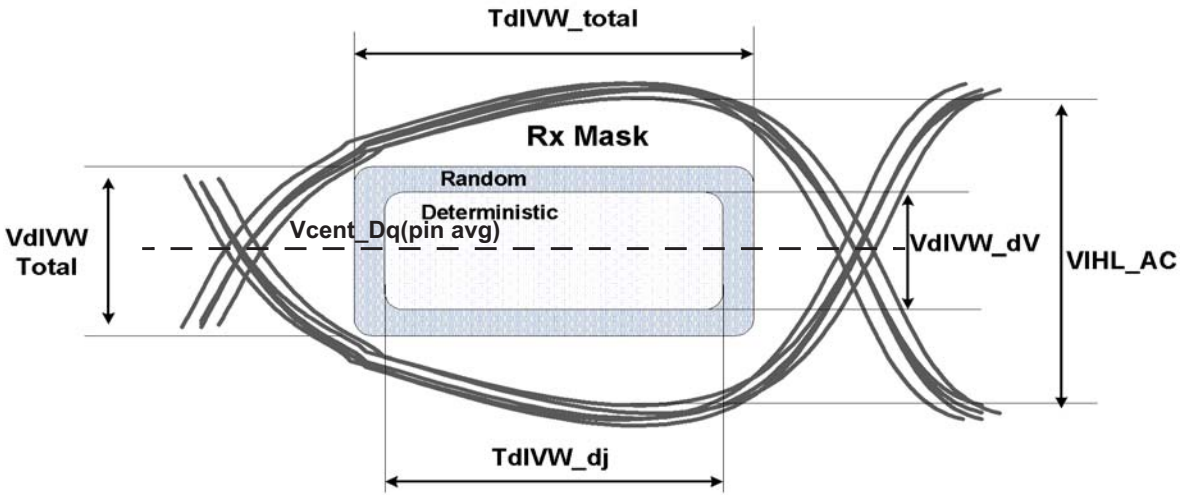
NOTE 50 For MR7 commands, the minimum delay to a subsequent non-MRS command is 5nCK.

UI=tCK(avg).min/2

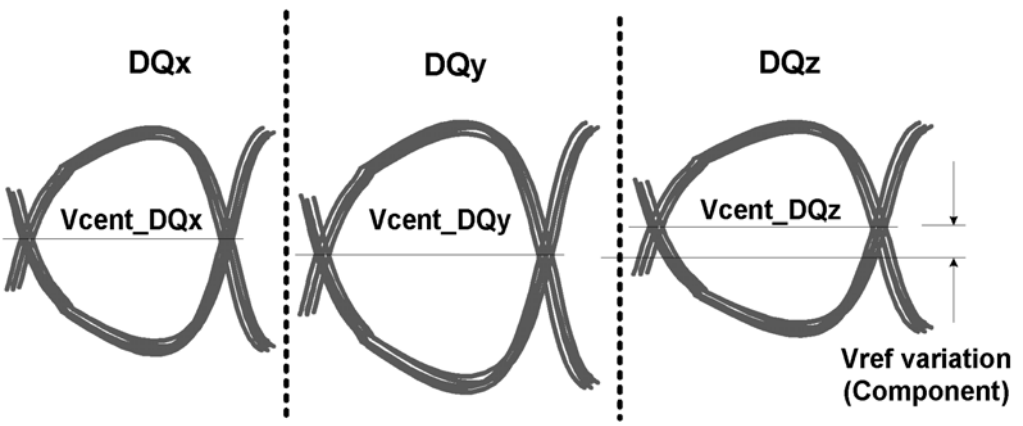
The DQ input receiver compliance mask for voltage and timing

The DQ input receiver compliance mask for voltage and timing is shown in the figure below. The receiver mask (Rx Mask) defines area the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal; it is not the valid data-eye.

DQ Receiver(Rx) compliance mask



Across pin Vref DQ voltage variation

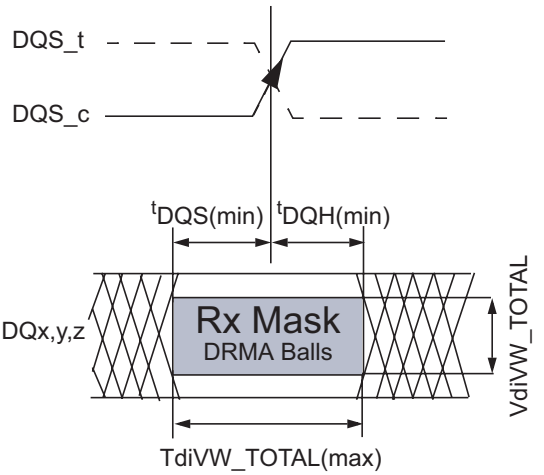


Vcent_DQ(pin avg) is defined as the midpoint between the largest Vref_DQ voltage level and the smallest Vref_DQ voltage level across all DQ pins for a given DRAM component. Each DQ pin Vref level is defined by the center, i.e. widest opening, of the cumulative data input eye as depicted in below.This clarifies that any DRAM component level variation must be accounted for within the DRAM Rx mask.The component level Vref will be set by the system to account for Ron and ODT settings.

DQ to DQS Timings at DRAM Balls

DQS, DQS Data-in at DRAM ball

Minimum Data-Eye / Maximum Rx Mask

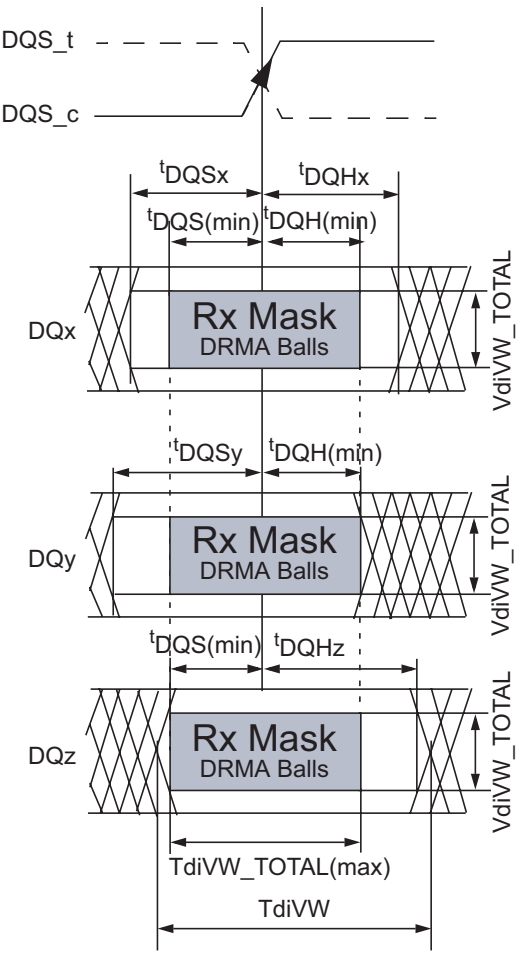


$$\frac{\text{TdiVW\_TOTAL(max)}}{2} = {}^{t}\text{DQS(min)}^{*} = {}^{t}\text{DQH(min)}^{*}$$

*NOTE: tDQS(min) and tDQH(min) are not new timing parameters, they are derived from the value of Tdivw_TOTAL(max)

DQS, DQS Data-in at DRAM ball

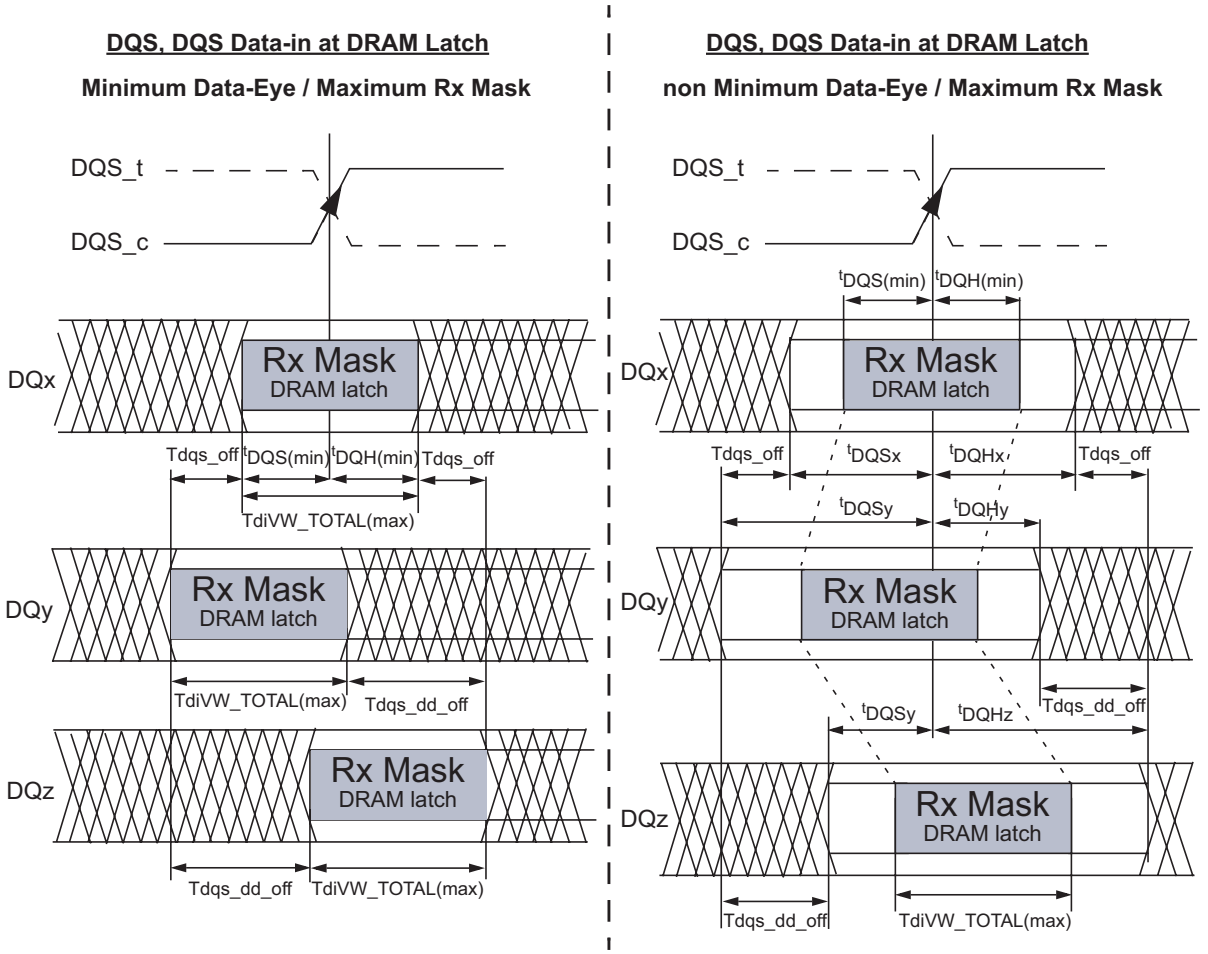
non Minimum Data-Eye / Maximum Rx Mask



NOTE: DQx represents an optimally centered input
DQy represents earliest valid transitioning input
DQz represents latest valid transitioning input

All of the timing terms in figure below are measured at the VdIVW_total voltage levels centered around Vcent_DQ(pin avg) and are referenced to the DQS/DQS center aligned to the DQ per pin.

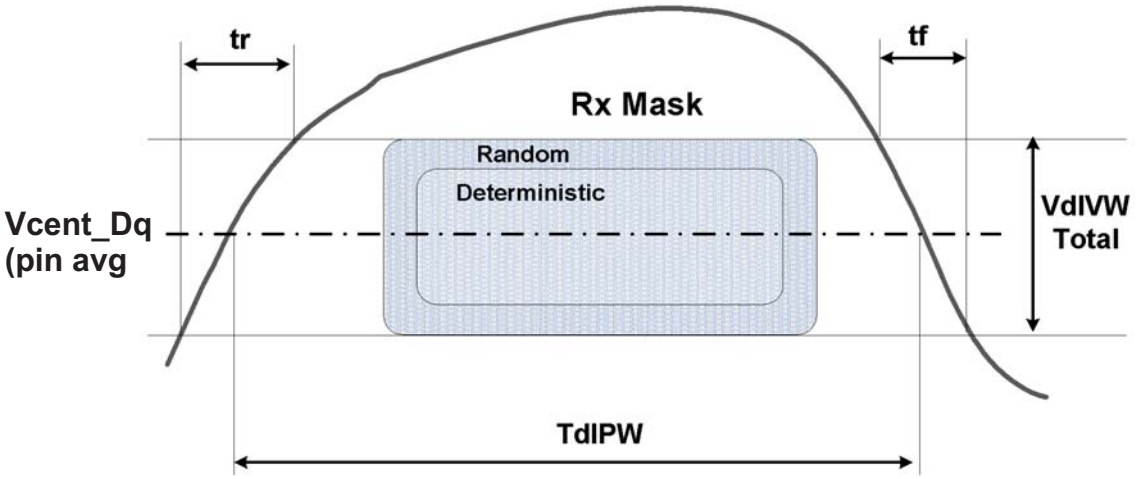
DQ to DQS Timings at DRAM latch



NOTE: DQx represents an optimally centered input
DQy represents earliest valid transitioning input
DQz represents latest valid transitioning input

All of the timing terms in figure below are measured at the VdIVW_total voltage levels centered around Vcent_DQ(pin avg) and are referenced to the DQS/$\overline{\text{DQS}}$ center aligned. Typical view assumes DQx, DQy, and DQz edges are aligned at DRAM balls.

DQ TdIPW and SRIN_dIVW definition (for each input pulse)



NOTE 1 SRIN_dIVW=VdIVW_Total/(tr or tf), signal must be monotonic within tr and tf range.

*DRAM DQs In Receive Mode ; * UI=tck(avg)min/2*

Symbol	Parameter	DDR4-1600/ 1866/2133		DDR4-2400		DDR4-2666/3200		Unit	NOTE
		min	max	min	max	min	max		
VdIVW_total	Rx Mask voltage - p-p tota	-	136 (note12)	-	130	-	120	mV	1,2,4,6
VdIVW_dV	Rx Mask voltage - deterministic	-	136	-	130	-	120	mV	1,5,13
TdIVW_total	Rx timing window total	-	0.2 (note12)	-	0.2	-	0.22	UI*	1,2,4,6
TdIVW_dj	Rx deterministic timing	-	0.2	-	0.2	-	0.22	UI*	1,5,13
VIHL_AC	DQ AC input swing pk-pk	186	-	160	-	150	-	mV	7
TdIPW	DQ input pulse width	0.58	TBD	0.58	-	0.58	-	UI*	8
Tdqs_off	DQ to DQS Setup offset	-	TBD	-	TBD	-	TBD	UI*	9
Tdqh_off	DQ to DQS Hold offset	-	TBD	-	TBD	-	TBD	UI*	9
Tdqs_dd_off	DQ to DQ Setup offset	-	TBD	-	TBD	-	TBD	UI*	10
Tdqh_dd_off	DQ to DQ Hold offset	-	TBD	-	TBD	-	TBD	UI*	10
SRIN_dIVW	Input Slew Rate over VdIVW_total	TBD	9	TBD	9	TBD	9	V/ns	11

NOTE 1 Data Rx mask voltage and timing total input valid window where VdIVW is centered around Vcent_DQ(pin avg). The data Rx mask is applied per bit and should include voltage and temperature drift terms. The design specification is BER <1e-16 and how this varies for lower BER is tbd. The BER will be characterized and extrapolated if necessary using a dual dirac method from a higher BER(tbd).
NOTE 2 Rx mask voltage AC swing peak-peak requirement over TdIVW_total with at least half of TdIVW_total(max) above Vcent_DQ(pin avg) and at least half of TdIVW_total(max) below Vcent_DQ(pin avg).

NOTE 3 Rx differential DQ to DQS jitter total timing window at the VdIVW voltage levels centered around Vcent_DQ(pin avg).
NOTE 4 Defined over the DQ internal Vref range 1.
NOTE 5 Deterministic component of the total Rx mask voltage or timing. Parameter will be characterized and guaranteed by design. Measurement method tbd.
NOTE 6 Overshoot and Undershoot Specifications tbd.
NOTE 7 DQ input pulse signal swing into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level. VIHL AC is the peak to peak voltage centered around Vcent_DQ(pin avg).
NOTE 8 DQ minimum input pulse width defined at the Vcent_DQ(pin avg).
NOTE 9 DQ to DQS setup or hold offset defined within byte from DRAM ball to DRAM internal latch; tDQS and tDQH are the minimum DQ setup and hold per DQ pin; each is equal to one-half of TdIVW_total(max).
NOTE 10 DQ to DQ setup or hold delta offset within byte. Defined as the static difference in Tdqs_off(max) and Tdqs_off(min) or Tdqh(max) - Tdqh(min) for a given component, from DRAM ball to DRAM internal latch.
NOTE 11 Input slew rate over VdIVW Mask centered at Vcent_DQ(pin avg). Slowest DQ slew rate to fastest DQ slew rate per transition edge must be within tbd V/ns of each other.
NOTE 12 The total timing and voltage terms(tdIVW_total & VdIVWtotal) are valid for any BER lower {lower fail rate} than the spec.
NOTE 13 VdIVW_total - VdIVW_dV and TdIVW_total - TdIVW_dj define the difference between random and deterministic fail mask. When VdIVW_total - VdIVW_dV = 0 and TdIVW_total - TdIVW_dj = 0, random error is assumed to be zero.

DDR4 Function Matrix

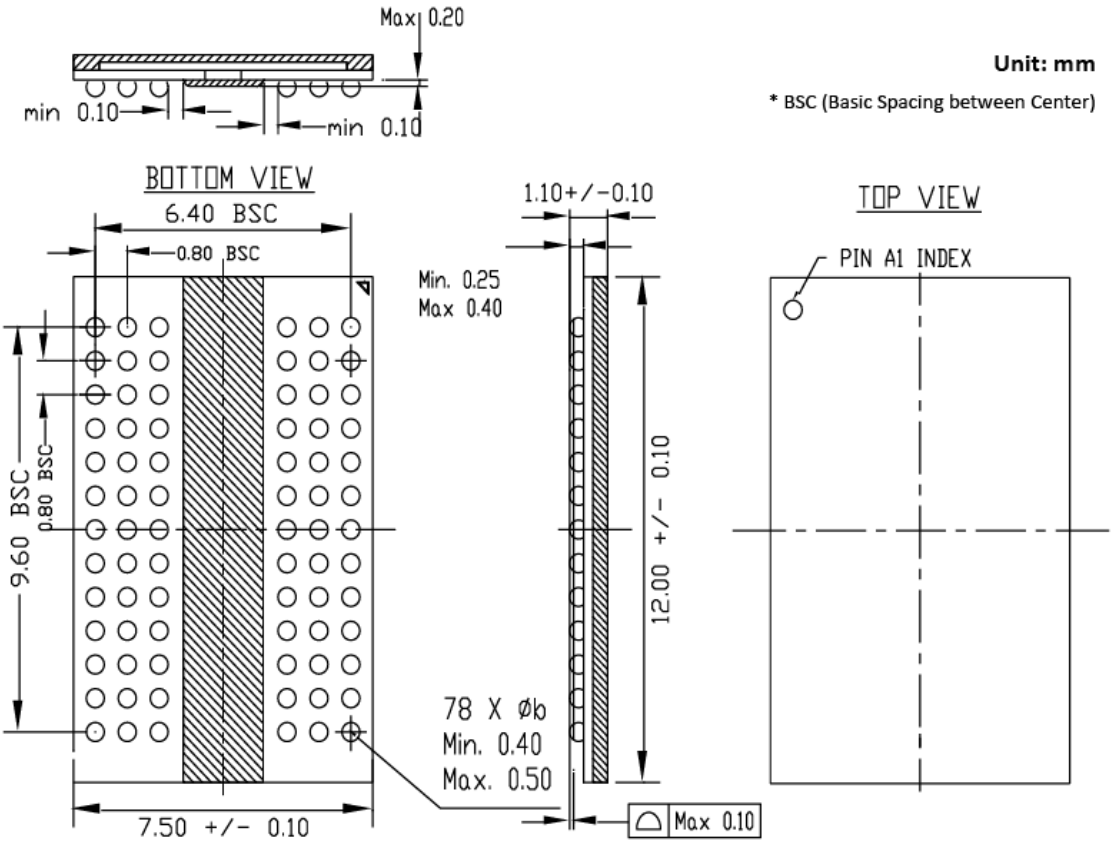
Function Matrix (By ORG. V: Supported, Blank: Not supported)

Functions	x4	x8	x16	NOTE
Write Leveling	V	V	V	
Temperature controlled Refresh	V	V	V	
Low Power Auto Self Refresh	V	V	V	
Fine Granularity Refresh	V	V	V	
Multi Purpose Register	V	V	V	
Data Mask		V	V	
Data Bus Inversion		V	V	
TDQS		V		
ZQ calibration	V	V	V	
DQ Vref Training	V	V	V	
Per DRAM Addressability	V	V	V	
Mode Register Readout	V	V	V	
CAL	V	V	V	
WRITE CRC	V	V	V	
CA Parity	V	V	V	
Control Gear Down Mode	V	V	V	
Programmable Preamble	V	V	V	
Maximum Power Down Mode	V	V		
Boundary Scan Mode			V	
Additive Latency	V	V		

Function Matrix (By Speed. V: Supported, Blank: Not supported)

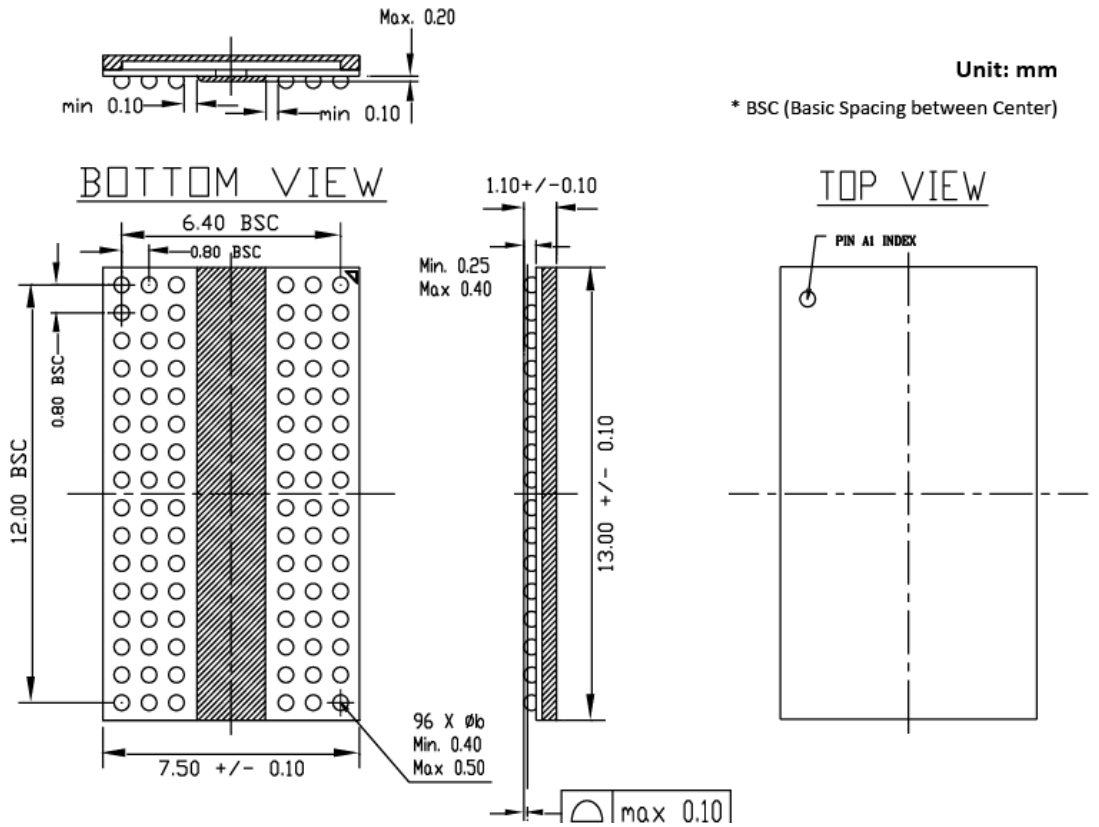
Functions	DDR4-1600/1866/2133	DDR4-2400	DDR4-2666/3200	NOTE
Write Leveling	V	V	V	
Temperature controlled Refresh	V	V	V	
Low Power Auto Self Refresh	V	V	V	
Fine Granularity Refresh	V	V	V	
Multi Purpose Register	V	V	V	
Data Mask	V	V	V	
Data Bus Inversion	V	V	V	
TDQS	V	V	V	
ZQ calibration	V	V	V	
DQ Vref Training	V	V	V	
Per DRAM Addressability	V	V	V	
Mode Register Readout	V	V	V	
CAL	V	V	V	
WRITE CRC	V	V	V	
CA Parity	V	V	V	
Control Gear Down Mode			V	
Programmable Preamble		V	V	
Maximum Power Down Mode	V	V	V	
Boundary Scan Mode	V	V	V	

Package Diagram (x8)
78-Ball Fine Pitch Ball Grid Array Outline



Package Diagram (x16)

96-Ball Fine Pitch Ball Grid Array Outline



Revision History

Revision No.	History	Draft Date	Remark
1.0	First release	April. 2019	