Delson
Technology Co, Ltd.

D75CDG04(80A/168)PC
HIGH PERFORMANCE 8Gbit DDR4 SDRAM
16 BANKS X 32Mbit X 8
8 BANKS X 32Mbit X 16

	L15	M16	N18	unit
	DDR4-2133	DDR4-2400	DDR4-2666	
System Frequency (f_{CK})	1066 MHz	1200 MHz	1333 MHz	MHz
Clock Cycle Time (t_{CK})	0.938	0.833	0.75	ns
$\overline{CAS}$ latency (CL)	15	16	18	t_{CK}

Specifications

- Density : 4G bits
- Organization :
  - 32M words x 8 bits x 16 banks (D75CDG0880APC)
  - 32M words x 16 bits x 8 banks (D75CDG08168PC)
- Package :
  - 78-ball FBGA for X8 / 96-ball FBGA for X16
  - Lead-free (RoHS compliant) and Halogen-free
- Power supply :
  - VDD, VDDQ = 1.2V ± 60mV
  - VPP = 2.5V, -125mV / +250mV
- Data rate : 2133Mbps/2400Mbps/2666Mbps
- 1KB page size for X8 / 2KB page size for X16
  - Row address: A0 to A15
  - Column address: A0 to A9
- Sixteen-banks(4 bank group with 4 banks for each bank group) for X8 and eight-banks(2 bank group with 4 banks for each bank group) for X16
- Burst lengths (BL) : BL8, BC4, BC4 or 8 on the fly
- Burst type (BT) : Sequential, Interleave
- $\overline{CAS}$ Latency (CL) : 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20
- $\overline{CAS}$ Write Latency (CWL) : 9, 10, 11, 12, 14, 16, 18
- Additive Latency (AL) : 0, CL-1, CL-2
- $\overline{CS}$ to Command Address Latency (AL) : 3, 4, 5, 6, 8
- Command Address Parity Latency : 4, 5, 6
- Write Recovery time : 10, 12, 14, 16, 18, 20, 24
- Driver strength : RZQ/7, RZQ/5 (RZQ = 240 Ω)
- RTT_PARK(34/40/48/60/80/120/240)
- RTT_NOM(34/40/48/60/80/120/240)
- RTT_WR(80/120/240)
- Read Preamble (1T/2T)
- Write Preamble (1T/2T)
- LPASR(Manual:Normal/Reduced/Extended, Auto:TS)
- Refresh cycles (Average refresh period) :
  - 7.8 μs at 0°C ≤ Tc ≤ +85°C
  - 3.9 μs at +85°C < Tc ≤ +95°C
- Operating case temperature range
  - Comercial Tc = 0°C to +95°C
  - Industrial Tc = -40°C to +95°C

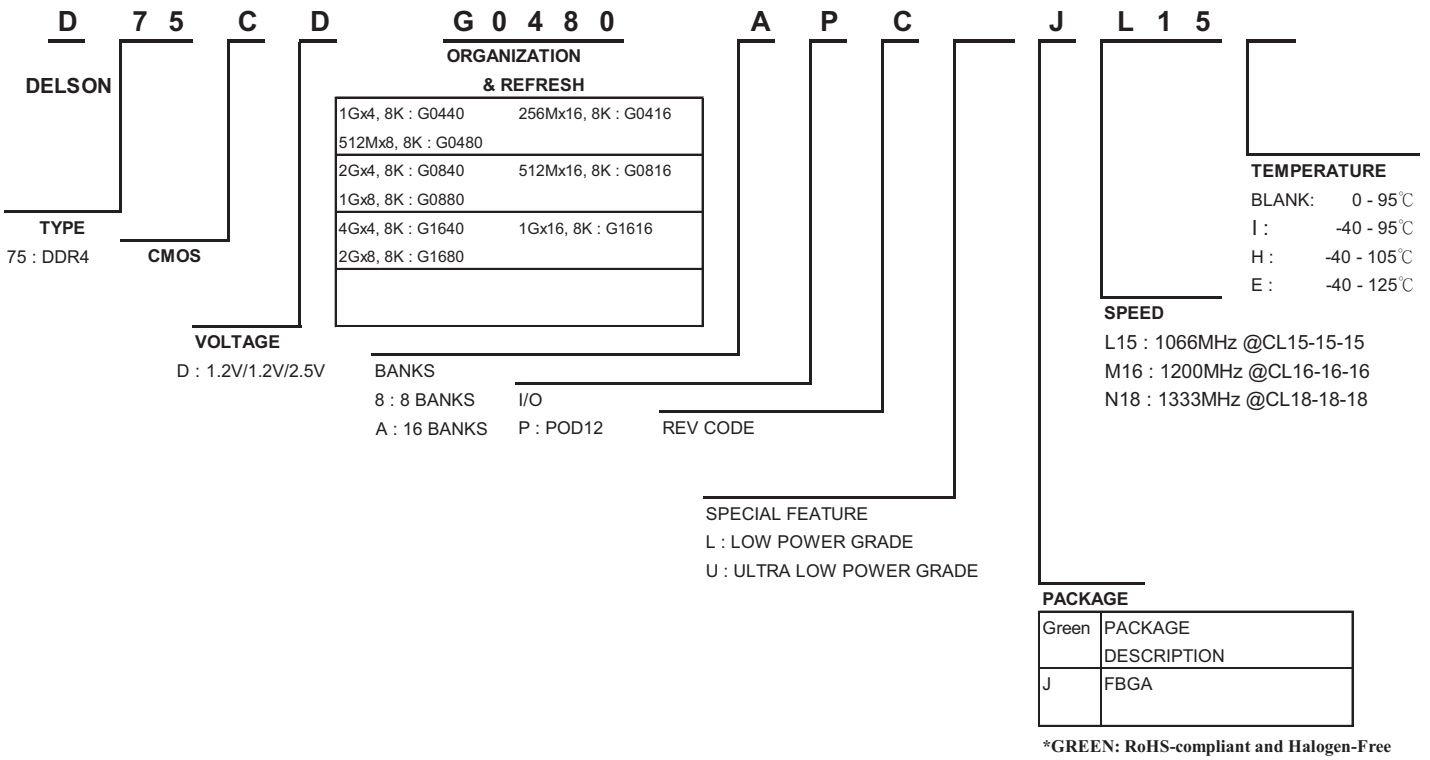
Features

- 1.2V pseudo open-drain interface
- 8n prefetch architecture
- Internal VREFDQ training
- Programmable data strobe preambles
- Data strobe preamble training
- Command/Address latency (CAL)
- Multipurpose register READ and WRITE capability
- Write and read leveling
- Auto refresh and self refresh Modes
- Low-power auto self refresh (LPASR)
- Auto Self Refresh (ASR) by DRAM built-in TS
- Fine granularity refresh
- Self refresh abort
- Maximum power saving
- Output driver calibration
- Configurable on-die termination (ODT)
- Data bus inversion (DBI) for data bus
- Command/Address (CA) parity
- Databus write cyclic redundancy check (CRC)
- Per-DRAM addressability
- Connectivity test (x16)

Device Usage Chart

Operating Temperature Range	Package Outline	Speed			Power	Temperature Mark
	78-ball FBGA 96-ball FBGA	- L15	- M16	- N18	Std.	
0°C ≤ Tc ≤ 95°C	•	•	•	•	•	Blank
-40°C ≤ Tc ≤ 95°C	•	•	•	•	•	I

Part Number Information



***GREEN: RoHS-compliant and Halogen-Free**

8Gb DDR4 SDRAM Addressing

Configuration	**1Gb x 8**	**512Mb x 16**
# of Bank	16	8
Bank Address	BA0 ~ BA1	BA0 ~ BA1
Bank Group	BG0 ~ BG1	BG0
Auto precharge	A10/AP	A10/AP
Row Address	A0 ~ A15	A0 ~ A15
Column Address	A0 ~ A9	A0 ~ A9
BC switch on the fly	A12/$\overline{BC}$	A12/$\overline{BC}$
Page size	1 KB	2 KB

Pin Configurations

78-ball FBGA (x8 configuration)

	1	2	3	4	5	6	7	8	9	
A	V_{DD}	V_{SSQ}	$\overline{TDQS}$				$\overline{DM}/\overline{DBI}/TDQS$	V_{SSQ}	V_{SS}	**A**
B	V_{PP}	V_{DDQ}	$\overline{DQS}$				DQ1	V_{DDQ}	ZQ	**B**
C	V_{DDQ}	DQ0	DQS				V_{DD}	V_{SS}	V_{DDQ}	**C**
D	V_{SSQ}	DQ4	DQ2				DQ3	DQ5	V_{SSQ}	**D**
E	V_{SS}	V_{DDQ}	DQ6				DQ7	V_{DDQ}	V_{SS}	**E**
F	V_{DD}	NC	ODT				CK	$\overline{CK}$	V_{DD}	**F**
G	V_{SS}	NC	CKE				$\overline{CS}$	NC	TEN	**G**
H	V_{DD}	$\overline{WE}$/A14	$\overline{ACT}$				$\overline{CAS}$/A15	$\overline{RAS}$/A16	V_{SS}	**H**
J	V_{REFCA}	BG0	A10/AP				A12/$\overline{BC}$	BG1	V_{DD}	**J**
K	V_{SS}	BA0	A4				A3	BA1	V_{SS}	**K**
L	$\overline{RESET}$	A6	A0				A1	A5	$\overline{ALERT}$	**L**
M	V_{DD}	A8	A2				A9	A7	V_{PP}	**M**
N	V_{SS}	A11	PAR				NC	A13	V_{DD}	**N**

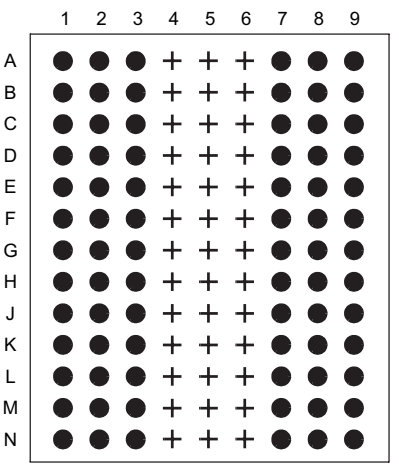
Ball Locations (x8)

● Populated ball

\+ Ball not populated

Top view

(See the balls through the package)



Pin Configurations

96-ball FBGA (x16 configuration)

	1	2	3	4	5	6	7	8	9	
A	V_{DDQ}	V_{SSQ}	DQ8				$\overline{DQSU}$	V_{SSQ}	V_{DDQ}	**A**
B	V_{PP}	V_{SS}	V_{DD}				DQSU	DQ9	V_{DD}	**B**
C	V_{DDQ}	DQ12	DQ10				DQ11	DQ13	V_{SSQ}	**C**
D	V_{DD}	V_{SSQ}	DQ14				DQ15	V_{SSQ}	V_{DDQ}	**D**
E	V_{SS}	$\overline{UDM}/\overline{UDBI}$	V_{SSQ}				$\overline{LDM}/\overline{LDBI}$	V_{SSQ}	V_{SS}	**E**
F	V_{SSQ}	V_{DDQ}	$\overline{DQSL}$				DQ1	V_{DDQ}	ZQ	**F**
G	V_{DDQ}	DQ0	DQSL				V_{DD}	V_{SS}	V_{DDQ}	**G**
H	V_{SSQ}	DQ4	DQ2				DQ3	DQ5	V_{SSQ}	**H**
J	V_{DD}	V_{DDQ}	DQ6				DQ7	V_{DDQ}	V_{DD}	**J**
K	V_{SS}	CKE	ODT				CK	$\overline{CK}$	V_{SS}	**K**
L	V_{DD}	$\overline{WE}$/A14	$\overline{ACT}$				$\overline{CS}$	$\overline{RAS}$/A16	V_{DD}	**L**
M	V_{REFCA}	BG0	A10/AP				A12/$\overline{BC}$	$\overline{CAS}$/A15	V_{SS}	**M**
N	V_{SS}	BA0	A4				A3	BA1	TEN	**N**
P	$\overline{RESET}$	A6	A0				A1	A5	$\overline{ALERT}$	**P**
R	V_{DD}	A8	A2				A9	A7	V_{PP}	**R**
T	V_{SS}	A11	PAR				NC	A13	V_{DD}	**T**

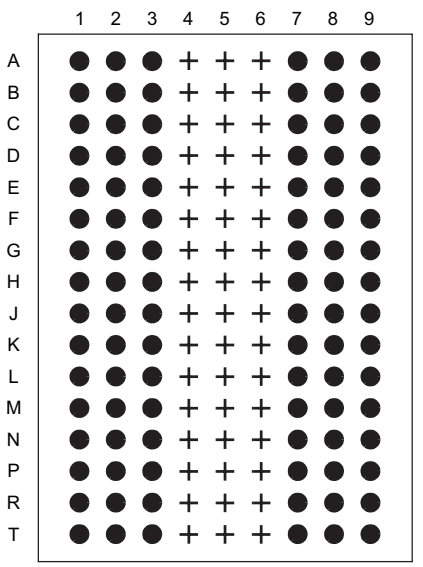
Ball Locations (x16)

● Populated ball

\+ Ball not populated

Top view

(See the balls through the package)



Signal Pin Description

Pin	Type	Function
CK, $\overline{CK}$	Input	**Clock :** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$.
CKE	Input	**Clock Enable :** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (Row Active in any bank). CKE is asynchronous for self refresh exit. After V_{REFCA} has become stable during the power on and initialization sequence, it must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self -Refresh.
$\overline{CS}$	Input	**Chip Select :** All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command code.
ODT	Input	**On Die Termination :** ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When ODT is enabled, on-die termination (RTT) is applied only to each DQ, DQS, $\overline{DQS}$, $\overline{DM}$/$\overline{DBI}$/TDQS, and $\overline{TDQS}$ signal for x4, x8 configurations (when the TDQS function is enabled via mode register). For the x16 configuration, RTT is applied to each DQ, DQSU, $\overline{DQSU}$, DQSL, $\overline{DQSL}$, $\overline{UDM}$, and $\overline{LDM}$ signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
BA0 - BA2	Input	**Bank Address Inputs :** BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
BG0 - BG1	Input	**Bank group address inputs:** Define the bank group to which a REFRESH, ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. X4/8 have BG0 and BG1 but X16 has only BG0.
$\overline{ACT}$	Input	Command input: $\overline{ACT}$ defines the Activation command being entered along with $\overline{CS}$. The input into $\overline{RAS}$/A16, $\overline{CAS}$/A15 and $\overline{WE}$/A14 will be considered as Row Address A16, A15 and A14
$\overline{RAS}$ / A16 $\overline{CAS}$ / A15 $\overline{WE}$ / A14	Input	**Command Inputs :** $\overline{RAS}$/A16, $\overline{CAS}$/A15 and $\overline{WE}$/A14 (along with $\overline{CS}$) define the command being entered. Those pins have multi function. For example, for activation with $\overline{ACT}$ Low, those are Addressing like A16,A15 and A14 but for non-activation command with $\overline{ACT}$ High, those are Command pins for Read, Write and other command defined in command truth table.
A10 / AP	Input	**Autoprecharge :** A10 is sampled during Read/Write commands to determine whether Autoprecharge should be per-formed to the accessed bank after the Read/Write operation. (HIGH:Autoprecharge; LOW: No Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). if only one bank is to be precharged, the bank is selected by bank addresses.
A12 / $\overline{BC}$	Input	**Burst Chop :** A12 is sampled during Read and Write commands to determine if burst chop(on-the-fly) will be per-formed. (HIGH : no burst chop, LOW : burst chopped). See command truth table for details.
A0 - A17	Input	**Address Inputs :** Provided the row address for Active commands and the column address for Read / Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/$\overline{BC}$, $\overline{WE}$/A14, $\overline{CAS}$/A15, $\overline{RAS}$/A16 have additional functions, see individual entries in this table). The address inputs also provide the op-code during the MODE REGISTER SET command. A16 is used on some 8Gb and 16Gb parts while A17 is only used on some 16Gb parts.

Pin	Type	Function
PAR	Input	**Parity for command and address :** DDR4 Supports Even Parity check in DRAM with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with $\overline{ACT}$, $\overline{RAS}$/A16, $\overline{CAS}$/A15, $\overline{WE}$/A14, A12/$\overline{BC}$, A10/$\overline{AP}$, A17-A0, BA0-BA1, and BG0-BG1. Input parity should maintain at the rising edge of the clock and at the same time with command & address with $\overline{CS}$ LOW. Control pins NOT covered by the PARITY signal are $\overline{CS}$, CKE, and ODT. Unused address pins that are density and configuration specific should be treated internally as 0s by the DRAM parity logic.
DQ	Input/output	**Data input/output :** Bidirectional data bus. DQ represents DQ[3:0], DQ[7:0], and DQ[15:0] for the x4, x8, and x16 configurations, respectively. If Write CRC is enabled via Mode register then the Write CRC code is added at the end of Data Burst. Either anyone or all DQ0, DQ1, DQ2, and DQ3 is used as monitoring of internal Vref level during test via Mode Register Setting MR4[4]=High, training times change when enabled. During this mode, RTT value should be set to Hi-Z. This measurement is for verification purposes and is NOT an external voltage supply pin.
DQS, $\overline{DQS}$ DQSL, $\overline{DQSL}$ DQSU, $\overline{DQSU}$	Input/ Output	**Data Strobe :** Output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQ0-DQ7; DQSU corresponds to the data on DQ8-DQ15. For the x4 and x8 configurations, DQS corresponds to the data on DQ0-DQ3 and DQ0-DQ7 respectively. DDR4 SDRAM supports a differential data strobe only and does not support a single-ended data strobe.
TDQS, $\overline{TDQS}$	Output	**Termination Data Strobe :** TDQS/$\overline{TDQS}$ is applicable for x8 DRAMs only. When enabled via Mode Register A11=1 in MR1, DRAM will enable the same termination resistance function on TDQS/$\overline{TDQS}$ that is applied to DQS/$\overline{DQS}$. When the TDQS function is disabled via the mode register, the $\overline{DM}$/$\overline{DBI}$/TDQS pin will provide the data mask ($\overline{DM}$) function or Data Bus Inversion ($\overline{DBI}$) depending on MR5, and the $\overline{TDQS}$ pin is not used. The TDQS function must be disabled in the mode register for both the x4 and x16 configurations.
$\overline{DM}$ $\overline{LDM}$, $\overline{UDM}$	Input	**Input Data Mask :** $\overline{DM}$ is an input mask signal for write data. Input data is masked when $\overline{DM}$ is sampled LOW coincident with that input data during a Write access. $\overline{DM}$ is sampled on both edges of DQS. $\overline{DM}$ is muxed with $\overline{DBI}$ function by Mode Register A[12:10] setting in MR5. For x8 device, the function of $\overline{DM}$ or TDQS is enabled by Mode Register A11 setting in MR1. $\overline{DBI}$ is an input/output identifing whether to store/output the true or inverted data. If $\overline{DBI}$ is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if $\overline{DBI}$ is HIGH. DM is not supported in X4.
$\overline{DBI}$ $\overline{UDBI}$, $\overline{LDBI}$	Input/Output	**DBI input/output :** Data bus inversion. DBI is an input/output signal used for data bus inversion in the x8 configuration. $\overline{UDBI}$ and $\overline{LDBI}$ are used in the x16 configuration; $\overline{UDBI}$ is associated with DQ8-DQ15, and LDBI is associated with DQ0-DQ7. The DBI feature is not supported on x4 configurations. $\overline{DBI}$ can be configured for both READ (output) and WRITE (input) operations depending on the mode register settings. The DM, DBI, and TDQS functions are enabled by mode egister settings. See Data Bus Inversion (DBI).
$\overline{ALERT}$	Output	**Alert output :** It has multi functions such as CRC error flag , Command and Address Parity error flag as Output signal. If there is error in CRC, then $\overline{ALERT}$ goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then $\overline{ALERT}$ goes LOW for relatively long period until on going DRAM internal recovery transaction to complete. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, open-drain $\overline{ALERT}$ Pin must be bounded to VDD on board.
TEN	Input	**Connectivity test mode :** Connectivity Test Mode is active when TEN is HIGH, and inactive when TEN is LOW. TEN must be LOW during normal operation. TEN is a CMOS rail-to-rail signal with AC HIGH and LOW at 80% and 20% of VDD (960mV for DC HIGH and 240mV for DC LOW). Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS.
ZQ	Input	**Reference pin for ZQ calibration :** This ball is tied to an external 240Ω resistor (RZQ), which is tied to VSSQ.

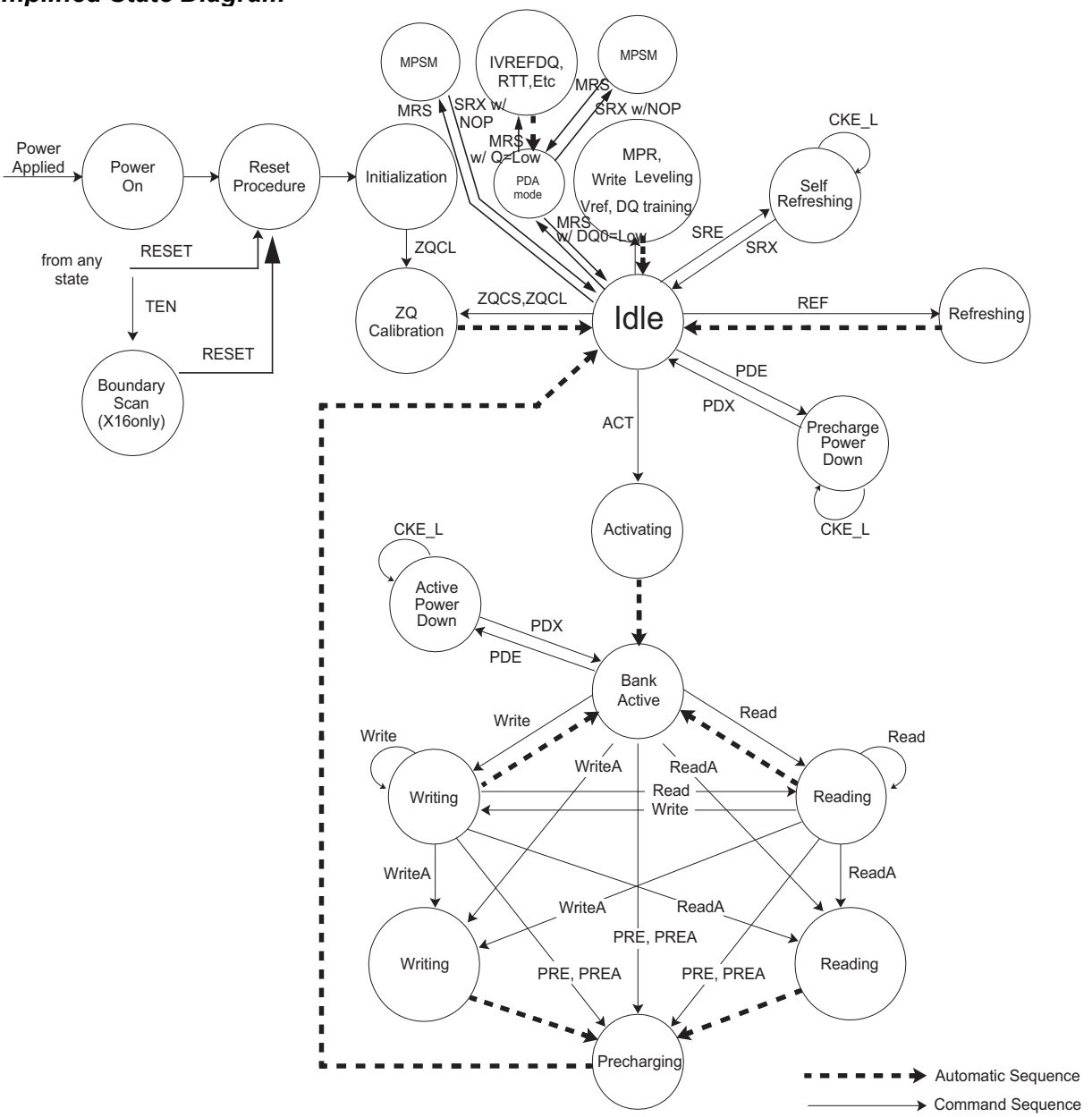
Pin	Type	Function
$\overline{\text{RESET}}$	Input	**Active Low Asynchronous Reset :** Reset is active when $\overline{\text{RESET}}$ is LOW, and inactive when $\overline{\text{RESET}}$ is HIGH. $\overline{\text{RESET}}$ must be HIGH during normal operation. $\overline{\text{RESET}}$ is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD, i.e. 1.20V for DC high and 0.30V for DC low.
VPP	Supply	**DRAM activating power supply :** 2.5V (2.375V min , 2.75V max)
VDD	Supply	**Power Supply :** 1.2V ± 0.060V
VDDQ	Supply	**DQ Power Supply :** 1.2V ± 0.060V
VSS	Supply	**Ground**
VSSQ	Supply	**DQ Ground**
VREFCA	Supply	**Reference Voltage for CA**
NC	-	**No Connect :** No internal electrical connection is present.
NF	-	**No function :** May have internal connection present, but has no function.
RFU	-	Reserved for future use.

NOTE :

1. Input only pins (BG0-BG1, BA0-BA2, A0-A17, $\overline{\text{RAS}}$/A16, $\overline{\text{CAS}}$/A15, $\overline{\text{WE}}$/A14, $\overline{\text{CS}}$, CKE, ODT and $\overline{\text{RESET}}$) do not supply termination.
2. The signal may show up in a different symbol but it indicates the same thing. e.g., /CK = CK# = #CK = $\overline{\text{CK}}$ = CKb = CK_n, /DQS = DQS# = #DQS = $\overline{\text{DQS}}$ = DQSb = DQS_n, /CS = CS# = #CS = $\overline{\text{CS}}$ = CSb = CS_n.

Functional Description

Simplified State Diagram



Abbreviation	Function	Abbreviation	Function	Abbreviation	Function
ACT	Activate	Read	RD,RDS4, RDS8	PDE	Enter Power-down
PRE	Precharge	Read A	RDA, RDAS4, RDAS8	PDX	Exit Power-down
PREA	PRECHARGE All	Write	WR, WRS4, WRS8 with/without CRC	SRE	Self-Refresh entry
MRS	Mode Register Set	Write A	WRA,WRAS4, WRAS8 with/without CRC	SRX	Self-Refresh exit
REF	Refresh, Fine granularity Refresh	RESET_n	Start RESET procedure	MPR	Multi Purpose Register
TEN	Boundary Scan Mode Enable				

NOTE This simplified State Diagram is intended to provide an overview of the possible state transitions and the commands to control them. In particular, situations involving more than on bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.

Basic Functionality

The DDR4 SDRAM is a high-speed dynamic random-access memory internally conured as sixteen-banks, 4 bank group with 4 banks for each bank group for x4/x8 and eight-banks, 2 bank group with 4 banks for each bankgroup for x16 DRAM. The DDR4 SDRAM uses a 8n prefetch architecture to achieve high-speed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR4 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write operation to the DDR4 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an ACTIVATE Command, which is then followed by a Read or Write command. The address bits registered coincident with the ACTIVATE Command are used to select the bank and row to be activated (BG0-BG1 in x4/8 and BG0 in x16 select the bankgroup; BA0-BA1 select the bank; A0-A15 select the row; refer to Addressing section for more details. The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register.

Prior to normal operation, the DDR4 SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions, and device operation.

RESET and Initialization Sequence

For power-up and reset initialization, in order to prevent DRAM from functioning improperly, default values for the following MR settings are defined:

Gear down mode (MR3 A[3]): 0 = 1/2 Rate
Per DRAM Addressability (MR3 A[4]): 0 = Disable
Max Power Saving Mode (MR4 A[1]): 0 = Disable
CS to Command/Address Latency (MR4 A[8:6]): 000 = Disable
CA Parity Latency Mode (MR5 A[2:0]): 000 = Disable

Power-up and Initialization Sequence

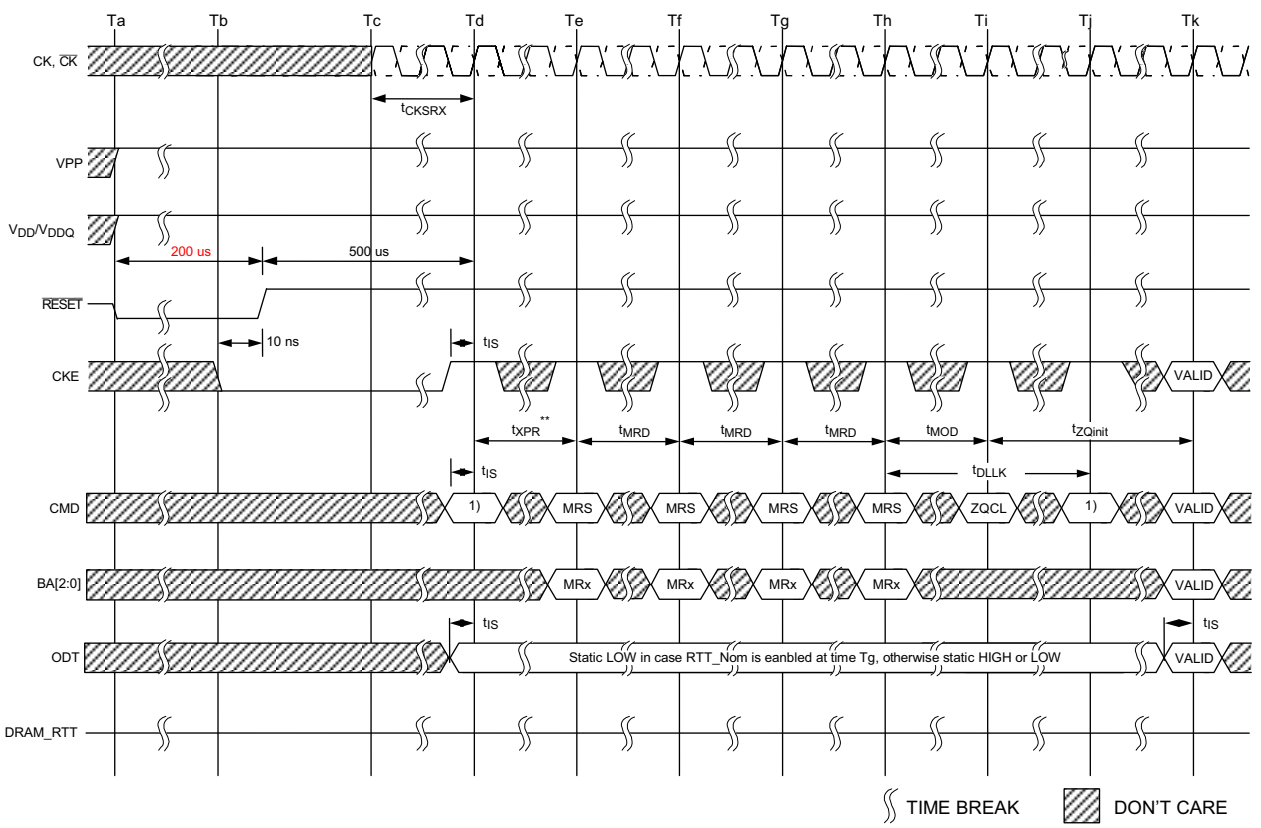
The following sequence is required for power-up and initialization:

1. Apply power ($\overline{\text{RESET}}$ is recommended to be maintained below 0.2 x VDD; all other inputs may be undefined). $\overline{\text{RESET}}$ needs to be maintained for minimum 200us with stable power. CKE is pulled LOW anytime before $\overline{\text{RESET}}$ is being deasserted (MIN time 10ns). The power voltage ramp time between 300mV to VDD, min must be no greater than 200ms, and, during the ramp, VDD must be greater than or equal to VDDQ and (VDD - VDDQ) < 0.3V. VPP must ramp at the same time or earlier than VDD, and VPP must be equal to or higher than VDD at all times.
   - VDD and VDDQ are driven from a single power converter output, AND
   - The voltage levels on all pins other than VDD,VDDQ,VSS,VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side. In addition, VTT is limited to TBDV max once power ramp is finished, AND
   - VREFCA tracks TBD.

   or
   - Apply VDD without any slope reversal before or at the same time as VDDQ.
   - Apply VDDQ without any slope reversal before or at the same time as VTT & VREFCA.
   - Apply VPP without any slope reversal before or at the same time as VDD.
   - The voltage levels on all pins other than VDD,VDDQ,VSS,VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.
2. After $\overline{\text{RESET}}$ is de-asserted, wait for another 500us until CKE becomes active. During this time, the DRAM will start internal state initialization; this will be done independently of external clocks.
3. Clocks (CK, $\overline{\text{CK}}$) need to be started and stabilized for at least 10ns or 5tCK (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding setup time to clock (tIS) must be met. Also a NOP or Deselect

command must be registered (with tIS set up time to clock) before CKE goes active. Once the CKE registered “High” after Reset, CKE needs to be continuously registered “High” until the initialization sequenceis finished, including expiration of tDLLK and tZQinit.

4. The DDR4 SDRAM keeps its on-die termination in high-impedance state as long as $\overline{\text{RESET}}$ is asserted. Further, the SDRAMkeeps its on-die termination in high impedance state after $\overline{\text{RESET}}$ deassertion until CKE is registered HIGH. The ODT inputsignal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signalmay be statically held at either LOW or HIGH. If RTT_NOM is to be enabled in MR1 the ODT input signal must be statically heldLOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expirationof tDLLK and tZQinit.
5. After CKE is registered high, wait minimum of Reset CKE Exit time, tXPR, before issuing the first MRS command to load mode register.(tXPR=Max(tXS, 5tCK))
6. Issue MRS Command to load MR3 with all application settings(To issue MRS command to MR3, provide “Low” to BG0, “High” to BA1, BA0)
7. Issue MRS command to load MR6 with all application settings (To issue MRS command to MR6, provide “Low” to BA0, “High” to BG0, BA1)
8. Issue MRS command to load MR5 with all application settings (To issue MRS command to MR5, provide “Low” to BA1, “High” to BG0, BA0)
9. Issue MRS command to load MR4 with all application settings (To issue MRS command to MR4, provide “Low” to BA1, BA0, “High” to BG0)
10. Issue MRS command to load MR2 with all application settings (To issue MRS command to MR2, provide “Low” to BG0, BA0, “High” to BA1)
11. Issue MRS command to load MR1 with all application settings (To issue MRS command to MR1, provide “Low” to BG0, BA1, “High” to BA0)
12. Issue MRS command to load MR0 with all application settings (To issue MRS command to MR0, provide “Low” to BG0, BA1, BA0)
13. Issue ZQCL command to starting ZQ calibration
14. Wait for both tDLLK and tZQ init completed
15. The DDR4 SDRAM is now ready for read/Write training (include VREF training and Write leveling).

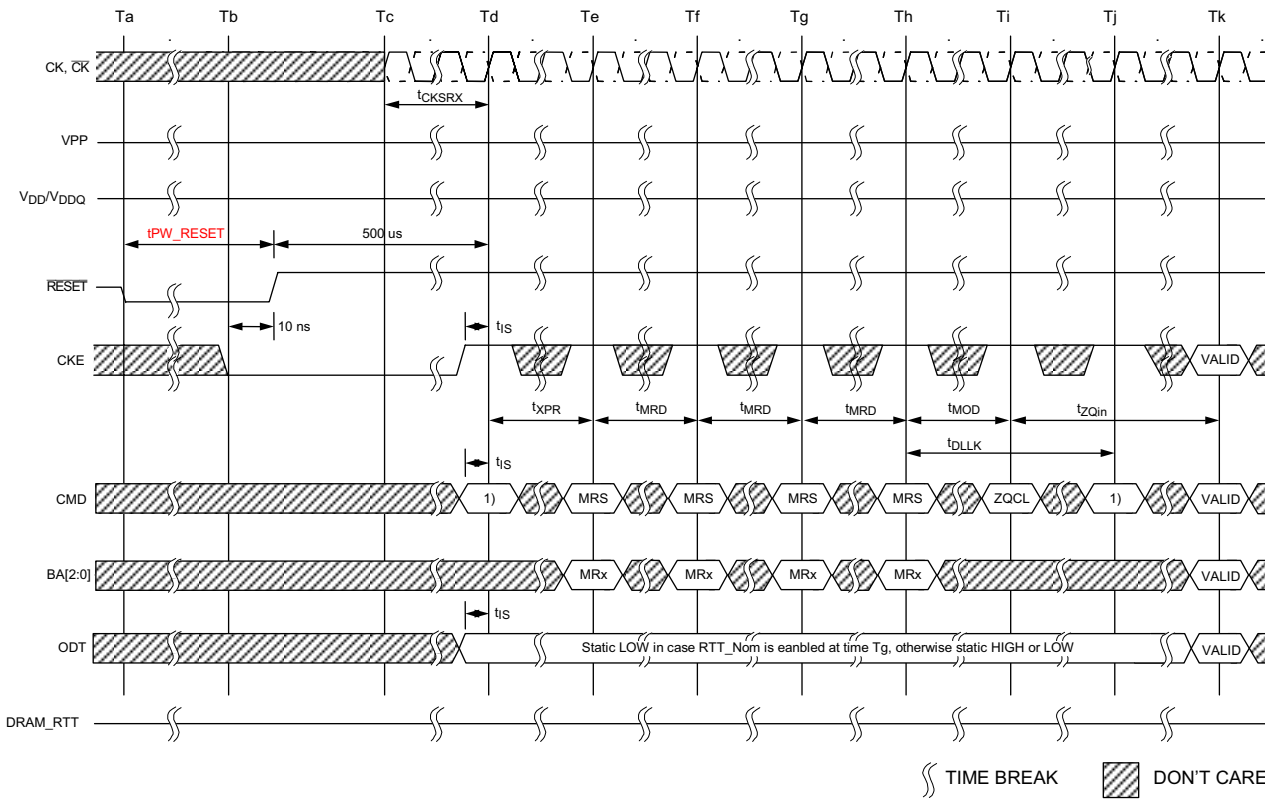


NOTE 1 From the time point Td until Tk, a DES command must be applied between MRS and ZQCL commands.
NOTE 2 MRS commands must be issued to all mode registers that have defined settings.
NOTE 3 In general, there is no specific sequence for setting the MRS locations (except for dependent or co-related features, such as ENABLE DLL in MR1 prior to RESET DLL in MR0, for example).
NOTE 4 TEN is not shown; however, it is assumed to be held LOW.

Reset and Initialization with Stable Power

The following sequence is required for RESET at no power interruption initialization:

1. Assert RESET below 0.2 x VDD anytime when reset is needed (all other inputs may be undefined). RESET needs to be maintained for minimum tPW_RESET. CKE is pulled low before RESET being de-asserted (minimum time 10ns).
2. Follow steps 2 to 10 in “Power-up Initialization Sequence”.
3. The Reset sequence is now completed, DDR4 SDRAM is ready for Read/Write training (include VREF training and Write leveling).

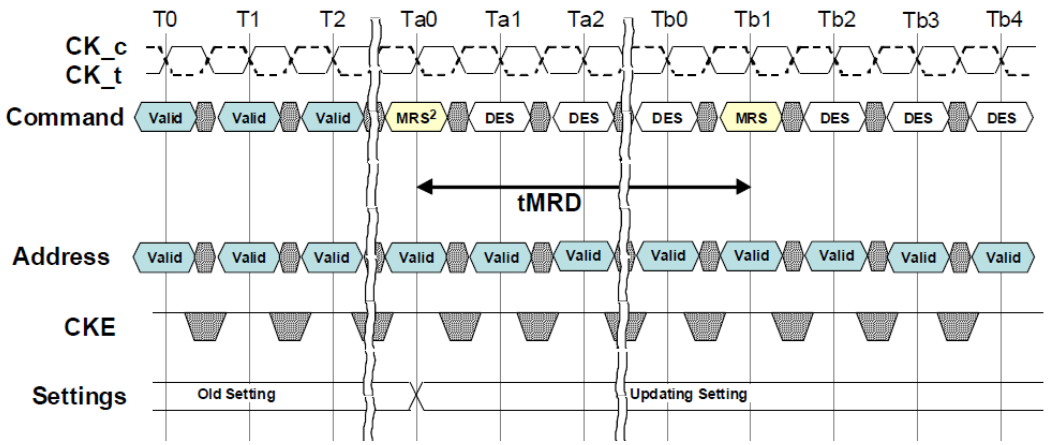


NOTE 1 From the time point Td until Tk, a DES command must be applied between MRS and ZQCL commands.
NOTE 2 MRS commands must be issued to all mode registers that have defined settings.
NOTE 3 In general, there is no specific sequence for setting the MRS locations (except for dependent or co-related features, such as ENABLE DLL in MR1 prior to RESET DLL in MR0,for example).
NOTE 4 TEN is not shown; however, it is assumed to be held LOW.

Register Definition

Programming the mode registers

For application flexibility, various functions, features, and modes are programmable in seven Mode Registers, provided by the DDR4 SDRAM, as user defined variables and they must be programmed via a Mode Register Set (MRS) command. The mode registers are divided into various fields depending on the functionality and/or modes. As not all the Mode Registers (MR#) have default values defined, contents of Mode Registers must be initialized and/or re-initialized, i. e. written, after power up and/or reset for proper operation. Also the contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS command and DLL Reset do not affect array contents, which means these commands can be executed any time after power-up without affecting the array contents. The mode register set command cycle time, tMRD is required to complete the write operation to the mode register and is the minimum time required between two MRS commands.



NOTE 1 This timing diagram shows C/A Parity Latency mode is “Disable” case.

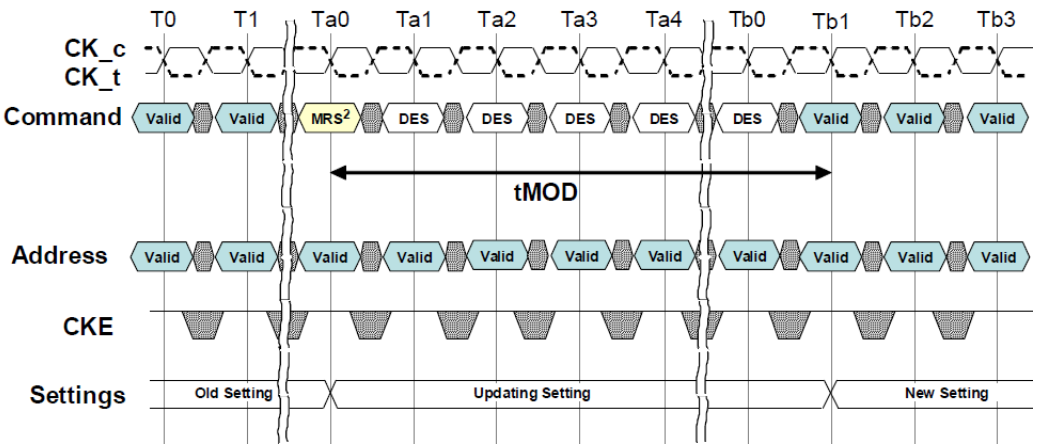
NOTE 2 List of MRS commands exception that do not apply to tMRD

- Gear down mode
- C/A Parity Latency mode
- CS to Command/Address Latency mode
- Per DRAM Addressability mode
- VREFDQ training Value, VREFDQ Training mode and VREFDQ training Range

Some of the Mode Register setting affect to address/command/control input functionality. These case, next MRS command can be allowed when the function updating by current MRS command completed.

This type of MRS command does not apply tMRD timing to next MRS command is listed in Note 2 of tMRD figure. These MRS command input cases have unique MR setting procedure, so refer to individual function description.

The most MRS command to Non-MRS command delay, tMOD, is required for the DRAM to update the features, and is the minimum time required from an MRS command to a non-MRS command excluding DES.



NOTE 1 This timing diagram shows C/A Parity Latency mode is “Disable” case.

NOTE 2 List of MRS commands exception that do not apply to tMOD

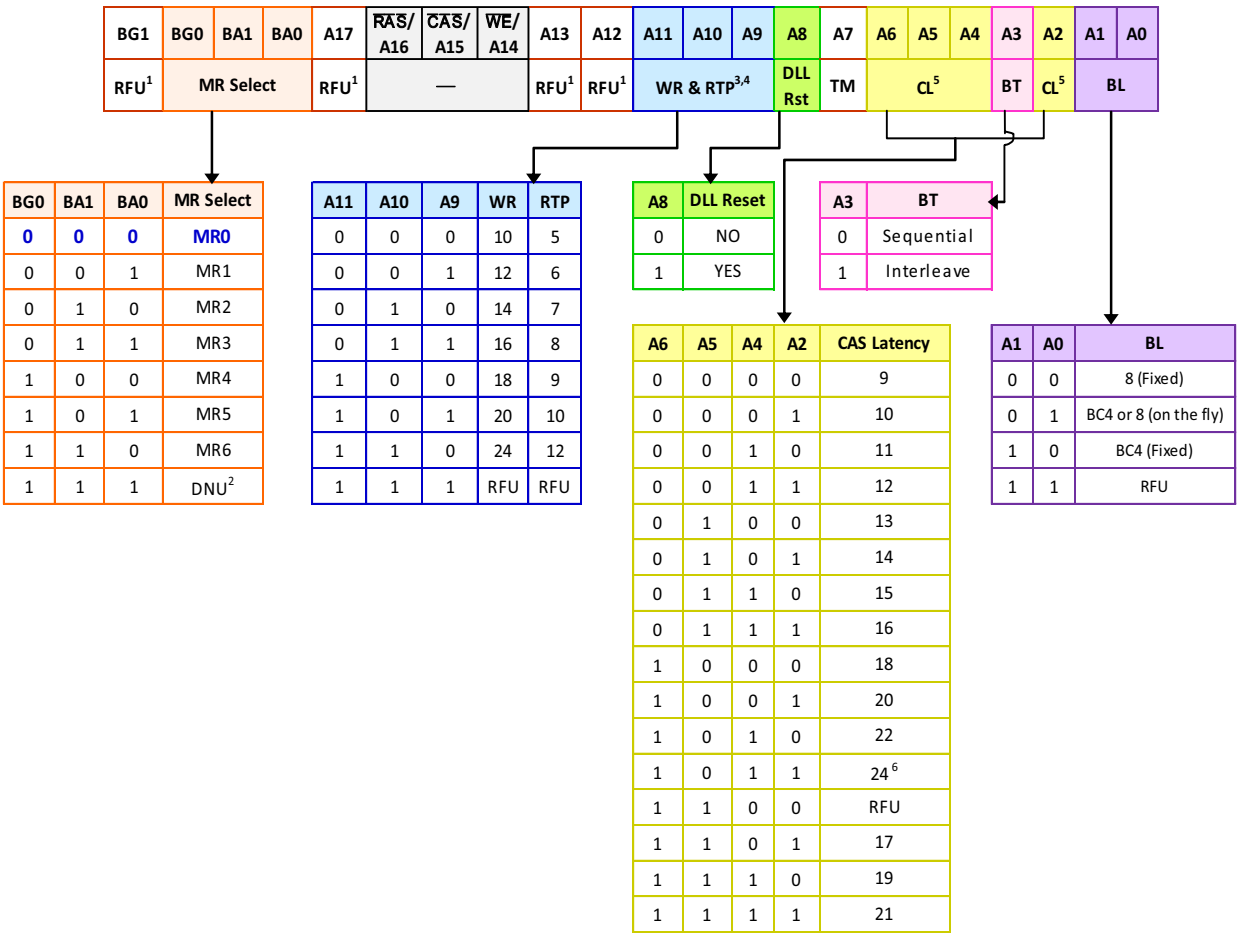
- DLL Enable, DLL Reset
- VREFDQ training Value, internal VREF Monitor, VREFDQ Training mode and VREFDQ training Range
- Gear down mode
- Per DRAM Addressability mode
- Maximum power saving mode
- CA Parity mode

The mode register contents can be changed using the same command and timing requirements during normal operation as long as the DRAM is in idle state, i.e., all banks are in the precharged state with tRP satisfied, all data bursts are completed and CKE is high prior to writing into the mode register. For MRS command, If RTT_Nom function is intended to change (enable to disable and vice versa) or already enabled in DRAM MR, ODT signal must be registered Low ensuring RTT_NOM is in an off state prior to MRS command affecting RTT_NOM turn-on and off timing. Refer to note2 of tMOD figure for this type of MRS. The ODT signal may be registered high after tMOD has expired. ODT signal is a don’t care during MRS command if DRAM RTT_Nom function is disabled in the mode register prior and after an MRS command.

Some of the mode register setting cases, function updating takes longer than tMOD. This type of MRS does not apply tMOD timing to next valid command excluding DES is listed in note 2 of tMOD figure. These MRS command input cases have unique MR setting procedure, so refer to individual function description.

Mode Register

Mode Register MR0



BG0	BA1	BA0	MR Select
0	0	0	MR0
0	0	1	MR1
0	1	0	MR2
0	1	1	MR3
1	0	0	MR4
1	0	1	MR5
1	1	0	MR6
1	1	1	DNU[2]

A11	A10	A9	WR	RTP
0	0	0	10	5
0	0	1	12	6
0	1	0	14	7
0	1	1	16	8
1	0	0	18	9
1	0	1	20	10
1	1	0	24	12
1	1	1	RFU	RFU

A8	DLL Reset
0	NO
1	YES

A3	BT
0	Sequential
1	Interleave

A6	A5	A4	A2	CAS Latency
0	0	0	0	9
0	0	0	1	10
0	0	1	0	11
0	0	1	1	12
0	1	0	0	13
0	1	0	1	14
0	1	1	0	15
0	1	1	1	16
1	0	0	0	18
1	0	0	1	20
1	0	1	0	22
1	0	1	1	24[6]
1	1	0	0	RFU
1	1	0	1	17
1	1	1	0	19
1	1	1	1	21

A1	A0	BL
0	0	8 (Fixed)
0	1	BC4 or 8 (on the fly)
1	0	BC4 (Fixed)
1	1	RFU

NOTE 1 Please refer to addressing table. If the address is available, it must be programmed to 0 during MRS
NOTE 2 Reserved for Register control word setting. DRAM ignores MR command with BG0,BA[1:0]=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.
NOTE 3 WR (write recovery for autoprecharge)min in clock cycles is calculated by dividing tWR(in ns) by tCK(in ns) and rounding up to the next integer:WRmin[cycles] = Roundup(tWR[ns] / tCK[ns]). The WR value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with tRP to determine tDAL.
NOTE 4 The table shows the encodings for Write Recovery and internal Read command to Precharge command delay. For actual Write recovery timing, please refer to AC timing table.
NOTE 5 The table only shows the encodings for a given Cas Latency. For actual supported Cas Latency, please refer to speed bin tables for each frequency.
NOTE 6 When CL is equal to 24 or more than 24, AL does not support CL-1.

Burst Length, Type and Order

Accesses within a given burst may be programmed to sequential or interleaved order. The burst type is selected via bit A3 of Mode Register MR0. The ordering of accesses within a burst is determined by the burst length, burst type, and the starting column address as shown in the following table. The burst length is defined by bits A0-A1 of Mode Register MR0. Burst length options include fixed BC4, fixed BL8, and 'on the fly' which allows BC4 or BL8 to be selected coincident with the registration of a Read or Write command via A12/$\overline{BC}$.

Burst Length	Read/ Write	Starting Column Adress(A2,A1,A0)	burst type = Sequential (decimal) A3=0	burst type = Interleaved (decimal) A3=1	NOTE
BC4	Read	0 0 0	0,1,2,3,T,T,T,T	0,1,2,3,T,T,T,T	1,2,3
		0 0 1	1,2,3,0,T,T,T,T	1,0,3,2,T,T,T,T	1,2,3
		0 1 0	2,3,0,1,T,T,T,T	2,3,0,1,T,T,T,T	1,2,3
		0 1 1	3,0,1,2,T,T,T,T	3,2,1,0,T,T,T,T	1,2,3
		1 0 0	4,5,6,7,T,T,T,T	4,5,6,7,T,T,T,T	1,2,3
		1 0 1	5,6,7,4,T,T,T,T	5,4,7,6,T,T,T,T	1,2,3
		1 1 0	6,7,4,5,T,T,T,T	6,7,4,5,T,T,T,T	1,2,3
		1 1 1	7,4,5,6,T,T,T,T	7,6,5,4,T,T,T,T	1,2,3
	Write	0 v v	0,1,2,3,X,X,X,X	0,1,2,3,X,X,X,X	1,2,4,5
		1 v v	4,5,6,7,X,X,X,X	4,5,6,7,X,X,X,X	1,2,4,5
BL8	Read	0 0 0	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2
		0 0 1	1,2,3,0,5,6,7,4	1,0,3,2,5,4,7,6	2
		0 1 0	2,3,0,1,6,7,4,5	2,3,0,1,6,7,4,5	2
		0 1 1	3,0,1,2,7,4,5,6	3,2,1,0,7,6,5,4	2
		1 0 0	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3	2
		1 0 1	5,6,7,4,1,2,3,0	5,4,7,6,1,0,3,2	2
		1 1 0	6,7,4,5,2,3,0,1	6,7,4,5,2,3,0,1	2
		1 1 1	7,4,5,6,3,0,1,2	7,6,5,4,3,2,1,0	2
	Write	v v v	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2,4

NOTE 1 In case of burst length being fixed to 4 by MR0 setting, the internal write operation starts two clock cycles earlier than for the BL8 mode. This means that the starting point for tWR and tWTR will be pulled in by two clocks. In case of burst length being selected on-the-fly via A12/$\overline{BC}$, the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for tWR and tWTR will not be pulled in by two clocks.

NOTE 2 0...7 bit number is value of CA[2:0] that causes this bit to be the first read during a burst.

NOTE 3 T : Output driver for data and strobes are in high impedance.

NOTE 4 V : A valid logic level (0 or 1), but respective buffer input ignores level on input pins.

NOTE 5 X : Don't Care.

CAS Latency (CL)

The CAS latency setting is defined in the MR0 Register Definition table. CAS latency is the delay, in clock cycles, between the internal READ command and the availability of the first bit of output data. DDR4 SDRAM does not support any half-clock latencies. The overall read latency (RL) is defined as additive latency (AL) + CAS latency (CL); RL = AL + CL.

Test Mode

The normal operating mode is selected by MR0[7] and all other bits set to the desired values shown in the MR0 Register Definition table. Programming MR0[7] to a 1 places the DDR4 SDRAM into a DRAM manufacturer defined test mode that is to be used only by the DRAM manufacturer; and should not be used by the end user. No operations or functionality is specified if MR0[7] = 1.

Write Recovery/Read to Precharge

The programmed WR value MR0[11:9] is used for the auto precharge feature along with tRP to determine tDAL. WR (write recovery for auto precharge) MIN in clock cycles is calculated by dividing tWR (in ns) by tCK (in ns) and rounding up to the next integer:

WRmin[cycles] = roundup (tWR[ns]/tCK[ns])

The WR must be programmed to be equal to or larger than tWR(MIN). When both DM and Write CRC are enabled in the DRAM mode register, the DRAM calculates CRC before sending the write data into the array; tWR values will change when enabled. If there is a CRC error, the DRAM blocks the write operation and discards the data.

RTP (internal READ command to PRECHARGE command delay for auto precharge) min in clock cycles is calculated by dividing tRTP (in ns) by tCK (in ns) and rounding up to the next integer:

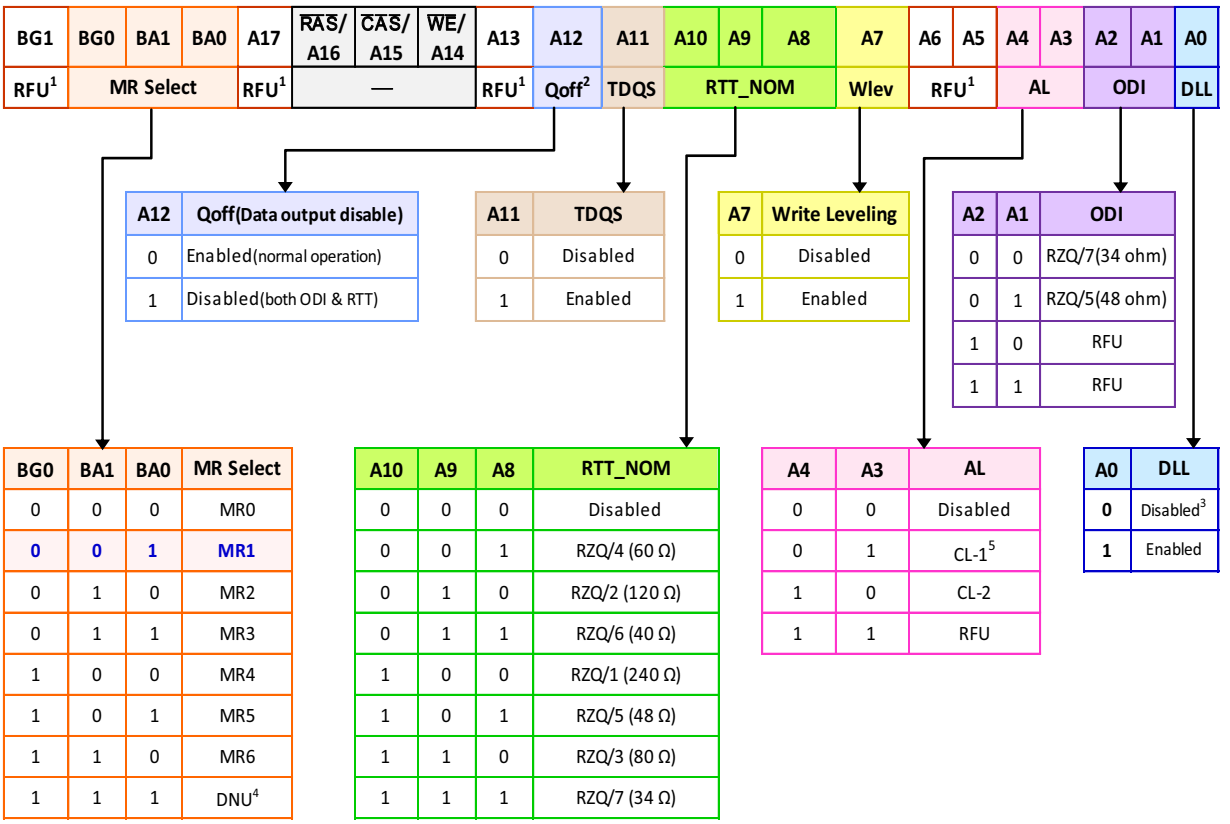
RTPmin[cycles] = roundup (tRTP[ns]/tCK[ns])

The RTP value in the mode register must be programmed to be equal or larger than RTPmin. The programmed RTP value is used with tRP to determine the act timing to the same bank.

DLL Reset

The DLL reset bit is self-clearing, meaning that it returns back to the value of 0 after the DLL reset function has been issued. After the DLL is enabled, a subsequent DLL RESET should be applied. Any time that the DLL reset function is used, tDLLK must be met before any functions that require the DLL can be used (for example, READ commands or ODT synchronous operations).

Mode Register MR1



NOTE 1 Please refer to addressing table. If the address is available, it must be programmed to 0 during MRS

NOTE 2 Outputs disabled - DQs, DQSs, $\overline{\text{DQS}}$s.

NOTE 3 States reversed to “0 as Disable” with respect to DDR4.

NOTE 4 Reserved for Register control word setting. DRAM ignores MR command with BG0,BA[1:0]=111 and doesn’t respond. When RFU MR code setting is inputted, DRAM operation is not defined.

NOTE 5 Not allowed when 1/4 rate geardown mode is enabled.

DLL Enable/DLL Disable

The DLL must be enabled for normal operation and is required during power-up initialization and upon returning to normal operation after having the DLL disabled. During normal operation, (DLL-enabled) with MR1[0], the DLL is automatically disabled when entering the SELF REFRESH operation and is automatically re-enabled upon exit of the SELF REFRESH operation. Any time the DLL is enabled and subsequently reset, tDLLK clock cycles must occur before a READ or SYNCHRONOUS ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tDQSCK, tAON, or tAOF parameters.

During tDLLK, CKE must continuously be registered HIGH. DDR4 SDRAM does not require DLL for any WRITE operation, except when RTT_WR is enabled and the DLL is required for proper ODT operation.

The direct ODT feature is not supported during DLL-off mode. The ODT resistors must be disabled by continuously registering the ODT pin LOW and/or by programming the RTT_NOM bits MR1[9,6,2] = 000 via a MODE REGISTER SET command during DLL-off mode.

The dynamic ODT feature is not supported in DLL-off mode; to disable dynamic ODT externally, use the MRS command to set RTT_WR, MR2[10:9] = 00.

Output Driver Impedance Control

The output driver impedance of the DDR4 SDRAM device is selected by MR1[2,1].

ODT RTT_NOM Values

DDR4 SDRAM is capable of providing three different termination values: RTT_Static, RTT_NOM, and RTT_WR. The nominal termination value, RTT_NOM, is programmed in MR1. A separate value (RTT_WR) may be programmed in MR2 to enable a unique RTT value when ODT is enabled during WRITEs. The RTT_WR value can be applied during WRITEs even when RTT_NOM is disabled. A third RTT value, RTT_Static, is programed in MR5. RTT_Static provides a termination value when the ODT signal is LOW.

Additive Latency (AL)

The additive latency (AL) operation is supported to make command and data bus efficient for sustainable bandwidths in DDR4 SDRAM. In this operation, the DDR4 SDRAM allows a READ or WRITE command (either with or without AUTO PRECHARGE) to be issued immediately after the ACTIVE command. The command is held for the time of AL before it is issued inside the device. The read latency (RL) is controlled by the sum of the AL and CAS latency (CL) register settings. Write latency (WL) is controlled by the sum of the AL and CAS write latency (CWL) register settings.

Write Leveling

For better signal integrity, DDR4 memory modules use fly-by topology for the commands,addresses, control signals, and clocks. Fly-by topology has the benefit of reducing the number of stubs and their length, but it also causes flight-time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the controller to maintain tDQSS, tDSS, and tDSH specifications. Therefore, the DDR4 SDRAM supports a write-leveling feature, which allows the controller to compensate for skew.

Output Disable

The DDR4 SDRAM outputs may be enabled/disabled by MR1[12]. When MR1[12] = 1 is enabled, all output pins (such as DQ, DQS, and $\overline{\text{DQS}}$) are disconnected from the device, which removes any loading of the output drivers. This feature may be useful when measuring module power, for example.For normal operation, set MR1[12] = 0.

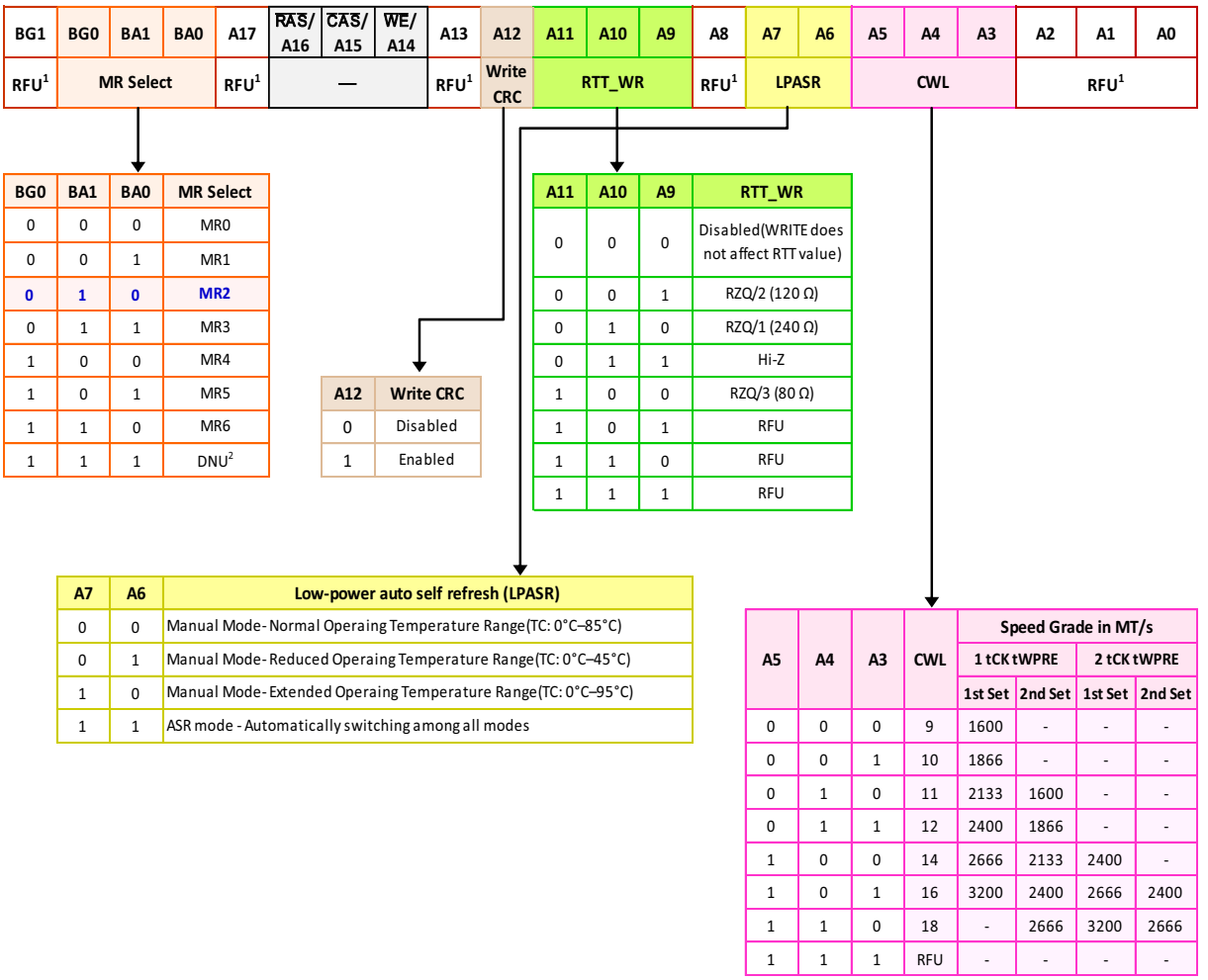
Termination Data Strobe (TDQS)

Termination data strobe (TDQS) is a feature of x8 DDR4 SDRAM and provides additional termination resistance outputs that may be useful in some system configurations. Because the TDQS function is available only in x8 DDR4 SDRAM, it must be disabled for x4 and x16 configurations. TDQS is not supported in x4 or x16 configurations. When enabled via the mode register, the same termination resistance function that is applied to the TDQS and $\overline{\text{TDQS}}$ pins is applied to the DQS and $\overline{\text{DQS}}$ pins.

The TDQS, DBI, and data mask functions share the same pin. When the TDQS function is enabled via the mode register, the data mask and DBI functions are not supported. When the TDQS function is disabled, the data mask and DBI functions can be enabled separately.

TDQS	Data Mask (DM)	WRITE DBI	READ DBI
Disabled	Enabled	Disabled	Enabled or disabled
	Disabled	Enabled	Enabled or disabled
	Disabled	Disabled	Enabled or disabled
Enabled	Disabled	Disabled	Disabled

Mode Register MR2



BG1	BG0	BA1	BA0	A17	RAS/ A16	CAS/ A15	WE/ A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
RFU[1]	MR Select			RFU[1]	—			RFU[1]	Write CRC	RTT_WR			RFU[1]	LPASR		CWL			RFU[1]		

BG0	BA1	BA0	MR Select
0	0	0	MR0
0	0	1	MR1
0	1	0	MR2
0	1	1	MR3
1	0	0	MR4
1	0	1	MR5
1	1	0	MR6
1	1	1	DNU[2]

A12	Write CRC
0	Disabled
1	Enabled

A11	A10	A9	RTT_WR
0	0	0	Disabled(WRITE does not affect RTT value)
0	0	1	RZQ/2 (120 Ω)
0	1	0	RZQ/1 (240 Ω)
0	1	1	Hi-Z
1	0	0	RZQ/3 (80 Ω)
1	0	1	RFU
1	1	0	RFU
1	1	1	RFU

A7	A6	Low-power auto self refresh (LPASR)
0	0	Manual Mode- Normal Operaing Temperature Range(TC: 0°C–85°C)
0	1	Manual Mode- Reduced Operaing Temperature Range(TC: 0°C–45°C)
1	0	Manual Mode- Extended Operaing Temperature Range(TC: 0°C–95°C)
1	1	ASR mode - Automatically switching among all modes

A5	A4	A3	CWL	Speed Grade in MT/s			
				1 tCK tWPRE		2 tCK tWPRE	
				1st Set	2nd Set	1st Set	2nd Set
0	0	0	9	1600	-	-	-
0	0	1	10	1866	-	-	-
0	1	0	11	2133	1600	-	-
0	1	1	12	2400	1866	-	-
1	0	0	14	2666	2133	2400	-
1	0	1	16	3200	2400	2666	2400
1	1	0	18	-	2666	3200	2666
1	1	1	RFU	-	-	-	-

NOTE 1 Please refer to addressing table. If the address is available, it must be programmed to 0 during MRS
NOTE 2 Reserved for Register control word setting. DRAM ignores MR command with BG0, BA[1:0]=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

CAS Write Latency (CWL)

CAS write latency (CWL) is defined by MR2[5:3] as shown in the MR2 Register Definition table. CWL is the delay, in clock cycles, between the internal WRITE command and the availability of the first bit of input data. DDR4 SDRAM does not support any half-clock latencies. The overall write latency (WL) is defined as additive latency (AL) + CAS write latency (CWL); WL = AL + CWL.

Low-Power Auto Self Refresh (LPASR)

Low-power auto self refresh (LPASR) is supported in DDR4 SDRAM. Applications requiring SELF REFRESH operation over different temperature ranges can use this feature to optimize the IDD6 current for a given temperature range as specified in the MR2 Register Definition table.

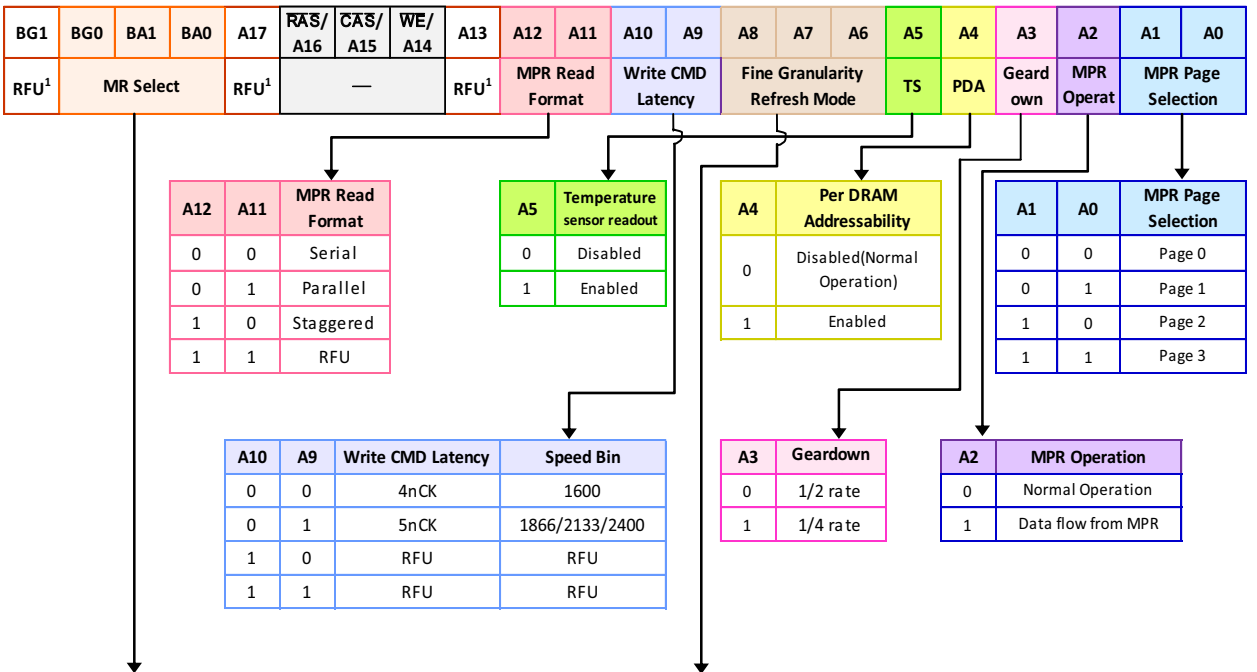
Dynamic ODT (RTT_WR)

In certain applications and to further enhance signal integrity on the data bus, it is desirable to change the termination strength of the DDR4 SDRAM without issuing an MRS command. Configure the Dynamic ODT settings in MR2[11:9]. In write-leveling mode, only RTT_NOM is available.

Write Cyclic Redundancy Check (CRC) Data Bus

The Write cyclic redundancy check (CRC) data bus feature during Writes has been added to DDR4 SDRAM. When enabled via the mode register, the data transfer size goes from the normal 8-bit (BL8) frame to a larger 10-bit UI frame, and the extra 2UIs are used for the CRC information.

Mode Register MR3



A12	A11	MPR Read Format
0	0	Serial
0	1	Parallel
1	0	Staggered
1	1	RFU

A5	Temperature sensor readout
0	Disabled
1	Enabled

A4	Per DRAM Addressability
0	Disabled(Normal Operation)
1	Enabled

A1	A0	MPR Page Selection
0	0	Page 0
0	1	Page 1
1	0	Page 2
1	1	Page 3

A10	A9	Write CMD Latency	Speed Bin
0	0	4nCK	1600
0	1	5nCK	1866/2133/2400
1	0	RFU	RFU
1	1	RFU	RFU

A3	Geardown
0	1/2 rate
1	1/4 rate

A2	MPR Operation
0	Normal Operation
1	Data flow from MPR

BG0	BA1	BA0	MR Select
0	0	0	MR0
0	0	1	MR1
0	1	0	MR2
0	1	1	MR3
1	0	0	MR4
1	0	1	MR5
1	1	0	MR6
1	1	1	DNU2

A8	A7	A6	Fine Granularity Refresh
0	0	0	Normal (Fixed 1x)
0	0	1	Fixed 2x
0	1	0	Fixed 4x
0	1	1	RFU
1	0	0	RFU
1	0	1	On-the-fly 1x/2x
1	1	0	On-the-fly 1x/4x
1	1	1	RFU

NOTE 1 Please refer to addressing table. If the address is available, it must be programmed to 0 during MRS
NOTE 2 Reserved for Register control word setting. DRAM ignores MR command with BG0,BA[1:0]=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

WRITE CMD latency when CRC/DM enabled

The Write Command Latency (WCL) must be set when both Write CRC and DM are enabled for Write CRC persistent mode. This provides the extra time required when completing a Write burst when Write CRC and DM are enabled.

Fine Granularity Refresh Mode

This mode had been added to DDR4 to help combat the performance penalty due to refresh lockout at high densities. Shortening tRFC and increasing cycle time allows more accesses to the chip and can produce higher bandwidth.

Temp Sensor Status

This mode directs the DRAM to update the temperature sensor status at MPR Page 2, MPR0 [4,3]. The temperature sensor setting should be updated within 32ms; at the time of MPR Read of the Temperature Sensor Status bits, the tem-

perature sensor status should be no older than 32ms.

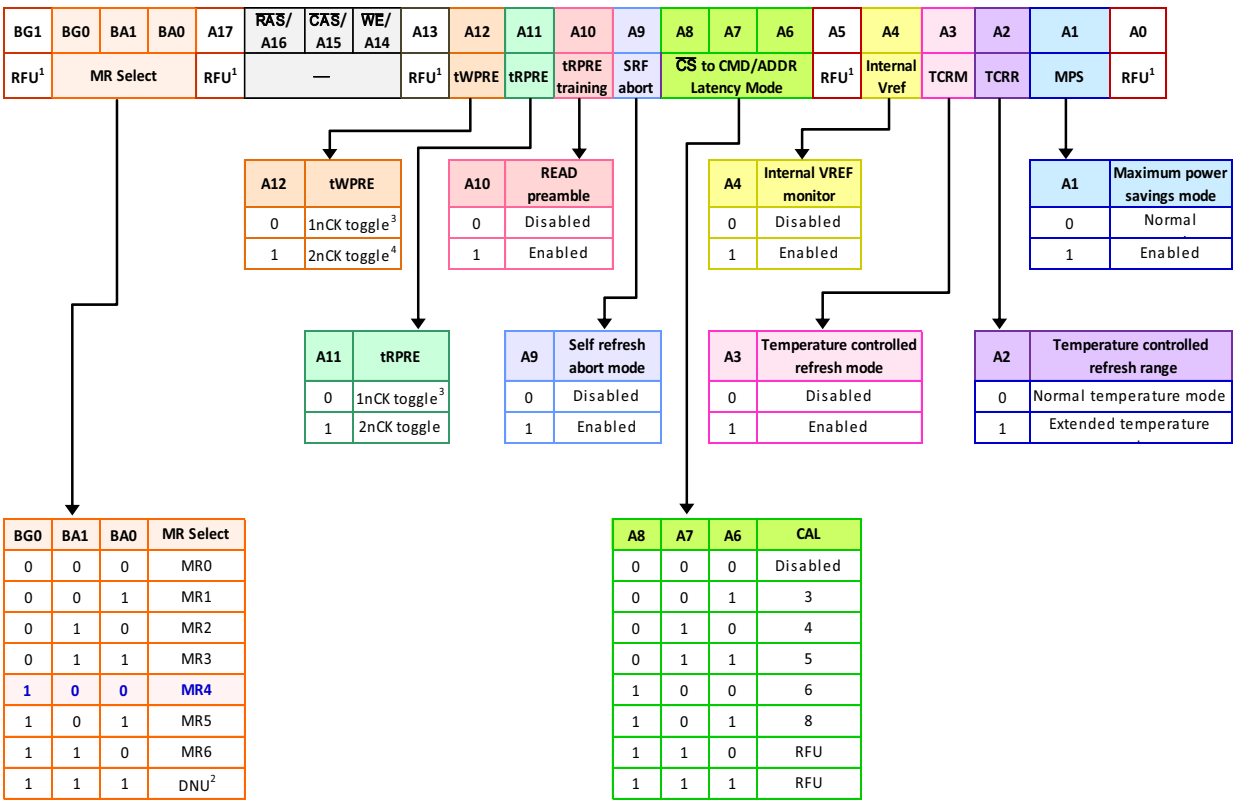
Per-DRAM Addressability

The MRS command mask allows programmability of a given device that may be in the same rank (devices sharing the same command and address signals). As an example, this feature can be used to program different ODT or VREF values on DRAM devices within a given rank.

Gear-down Mode

The DDR4 SDRAM defaults in half-rate (1N) clock mode and utilizes a low frequency MRS command followed by a sync pulse to align the proper clock edge for operating the control lines $\overline{CS}$, CKE, and ODT when in quarter-rate (2N) mode. For operation in half-rate mode, no MRS command or sync pulse is required.

Mode Register MR4



NOTE 1 Please refer to addressing table. If the address is available, it must be programmed to 0 during MRS
NOTE 2 Reserved for Register control word setting .DRAM ignores MR command with BG0,BA[1:0]=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.
NOTE 3 Not allowed when 1/4 rate Gear-down mode is enabled.
NOTE 4 When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range.

WRITE Preamble

DDR4 SDRAM introduces a programmable WRITE preamble tWPRE that can either be set to 1tCK or 2 tCK via the MR4 register. Note the 1tCK setting is similar to DDR3; however, the 2tCK setting is different. When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range. Check the table of CWL Selection for details.

READ Preamble

DDR4 SDRAM introduces a programmable READ preamble tRPRE that can be set to either 1tCK or 2tCK via the MR4 register. Note that both the 1tCK and 2tCK DDR4 preamble settings are different from what DDR3 SDRAM defined. Both of these READ preamble settings may require the memory controller to train (or READ-level) its data strobe receivers using the READ preamble training.

READ Preamble Training

DDR4 supports programmable READ preamble settings (1tCK or 2tCK). This mode can be used by the memory controller to train or READ level its data strobe receivers.

Temperature-Controlled Refresh (MR4[3] = 1 & MR2[6:7]=11)

When temperature-controlled refresh mode is enabled, the DDR4 SDRAM may adjust the internal refresh period to be longer than tREFI of the normal temperature range by skipping external refresh commands with the proper gear ratio. For example, the DRAM temperature sensor detected less than 45'C. Normal temperature mode covers the range of 0'C to 85'C, while the extended temperature range covers 0'C to 95'C.

Command Address Latency (CAL)

DDR4 supports the command address latency (CAL) function as a power savings feature. This feature can be enabled or disabled via the MRS setting. CAL is defined as the delay in clock cycles (tCAL) between a $\overline{CS}$ registered LOW and its corresponding registered command and address. The value of CAL (in clocks) must be programmed into the mode register and is based on the roundup (in clocks) of [tCAL(ns)/tCK(ns)].

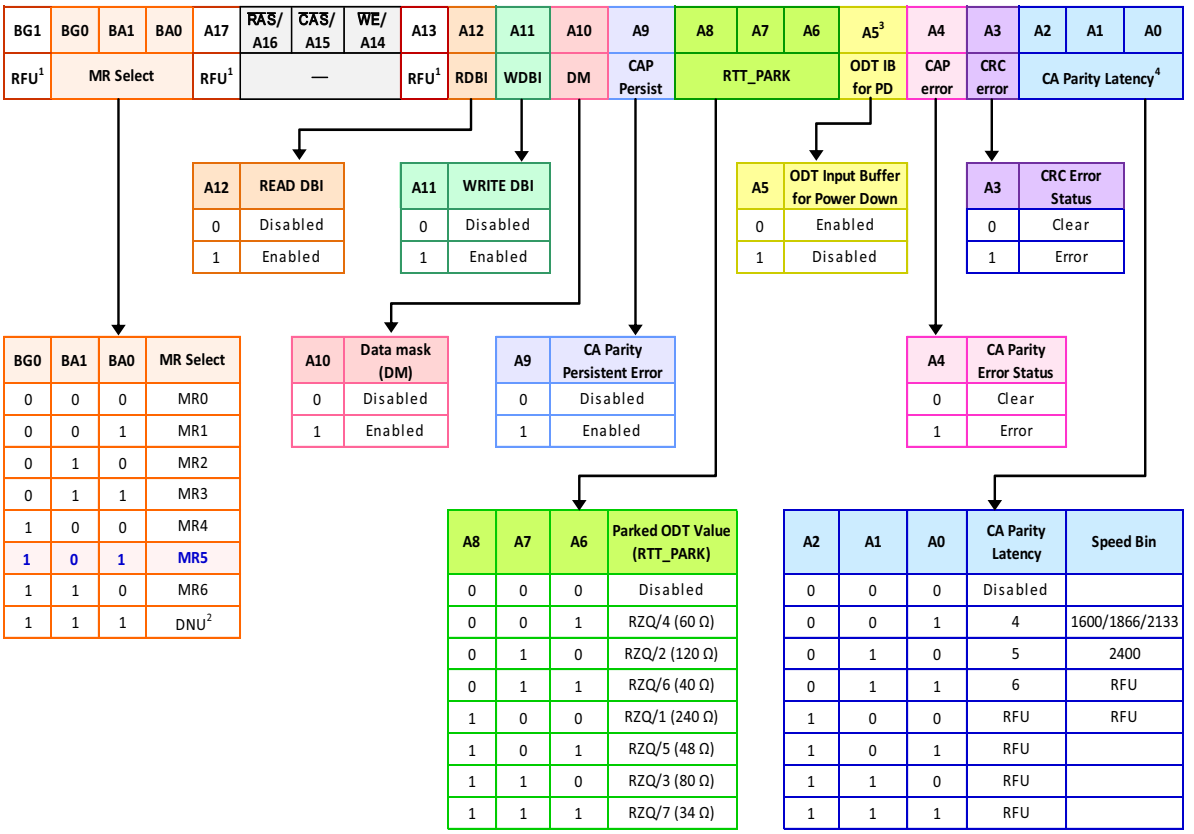
Internal VREF Monitor

DDR4 generates its own internal VREFDQ. This mode is allowed to be enabled during VREFDQ training and when enabled, VREF_time-short and VREF_time-long need to be increased by 10ns if DQ0, or DQ1, or DQ2, or DQ3 have 0pF loading; and add an additional 15ns per pF of added loading.

Maximum Power Savings Mode

This mode provides the lowest power mode where data retention is not required. When DDR4 SDRAM is in the maximum power saving mode, it does not need to guarantee data retention or respond to any external command (except maximum power saving mode exit command and during the assertion of $\overline{RESET}$ signal LOW).

Mode Register MR5



NOTE 1 Please refer to addressing table. If the address is available, it must be programmed to 0 during MRS
NOTE 2 Reserved for Register control word setting. DRAM ignores MR command with BG0,BA[1:0]=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.
NOTE 3 When RTT_NOM Disable is set in MR1, A5 of MR5 will be ignored.
NOTE 4 Parity latency must be programmed according to timing parameters by speed grade table.

Data Bus Inversion (DBI)

The data bus inversion (DBI) function has been added to DDR4 SDRAM and is supported for x8 and x16 configurations only (x4 is not supported). The DBI function shares a common pin with the DM and TDQS functions. The DBI function applies to both READ and WRITE operations and cannot be enabled at the same time the DM function is enabled. Refer to the TDQS Function Matrix table for valid configurations for all three functions (TDQS/DM/DBI).

Data Mask (DM)

The data mask (DM) function, also described as a partial write, has been added to DDR4 SDRAM and is supported for x8 and x16 configurations only (x4 is not supported). The DM function shares a common pin with the DBI and TDQS functions. The DM function applies only to WRITE operations and cannot be enabled at the same time the DBI function is enabled. Refer to the TDQS Function Matrix table for valid configurations for all three functions (TDQS/DM/DBI).

CA Parity Persistent Error Mode

Normal CA Parity Mode (CA Parity Persistent Mode disabled) no longer performs CA parity checking while the parity error status bit remains set at 1. However, with CA Parity Persistent Mode enabled, CA parity checking continues to be performed when the parity error status bit is set to a 1.

ODT Input Buffer for Power Down

Determines whether the ODT input buffer is on or off during Power Down. If the ODT input buffer is configured to be on (enabled during power down), the ODT input signal must be at a valid logic level. If the input buffer is configured to be off (disabled during power down), the ODT input signal may be floating and the DRAM does not provide RTT_NOM termination. The DRAM may, however, provide Rtt_Park termination depending on the MR settings. This is primarily for additional power savings.

CA Parity Error Status

DRAM will set the error status bit to 1 upon detecting a parity error. The parity error status bit remains set at 1 until the DRAM Controller clears it explicitly using an MRS command.

CRC Error Status

DRAM will set the error status bit to 1 upon detecting a CRC error. The CRC error status bit remains set at 1 until the DRAM controller clears it explicitly using an MRS command.

C/A Parity Latency Mode

CA Parity is enabled when a latency value, dependent on tCK, is programmed; this accounts for parity calculation delay internal to the DRAM. The normal state of CA Parity is to be disabled. If CA parity is enabled, the DRAM has to ensure that there are no parity errors before executing the command. CA Parity signal (PAR) covers $\overline{\text{ACT}}$, $\overline{\text{RAS}}$/A16 , $\overline{\text{CAS}}$/A15, $\overline{\text{WE}}$/A14, and the address bus including bank address and bank group bits. The control signals CKE, ODT and $\overline{\text{CS}}$ are not included in the parity calculation.

Mode Register MR6

BG1	BG0	BA1	BA0	A17	RAS/ A16	CAS/ A15	WE/ A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
RFU[1]	MR Select			RFU[1]	—			RFU[1]	tCCD_L[3]			RFU[1]		VrefDQ Training	VrefDQ Range	VrefDQ Training Value					

BG0	BA1	BA0	MR Select
0	0	0	MR0
0	0	1	MR1
0	1	0	MR2
0	1	1	MR3
1	0	0	MR4
1	0	1	MR5
1	1	0	MR6
1	1	1	DNU[2]

A12	A11	A10	tCCD_L.min(nCK)	Remark [4]
0	0	0	4	≦2400Mbps
0	0	1	5	TBD
0	1	0	6	TBD
0	1	1	7	TBD
1	0	0	8	TBD
1	0	1	RFU	
1	1	0	RFU	
1	1	1	RFU	

A7	VrefDQ Training Enable
0	Disabled
1	Enabled

A6	VrefDQ Range
0	Range 1
1	Range 2

MR6 [5:0]	Range 1 (MR6[6]=0)	Range 2 (MR6[6]=1)	MR6 [5:0]	Range 1 (MR6[6]=0)	Range 2 (MR6[6]=1)	MR6 [5:0]	Range 1 (MR6[6]=0)	Range 2 (MR6[6]=1)	MR6 [5:0]	Range 1 (MR6[6]=0)	Range 2 (MR6[6]=1)
00 0000	60.00%	45.00%	00 1101	68.45%	53.45%	01 1010	76.90%	61.90%	10 0111	85.35%	70.35%
00 0001	60.65%	45.65%	00 1110	69.10%	54.10%	01 1011	77.55%	62.55%	10 1000	86.00%	71.00%
00 0010	61.30%	46.30%	00 1111	69.75%	54.75%	01 1100	78.20%	63.20%	10 1001	86.65%	71.65%
00 0011	61.95%	46.95%	01 0000	70.40%	55.40%	01 1101	78.85%	63.85%	10 1010	87.30%	72.30%
00 0100	62.60%	47.60%	01 0001	71.05%	56.05%	01 1110	79.50%	64.50%	10 1011	87.95%	72.95%
00 0101	63.25%	48.25%	01 0010	71.70%	56.70%	01 1111	80.15%	65.15%	10 1100	88.60%	73.60%
00 0110	63.90%	48.90%	01 0011	72.35%	57.35%	10 0000	80.80%	65.80%	10 1101	89.25%	74.25%
00 0111	64.55%	49.55%	01 0100	73.00%	58.00%	10 0001	81.45%	66.45%	10 1110	89.90%	74.90%
00 1000	65.20%	50.20%	01 0101	73.65%	58.65%	10 0010	82.10%	67.10%	10 1111	90.55%	75.55%
00 1001	65.85%	50.85%	01 0110	74.30%	59.30%	10 0011	82.75%	67.75%	11 0000	91.20%	76.20%
00 1010	66.50%	51.50%	01 0111	74.95%	59.95%	10 0100	83.40%	68.40%	11 0001	91.85%	76.85%
00 1011	67.15%	52.15%	01 1000	75.60%	60.60%	10 0101	84.05%	69.05%	11 0010	92.50%	77.50%
00 1100	67.80%	52.80%	01 1001	76.25%	61.25%	10 0110	84.70%	69.70%	11 0011 to 111111	Reserved	Reserved

NOTE 1 Please refer to addressing table. If the address is available, it must be programmed to 0 during MRS
NOTE 2 Reserved for Register control word setting. DRAM ignores MR command with BG0,BA[1:0]=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.
NOTE 3 tCCD_L should be programmed according to the value defined in AC parameter table per operating frequency.
NOTE 4 It's not finalized. Might be changed.

tCCD_L Programming

The DRAM Controller must program the correct tCCD_L value. tCCD_L will be programmed according to the value defined in the AC parameter table per operating frequency.

VREFDQ Training Enable

VREFDQ Training is where the DRAM internally generates it's own VREFDQ used by the DQ input receivers. The DRAM controller must use a MRS protocol (adjust up, adjust down, etc.) for setting and calibrating the internal VREFDQ level. The procedure is a series of Writes and Reads in conduction with VREFDQ adjustments to optimize and verify the data eye. Enabling VREFDQ Training should be used whenever MR6[6:0] register values are being written to.

VREFDQ Training Range

DDR4 defines two VREFDQ training ranges - Range 1 and Range 2. Range 1 supports VREFDQ between 60% and 92% of VDDQ while Range 2 supports VREFDQ between 45% and 77% of VDDQ. Range 1 is targeted for module based designs and Range 2 is added targeting point-to point designs.

VREFDQ Training Value

Fifty settings provided 0.65% of granularity steps sizes for both Range 1 and Range 2 of VREFDQ.

DRAM MR7 Ignore

The DDR4 SDRAM shall ignore any access to MR7 for all DDR4 SDRAM.Any bit setting within MR7 may not take any effect in the DDR4 SDRAM.

DDR4 SDRAM Command Description and Operation

Command Truth Table

(a) Note 1,2,3 and 4 apply to the entire Command truth table

(b) Note 5 applies to all Read/Write commands

[BG=Bank Group Address, BA=Bank Address, RA=Row Address, CA=Column Address, $\overline{BC}$=Burst Chop, X=Don't Care, V=Valid].

Function	Abbre-viation	CKE		$\overline{CS}$	$\overline{ACT}$	$\overline{RAS}$/A14	$\overline{CAS}$/A15	$\overline{WE}$/A14	BG0-BG1	BA0-BA1	C2-C0	A12/$\overline{BC}$	A17, A13, A11	A10/AP	A0-A9	NOTE
		Previous Cycle	Current Cycle													
Mode Register Set	MRS	H	H	L	H	L	L	L	BG	BA	V	OP Code				12
Refresh	REF	H	H	L	H	L	L	H	V	V	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	H	L	L	H	V	V	V	V	V	V	V	7,9
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	7,8,9,10
				L	H	H	H	H	V	V	V	V	V	V	V	
Single Bank Pre-charge	PRE	H	H	L	H	L	H	L	BG	BA	V	V	V	L	V	
Precharge all Banks	PREA	H	H	L	H	L	H	L	V	V	V	V	V	H	V	
RFU	RFU	H	H	L	H	L	H	H	RFU							
Bank Activate	ACT	H	H	L	L	Row Address (RA)			BG	BA	V	Row Address (RA)				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	H	L	L	BG	BA	V	V	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	H	L	L	BG	BA	V	L	V	L	CA	
Write (BL8, on the Fly)t	WRS8	H	H	L	H	H	L	L	BG	BA	V	H	V	L	CA	
Write with Auto Pre-charge(Fixed BL8 or BC4)	WRA	H	H	L	H	H	L	L	BG	BA	V	V	V	H	CA	
Write with Auto Pre-charge(BC4, on the Fly)	WRAS4	H	H	L	H	H	L	L	BG	BA	V	L	V	H	CA	
Write with Auto Pre-charge(BL8, on the Fly)	WRAS8	H	H	L	H	H	L	L	BG	BA	V	H	V	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	H	L	H	BG	BA	V	V	V	L	CA	
Read (BC4, on the Fly)	RDS4	H	H	L	H	H	L	H	BG	BA	V	L	V	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	H	L	H	BG	BA	V	H	V	L	CA	
Read with Auto Pre-charge(Fixed BL8 or BC4)	RDA	H	H	L	H	H	L	H	BG	BA	V	V	V	H	CA	

Function	Abbre-viation	CKE		CS	ACT	RAS/A14	CAS/A15	WE/A14	BG0-BG1	BA0-BA1	C2-C0	A12/BC	A17, A13, A11	A10/AP	A0-A9	NOTE
		Previous Cycle	Current Cycle													
Read with Auto Pre-charge(BC4, on the Fly)	RDAS4	H	H	L	H	H	L	H	BG	BA	V	L	V	H	CA	
Read with Auto Pre-charge(BL8, on the Fly)	RDAS8	H	H	L	H	H	L	H	BG	BA	V	H	V	H	CA	
No Operation	NOP	H	H	L	H	H	H	H	V	V	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	X	X	X	
Power Down Entry	PDE	H	L	H	X	X	X	X	X	X	X	X	X	X	X	6
Power Down Exit	PDX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	6
ZQ calibration Long	ZQCL	H	H	L	H	H	H	L	V	V	V	V	V	H	V	
ZQ calibration Short	ZQCS	H	H	L	H	H	H	L	V	V	V	V	V	L	V	

NOTE 1 All DDR4 SDRAM commands are defined by states of $\overline{CS}$, $\overline{ACT}$, $\overline{RAS}$/A16, $\overline{CAS}$/A15, $\overline{WE}$/A14 and CKE at the rising edge of the clock. The MSB of BG, BA, RA and CA are device density and conuration dependant. When $\overline{ACT}$ = H; pins $\overline{RAS}$/A16, $\overline{CAS}$/A15, and $\overline{WE}$/A14 are used as command pins $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ respectively. When $\overline{ACT}$= L; pins $\overline{RAS}$/A16, $\overline{CAS}$/A15, and $\overline{WE}$/A14 are used as address pins A16, A15, and A14 respectively.

NOTE 2 $\overline{RESET}$ is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.

NOTE 3 Bank Group addresses (BG) and Bank addresses (BA) determine which bank within a bank group to be operated upon. For MRS commands the BG and BA selects the specific Mode Register location.

NOTE 4 “V” means “H or L (but a defined logic level)” and “X” means either “defined or undefined (like floating) logic level”.

NOTE 5 Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-Fly BL will be defined by MRS.

NOTE 6 The Power Down Mode does not perform any refresh operation.

NOTE 7 The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.

NOTE 8 Controller guarantees self refresh exit to be synchronous.

NOTE 9 VPP and VREF(VREFCA) must be maintained during Self Refresh operation.

NOTE 10 The No Operation command should be used in cases when the DDR4 SDRAM is in Gear Down Mode and Max Power Saving Mode Exit.

NOTE 11 Refer to the CKE Truth Table for more detail with CKE transition.

NOTE 12 During a MRS command A17 is Reserved for Future Use and is device density and configuration dependent.

CKE Truth Table

Current State[2]	CKE		Command (N)[3]	Action (N)[3]	NOTE
	Previous Cycle[1](N-1)	Current Cycle[1](N)	RAS, CAS, WE, CS		
Power Down	L	L	X	Maintain Power-Down	14,15
	L	H	DESELECT	Power Down Exit	11,14
Self Refresh	L	L	X	Maintain Self Refresh	15,16
	L	H	DESELECT	Self Refresh Exit	8,12,16
Bank(s) Active	H	L	DESELECT	Active Power Down Entry	11, 13, 14
Reading	H	L	DESELECT	Power Down Entry	11, 13, 14, 17
Writing	H	L	DESELECT	Power Down Entry	11, 13, 14, 17
Precharging	H	L	DESELECT	Power Down Entry	11, 13, 14, 17
Refreshing	H	L	DESELECT	Precharge Power Down Entry	11
All Banks Idle	H	L	DESELECT	Precharge Power Down Entry	11,13, 14, 18
	H	L	DESELECT	Self Refresh Entry	9,13,18
For more details with all signals See “Command Truth Table”.					10

NOTE 1 CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.
NOTE 2 Current state is defined as the state of the DDR4 SDRAM immediately prior to clock edge N.

NOTE 3 COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N),ODT is not included here.

NOTE 4 All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.

NOTE 5 The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.

NOTE 6 During any CKE transition (registration of CKE H->L or CKE L->H), the CKE level must be maintained until 1nCK prior to tCKEmin being satisfied (at which time CKE may transition again).

NOTE 7 DESELECT and NOP are defined in the Command Truth Table.

NOTE 8 On Self-Refresh Exit DESELECT commands must be issued on every clock edge occurring during the tXS period. Read or ODT commands may be issued only after tXSDLL is satisfied.

NOTE 9 Self-Refresh mode can only be entered from the All Banks Idle state.

NOTE 10 Must be a legal command as defined in the Command Truth Table.

NOTE 11 Valid commands for Power-Down Entry and Exit are DESELECT only.

NOTE 12 Valid commands for Self-Refresh Exit are DESELECT only except for Gear Down mode and Max Power Saving exit. NOP is allowed for these 2 modes.

NOTE 13 Self-Refresh can not be entered during Read or Write operations. For a detailed list of restrictions, see “Self-Refresh Operation” and “Power-Down Modes”.

NOTE 14 The Power-Down does not perform any refresh operations.

NOTE 15 “X” means “don’t care” (including floating around VREF) in Self-Refresh and Power-Down. It also applies to Address pins.

NOTE 16 VPP and VREF(VREFCA) must be maintained during Self-Refresh operation.

NOTE 17 If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power-

Down is entered, otherwise Active Power-Down is entered.

NOTE 18 'Idle state' is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, etc.) as well as all Self-Refresh exit and Power-Down Exit parameters are satisfied (tXS, tXP,etc).

NOP Command

The NO OPERATION (NOP) command was originally used to instruct the selected DDR4 SDRAM to perform a NOP ($\overline{CS}$ = LOW and $\overline{AST}$, $\overline{RAS}$/A16, $\overline{CAS}$/A15, and $\overline{WE}$/A14 = HIGH). This prevented unwanted commands from being registered during idle or wait states. The NOP command general support has been removed and should not be used unless specifically allowed; which is when exiting Max Power Saving Mode or when entering Gear-down Mode.

DESELECT Command

The DESELECT function ($\overline{CS}$ HIGH) prevents new commands from being executed by the DDR4 SDRAM. The DDR4 SDRAM is effectively deselected. Operations already in progress are not affected.

DLL on/off switching procedure

DDR4 SDRAM DLL-off mode is entered by setting MR1 bit A0 to “0”; this will disable the DLL for subsequent operations until A0 bit is set back to “1”.

DLL on to DLL off Procedure

To switch from DLL on to DLL off requires the frequency to be changed during Self-Refresh, as outlined in the following procedure:

1. Starting from Idle state (All banks pre-charged, all timings fulfilled, and DRAMs On-die Terminationresistors, RTT_NOM, must be in high impedance state before MRS to MR1 to disable the DLL.)

2. Set MR1 bit A0 to “0” to disable the DLL.

3. Wait tMOD.

4. Enter Self Refresh Mode; wait until (tCKSRE) is satisfied.

5. Change frequency, in guidance with “Input clock frequency change”.

6. Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs.

7. Starting with the Self Refresh Exit command, CKE must continuously be registered HIGH until alltMOD timings from any MRS command are satisfied. In addition, if any ODT features were enabled inthe mode registers when Self Refresh mode was entered, the ODT signal must continuously be registered LOW until all tMOD timings from any MRS command are satisfied. If RTT_NOM features were disabled in the mode registers when Self Refresh mode was entered, ODT signal is Don’t Care.

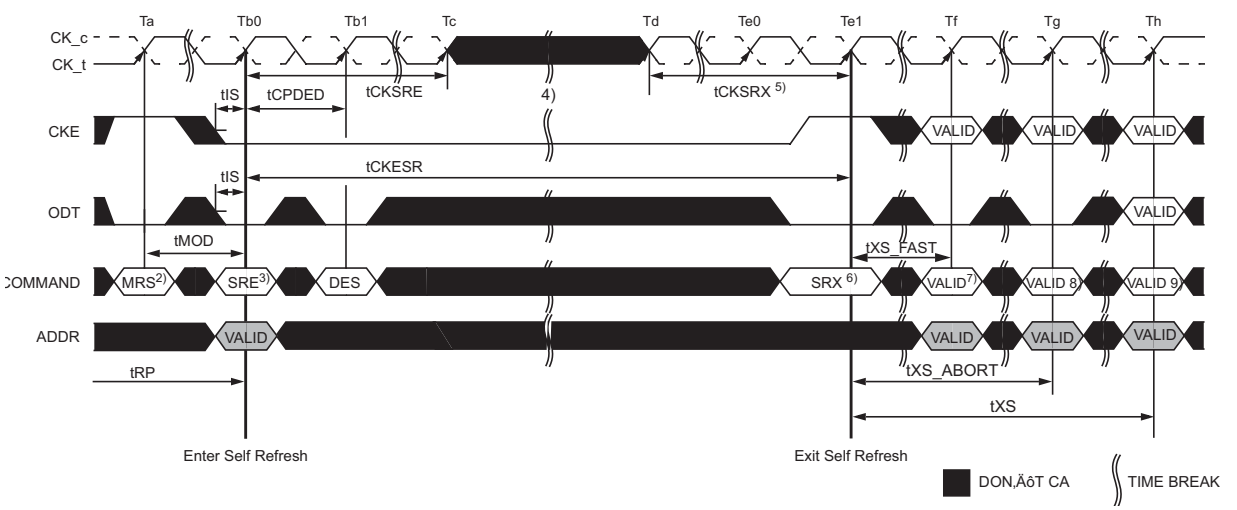
8. Wait tXS_Fast or tXS_Abort or tXS, then set Mode Registers with appropriate values (especially an update of CL, CWL and WR may be necessary. A ZQCL command may also be issued after tXS_Fast).

- tXS - ACT, PRE, PREA, REF, SRE, PDE, WR, WRS4, WRS8, WRA, WRAS4, WRAS8, RD, RDS4, RDS8, RDA, RDAS4, RDAS8

- tXS_Fast - ZQCL, ZQCS, MRS commands. For MRS command, only DRAM CL and WR/RTP register in MR0, CWL register in MR2 and geardown mode in MR3 are allowed to be accessed provided DRAM is not in per DRAM addressibility mode. Access to other DRAM mode registers must satisfy tXS timing.

- tXS_Abort - If the MR4 bit A9 is enabled then the DRAM aborts any ongoing refresh and does not increment the refresh counter. The controller can issue a valid command after a delay of tXS_abort. Upon exit from Self-Refresh, the DDR4 SDRAM requires a minimum of one extra refresh command before it is put back into Self-Refresh Mode. This requirement remains the same irrespective of the setting of the MRS bit for self refresh abort.

9. Wait for tMOD, then DRAM is ready for next command.



NOTE 1 Starting in the idle state. RTT in stable state.

NOTE 2 Disable DLL by setting MR1 bit A0 to 0.

NOTE 3 Enter SR.

NOTE 4 Change frequency.

NOTE 5 Clock must be stable tCKSRX.

NOTE 6 Exit SR.

NOTE 7,8,9 Update mode registers allowed with DLL_off settings met.

DLL off to DLL on Procedure

To switch from DLL off to DLL on (with required frequency change) during Self-Refresh:

1. Starting from Idle state (All banks pre-charged, all timings fulfilled and DRAMs On-die Termination resistors (RTT_NOM) must be in high impedance state before Self-Refresh mode is entered.)

2. Enter Self Refresh Mode, wait until tCKSRE satisfied.

3. Change frequency, in guidance with "Input clock frequency change".

4. Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs.

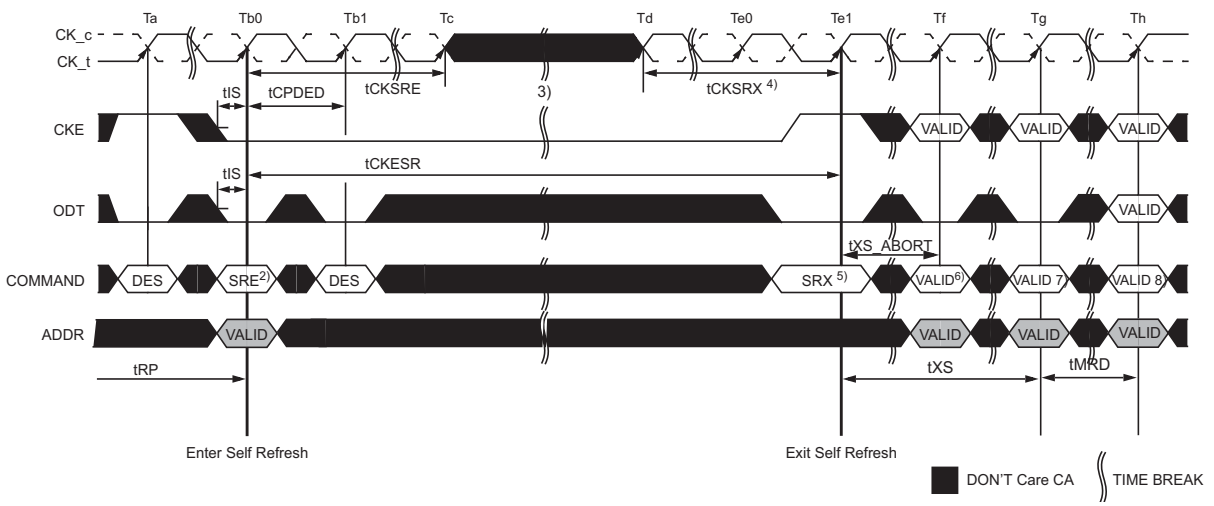
5. Starting with the Self Refresh Exit command, CKE must continuously be registered HIGH until tDLLK timing from subsequent DLL Reset command is satisfied. In addition, if any ODT features were enabled in the mode registers when Self Refresh mode was entered, the ODT signal must continuously be registered LOW until tDLLK timings from subsequent DLL Reset command is satisfied. If RTT_NOM were disabled in the mode registers when Self Refresh mode was entered, ODT signal is Don't care.

6. Wait tXS or tXS_ABORT depending on Bit A9 in MR4, then set MR1 bit A0 to "1" to enable the DLL.

7. Wait tMRD, then set MR0 bit A8 to "1" to start DLL Reset.

8. Wait tMRD, then set Mode Registers with appropriate values (especially an update of CL, CWL and WR may be necessary. After tMOD satisfied from any proceeding MRS command, a ZQCL command may also be issued during or after tDLLK.)

9. Wait for tMOD, then DRAM is ready for next command (Remember to wait tDLLK after DLL Reset before applying command requiring a locked DLL!). In addition, wait also for tZQoper in case a ZQCL command was issued.



NOTE 1 Starting in the idle state.

NOTE 2 Enter SR.

NOTE 3 Change frequency.

NOTE 4 Clock must be stable tCKSRX.

NOTE 5 Exit SR.

NOTE 6,7 Set DLL to on by setting MR1 ro A0 = 1.

NOTE 8 Start DLLReset.

NOTE 9 Update rest MR register values after tDLLK (not shown in the diagram).

NOTE 10 Ready for valid command after tDLLK (not shown in the diagram).

DLL-off Mode

DDR4 SDRAM DLL-off mode is entered by setting MR1 bit A0 to “0”; this will disable the DLL for subsequent operations until A0 bit is set back to “1”. The MR1 A0 bit for DLL control can be switched either during initialization or later. Refer to “Input clock frequency change”.

The DLL-off Mode operations listed below are an optional feature for DDR4 SDRAM. The maximum clock frequency for DLL-off Mode is specified by the parameter tCKDLL_OFF. There is no minimum frequency limit besides the need to satisfy the refresh interval, tREFI.

Due to latency counter and timing restrictions, only one value of CAS Latency (CL) in MR0 and CAS Write Latency (CWL) in MR2 are supported. The DLL-off mode is only required to support setting of both CL=10 and CWL=9. When DLL-off Mode is enabled, use of CA Parity Mode is not allowed.

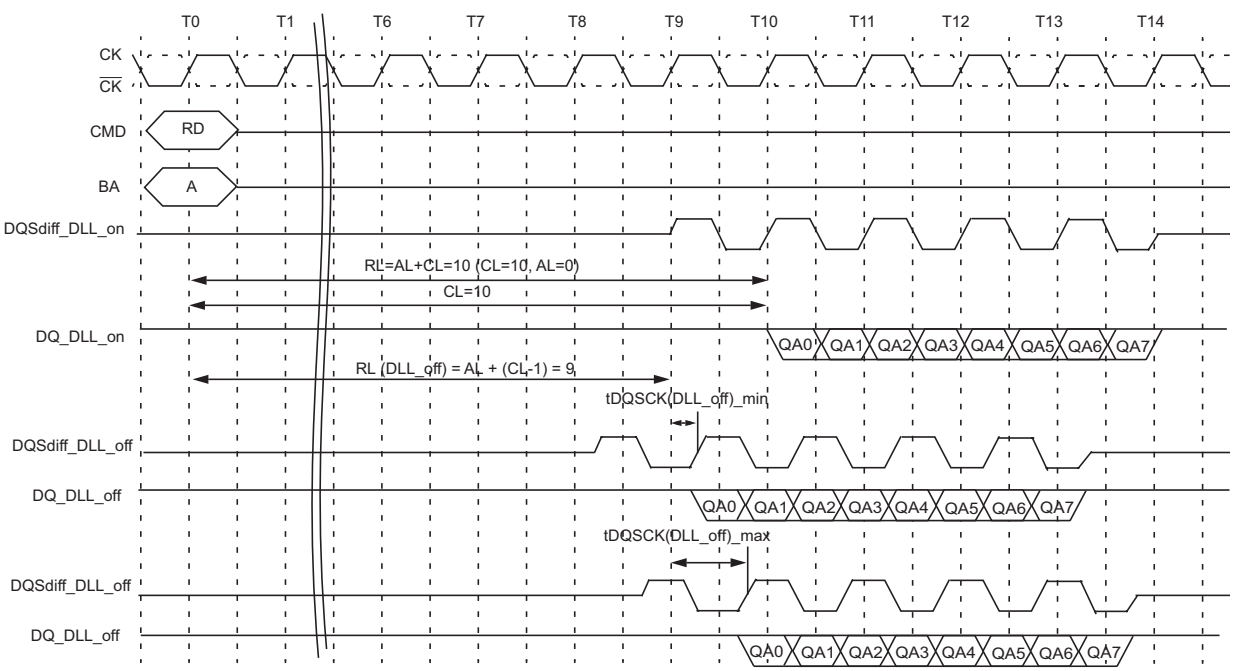
DLL-off mode will affect the Read data Clock to Data Strobe relationship (tDQSCK), but not the Data Strobe to Data relationship (tDQSQ, tQH). Special attention is needed to line up Read data to controller time domain.

Comparing with DLL-on mode, where tDQSCK starts from the rising clock edge (AL+CL) cycles after the Read command, the DLL-off mode tDQSCK starts (AL+CL - 1) cycles after the read command.

Another difference is that tDQSCK may not be small compared to tCK (it might even be larger than tCK) and the difference between tDQSCKmin and tDQSCKmax is significantly larger than in DLL-on mode.

tDQSCK(DLL_off) values are vendor specific.

The timing relations on DLL-off mode READ operation are shown in the following Timing Diagram(CL=10, BL=8, PL=0):



Input Clock Frequency Change

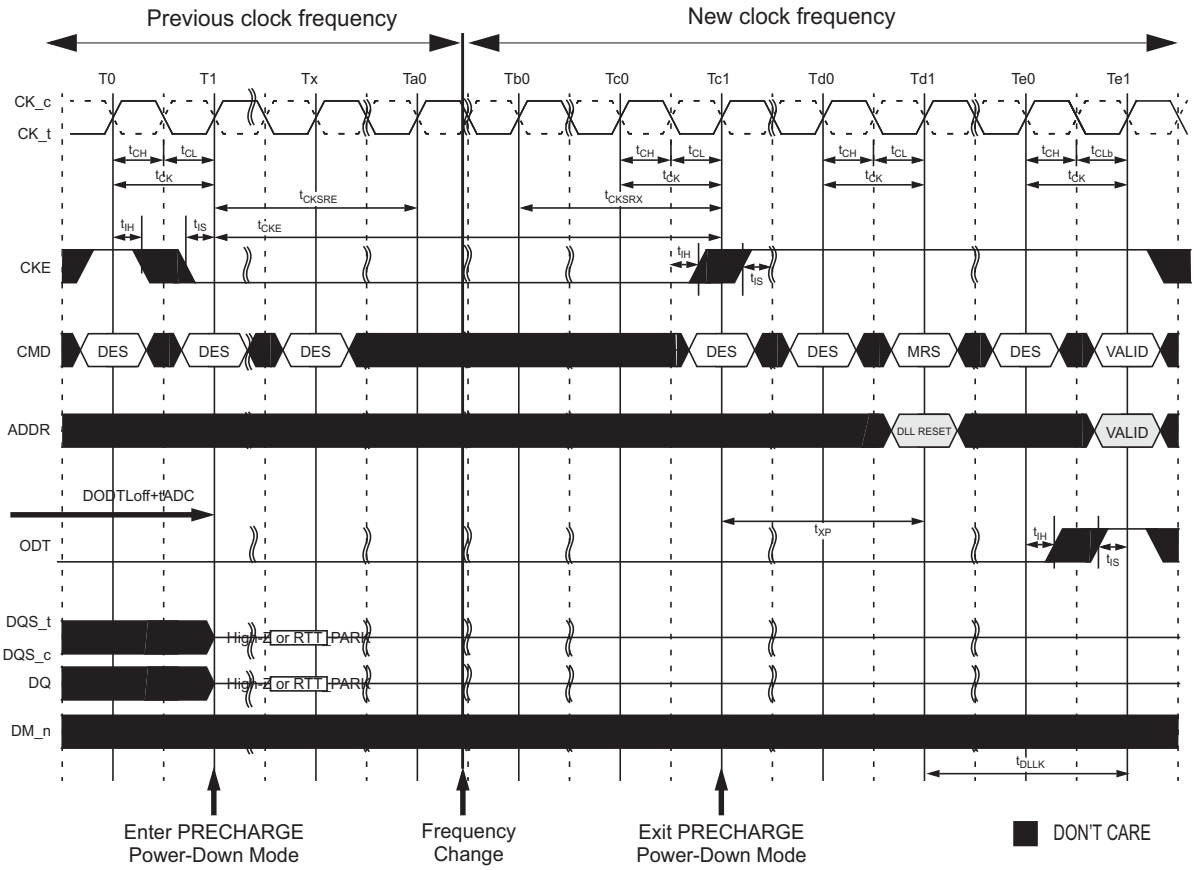
Once the DDR4 SDRAM is initialized, the DDR4 SDRAM requires the clock to be “stable” during almost all states of normal operation. This means that, once the clock frequency has been set and is to be in the °ßstable state°®, the clock period is not allowed to deviate except for what is allowed for by the clock jitter and SSC (spread spectrum clocking) specifications.

The input clock frequency can be changed from one stable clock rate to another stable clock rate under two conditions: (1) Self-Refresh mode and (2) Precharge Power-down mode. Outside of these two modes, it is illegal to change the clock frequency.For the first condition, once the DDR4 SDRAM has been successfully placed in to Self-Refresh mode and tCKSRE has been satisfied, the state of the clock becomes a don’t care. Once a don’t care, changing the clock frequency is permissible, provided the new clock frequency is stable prior to tCKSRX. When entering and exiting Self-Refresh mode for the sole purpose of changing the clock frequency, the Self-Refresh entry and exit specifications must still be met as outlined in “Self-Refresh Operation”.However, because DDR4 DLL lock time ranges from 597nCK at 1333MT/s to 1024nCK at 3200MT/s, additional MRS commands need to be issued for the new clock frequency. If DLL is enabled, tDLLK must be programmed according to the value defined in AC parameter tables, and the DLL must be RESET by an explicit MRS command (MR0 bit A8=’1’b) when the input clock frequency is different before and after self refresh.The DDR4 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade. Any frequency change below the minimum operating frequency would require the use of DLL_on- mode -> DLL_off -mode transition sequence, refer to “DLL on/off switching procedure”.

The second condition is when the DDR4 SDRAM is in Precharge Power-down mode. If the RTT_NOM feature was enabled in the mode register prior to entering Precharge power down mode, the ODT signal must continuously be registered LOW during this sequence until DLL re-lock to complete.

If the RTT_NOM feature was disabled in the mode register prior to entering Precharge power down mode, ODT signal is allowed to be floating and DRAM does not provide RTT_NOM termination. A minimum of tCKSRE must occur after CKE goes LOW before the clock frequency may change.

The DDR4 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade. During the input clock frequency change, CKE must be held at stable LOW levels. Once the input clock frequency is changed, stable new clocks must be provided to the DRAM tCKSRX before Precharge Power-down may be exited; after Precharge Power-down is exited and tXP has expired, tDLLK MRS command followed by DLL reset must be issued. Depending on the new clock frequency, additional MRS commands may need to be issued to appropriately set the WR/RTP, CL, and CWL with CKE continuously registered high. During DLL re-lock period, CKE must remain HIGH. After the DLL lock time, the DRAM is ready to operate with new clock frequency.



NOTE 1 tCKSRE and tCKSRX are Self-Refresh mode specifications but the value they represent are applicable here.

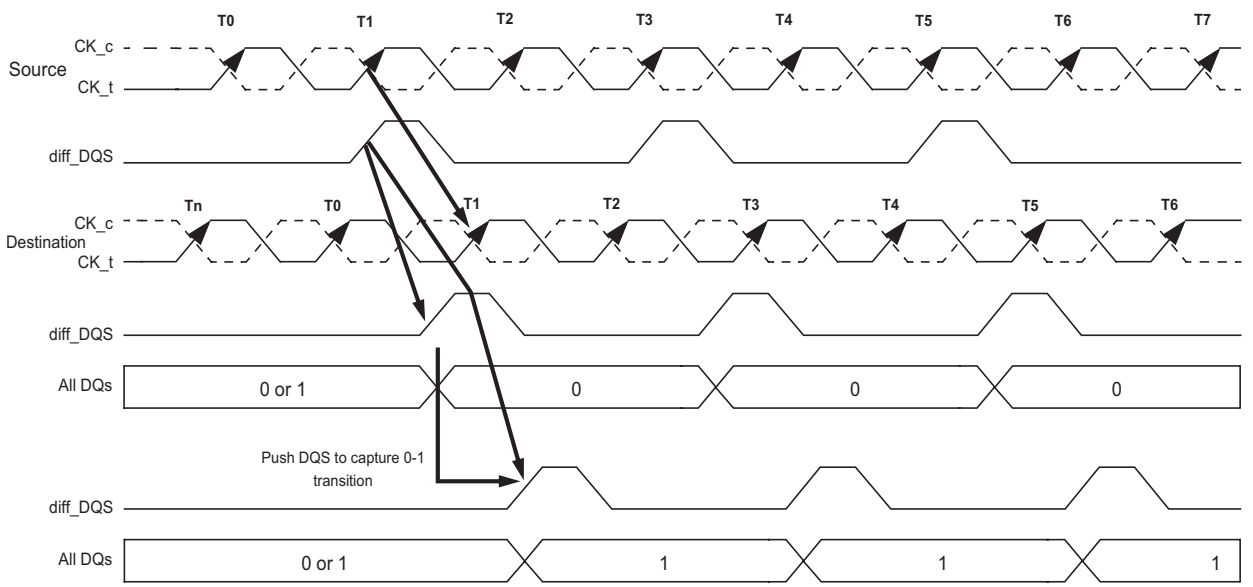
NOTE 2 If the RTT_NOM feature was enabled in the mode register prior to entering Precharge power down mode, the ODT signal must continuously be registered LOW ensuring RTT is in an off state. If the RTT_NOM feature was disabled in the mode register prior to entering Precharge power down mode or DRAM ODT input deactivation is enabled, RTT will remain in the off state. The ODT signal can be registered either LOW or HIGH in this case.

NOTE 3 If RTT_PARK is disabled and ODT input buffer is not deactivated.

Write Leveling

For better signal integrity, the DDR4 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has benefits from reducing number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the DDR4 SDRAM supports a 'write leveling' feature to allow the controller to compensate for skew. This feature may not be required under some system conditions provided the host can maintain the tDQSS, tDSS and tDSH specifications.

The memory controller can use the 'write leveling' feature and feedback from the DDR4 SDRAM to adjust the DQS - $\overline{\text{DQS}}$ to CK - $\overline{\text{CK}}$ relationship. The memory controller involved in the leveling must have adjustable delay setting on DQS - $\overline{\text{DQS}}$ to align the rising edge of DQS - $\overline{\text{DQS}}$ with that of the clock at the DRAM pin. The DRAM asynchronously feeds back CK - $\overline{\text{CK}}$, sampled with the rising edge of DQS - $\overline{\text{DQS}}$, through the DQ bus. The controller repeatedly delays DQS - $\overline{\text{DQS}}$ until a transition from 0 to 1 is detected. The DQS - $\overline{\text{DQS}}$ delay established through this exercise would ensure tDQSS specification. Besides tDQSS, tDSS and tDSH specification also needs to be fulfilled. One way to achieve this is to combine the actual tDQSS in the application with an appropriate duty cycle and jitter on the DQS - $\overline{\text{DQS}}$ signals. Depending on the actual tDQSS in the application, the actual values for tDQSL and tDQSH may have to be better than the absolute limits provided in the chapter "AC Timing Parameters" in order to satisfy tDSS and tDSH specification. A conceptual timing of this scheme is shown below.



DQS - $\overline{\text{DQS}}$ driven by the controller during leveling mode must be terminated by the DRAM based on ranks populated. Similarly, the DQ bus driven by the DRAM must also be terminated at the controller.

All data bits should carry the leveling feedback to the controller across the DRAM configurations X4, X8, and X16. On a X16 device, both byte lanes should be leveled independently. Therefore, a separate feedback mechanism should be available for each byte lane. The upper data bits should provide the feedback of the upper diff_DQS(diff_UDQS) to clock relationship whereas the lower data bits would indicate the lower diff_DQS(diff_LDQS) to clock relationship.

RAM setting for write leveling & DRAM termination function in that mode

DRAM enters into Write leveling mode if A7 in MR1 set 'High' and after finishing leveling, DRAM exits from write leveling mode if A7 in MR1 set 'Low'. Note that in write leveling mode, only DQS/$\overline{\text{DQS}}$ terminations are activated and deactivated via ODT pin, unlike normal operation.

MR setting involved in the leveling procedure

Function	MR1	Enable	Disable
Write leveling enable	A7	1	0
Output buffer mode (Qoff)	A12	0	1

MR setting involved in the leveling procedure

ODT pin @DRAM if RTT_NOM/PARK Value is set via MRS	DQS/$\overline{DQS}$ termination	DQs termination
RTT_NOM with ODT High	On	Off
RTT_PARK with ODT LOW	On	Off

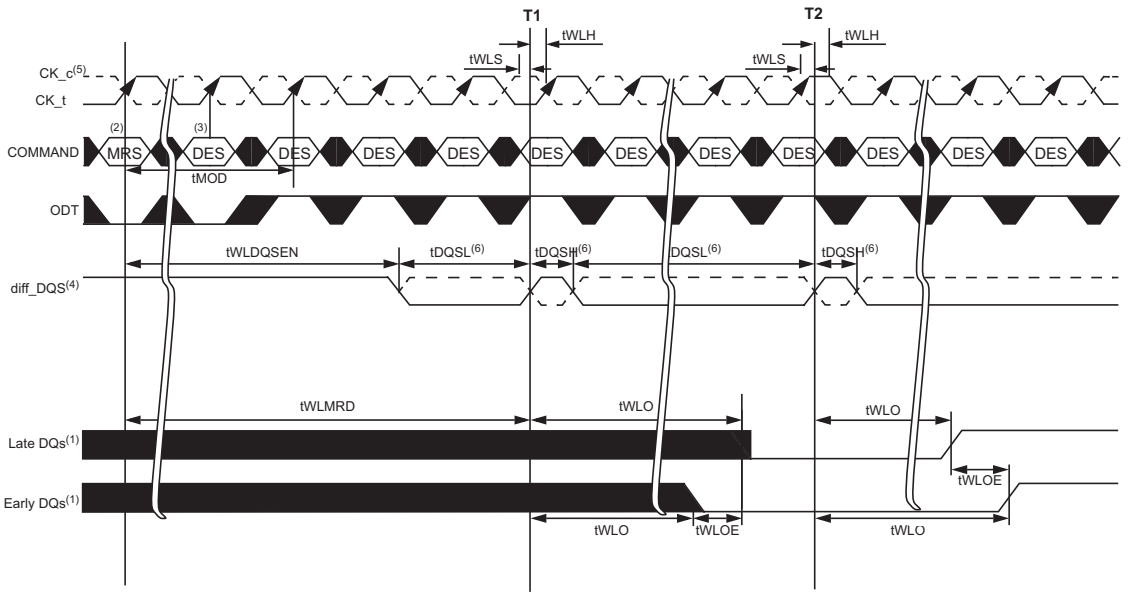
NOTE 1 In Write Leveling Mode with its output buffer disabled (MR1[bit A7] = 1 with MR1[bit A12] = 1) all RTT_NOM and RTT_PARK settings are allowed; in Write Leveling Mode with its output buffer enabled (MR1[bit A7] = 1 with MR1[bit A12] = 0) only RTT_NOM and RTT_PARK settings of TBD are allowed.

Procedure Description

The Memory controller initiates Leveling mode of all DRAMs by setting bit A7 of MR1 to 1. When entering write leveling mode, the DQ pins are in undefined driving mode. During write leveling mode, only DESELECT commands are allowed, as well as an MRS command to change Qoff bit (MR1[A12]) and an MRS command to exit write leveling (MR1[A7]). Upon exiting write leveling mode, the MRS command performing the exit (MR1[A7]=0) may also change MR1 bits of A12-A8 ,A2-A1. Since the controller levels one rank at a time, the output of other ranks must be disabled by setting MR1 bit A12 to 1. The Controller may assert ODT after tMOD, at which time the DRAM is ready to accept the ODT signal.

The Controller may drive DQS low and $\overline{DQS}$ high after a delay of tWLDQSEN, at which time the DRAM has applied on-die termination on these signals. After tDQSL and tWLMRD, the controller provides a single DQS, $\overline{DQS}$ edge which is used by the DRAM to sample CK - $\overline{CK}$ driven from controller. tWLMRD(max) timing is controller dependent.

DRAM samples CK - $\overline{CK}$ status with rising edge of DQS - $\overline{DQS}$ and provides feedback on all the DQ bits asynchronously after tWLO timing. There is a DQ output uncertainty of tWLOE defined to allow mismatch on DQ bits. The tWLOE period is defined from the transition of the earliest DQ bit to the corresponding transition of the latest DQ bit. There are no read strobes (DQS/$\overline{DQS}$) needed for these DQs. Controller samples incoming DQs and decides to increment or decrement DQS - $\overline{DQS}$ delay setting and launches the next DQS/$\overline{DQS}$ pulse after some time, which is controller dependent. Once a 0 to 1 transition is detected, the controller locks DQS - $\overline{DQS}$ delay setting and write leveling is achieved for the device. The following figure describes the timing diagram and parameters for the overall Write Leveling procedure.



NOTE 1 DDR4 SDRAM drives leveling feedback on all DQs

NOTE 2 MRS : Load MR1 to enter write leveling mode

NOTE 3 DES : Deselect

NOTE 4 diff_DQS is the differential data strobe (DQS-$\overline{DQS}$). Timing reference points are the zero crossings. DQS is shown with solid line, $\overline{DQS}$ is shown with dotted line

NOTE 5 CK/$\overline{CK}$: CK is shown with solid dark line, where as $\overline{CK}$ is drawn with dotted line.

NOTE 6 DQS, $\overline{DQS}$ needs to fulfill minimum pulse width requirements tDQSH(min) and tDQSL(min) as defined for regular Writes; the max pulse width is system dependent

Write Leveling Mode Exit

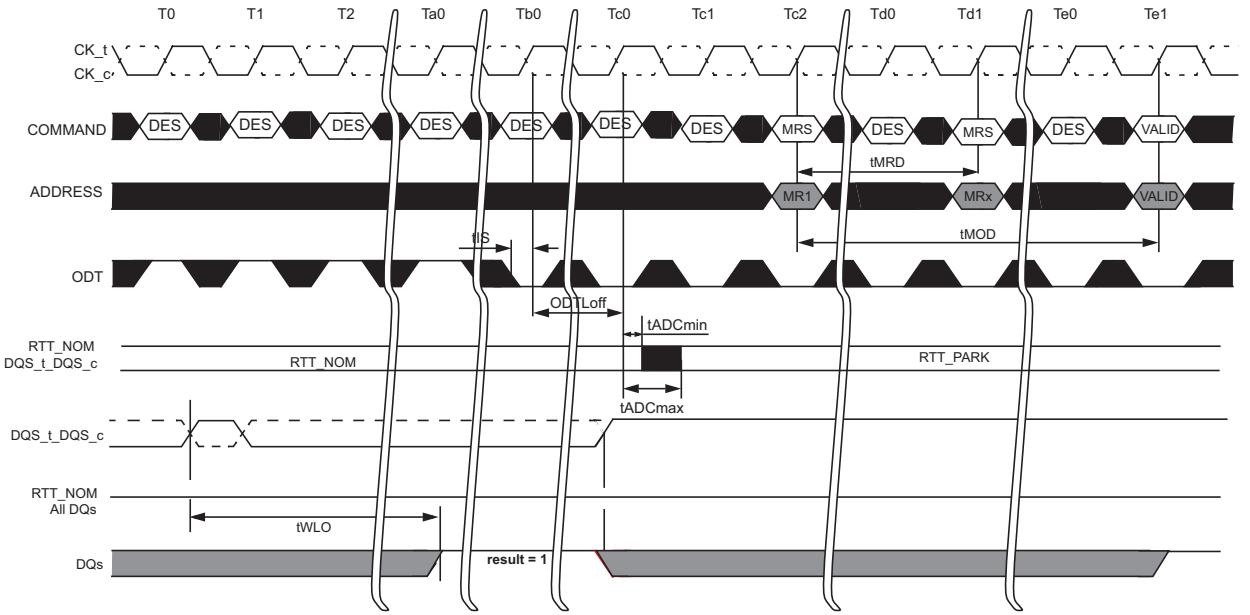
The following sequence describes how the Write Leveling Mode should be exited:

1.After the last rising strobe edge (see ~T0), stop driving the strobe signals (see ~Tc0). Note: From now on, DQ pins are in undefined driving mode, and will remain undefined, until tMOD after the respective MRS command (Te1).

2.Drive ODT pin low (tIS must be satisfied) and continue registering low. (see Tb0).

3.After the RTT is switched off, disable Write Level Mode via MRS command (see Tc2).

4.After tMOD is satisfied (Te1), any valid command may be registered. (MRS commands may be issued after tMRD (Td1)).

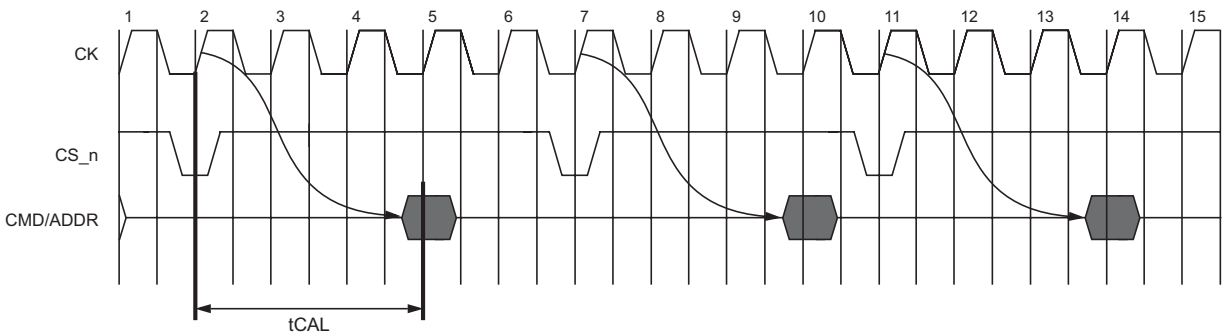

T0
T1
T2
Ta0
Tb0
Tc0
Tc1
Tc2
Td0
Td1
Te0
Te1
CK_t
CK_c
COMMAND
DES
MRS
VALID
tMRD
ADDRESS
MR1
MRx
tMOD
tIS
ODT
ODTLoff
tADCmin
RTT_NOM
DQS_t_DQS_c
RTT_PARK
tADCmax
RTT_NOM
All DQs
tWLO
DQs
result = 1

CAL Mode ($\overline{CS}$ to Command Address Latency)

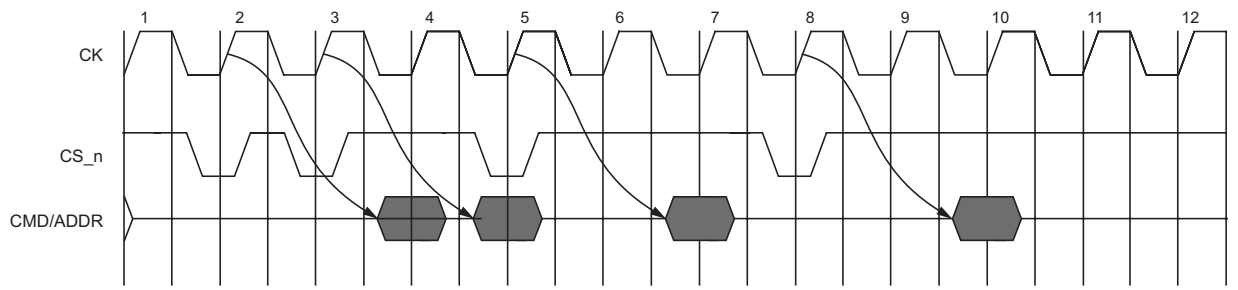
DDR4 supports Command Address Latency, CAL, function as a power savings feature. CAL is the delay in clock cycles between $\overline{CS}$ and CMD/ADDR defined by MR4[A8:A6] .

CAL gives the DRAM time to enable the CMD/ADDR receivers before a command is issued. Once the command and the address are latched, the receivers can be disabled. For consecutive commands, the DRAM will keep the receivers enabled for the duration of the command sequence.

Definition of CAL



CAL operational timing for consecutive command issues



The following tables show the timing requirements for tCAL and MRS settings at different data rates.

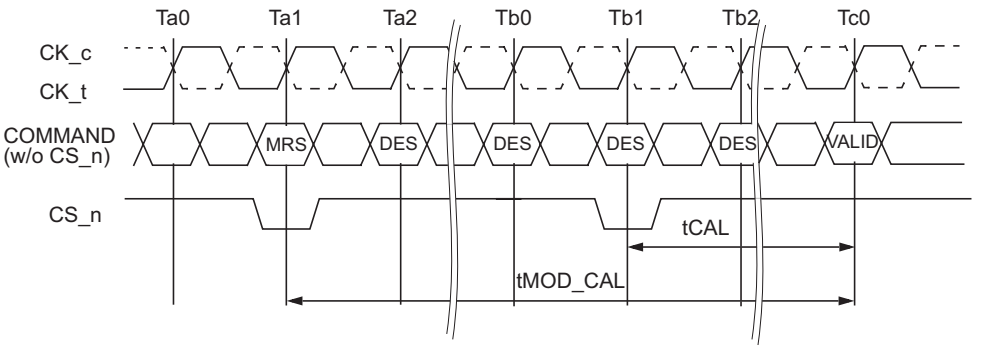
Parameter	Symbol	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	Units
$\overline{CS}$ to Command Address Latency	CAL	3	4	4	5	nCK

Parameter	Symbol	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	Units
$\overline{CS}$ to Command Address Latency (Gear down mode even CK)	CAL	4	4	4	6	nCK

MRS Timings with Command/Address Latency enabled

When Command/Address latency mode is enabled, users must allow more time for MRS commands to take effect. When CAL modeis enabled, or being enabled by an MRS command, the earliest the next valid command can be issued is tMOD_CAL, wheretMOD_CAL=tMOD+tCAL.

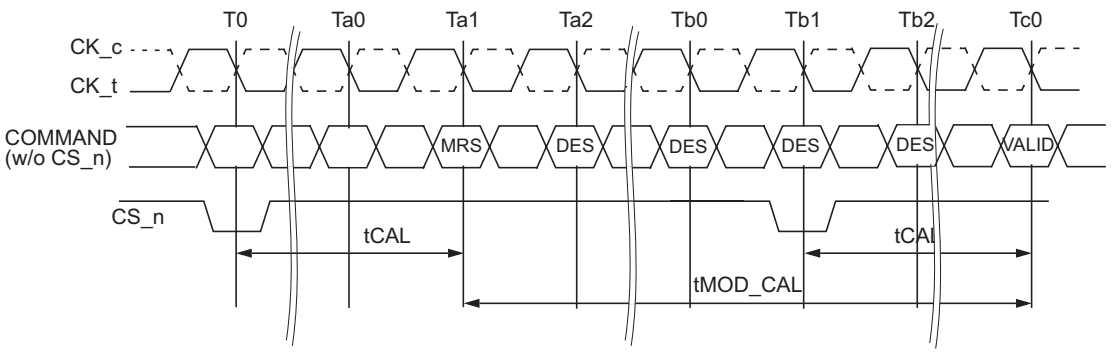
CAL enable timing - tMOD_CAL



NOTE 1 MRS command at Ta1 enables CAL mode

NOTE 2 tMOD_CAL=tMOD+tCAL

tMOD_CAL, MRS to valid command timing with CAL enabled

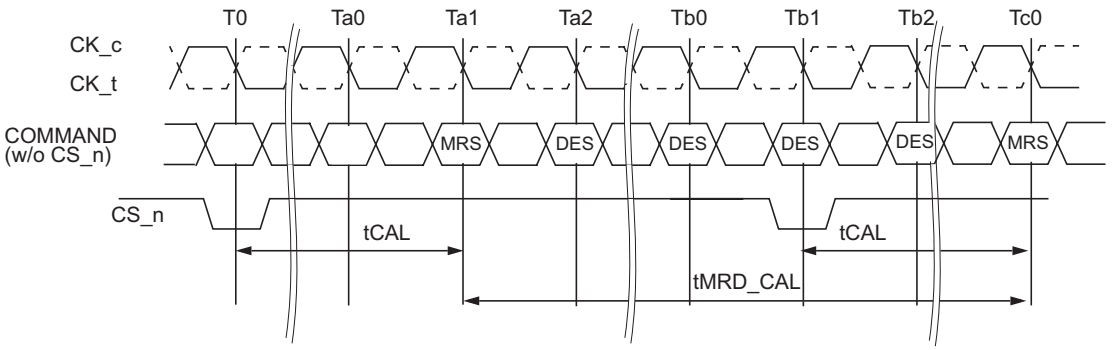


NOTE 1 MRS at Ta1 may or may not modify CAL, tMOD_CAL is computed based on new tCAL setting.

NOTE 2 tMOD_CAL=tMOD+tCAL.

When Command/Address latency is enabled or being entered, users must wait tMRD_CAL until the next MRS command can be issued. tMRD_CAL=tMOD+tCAL.

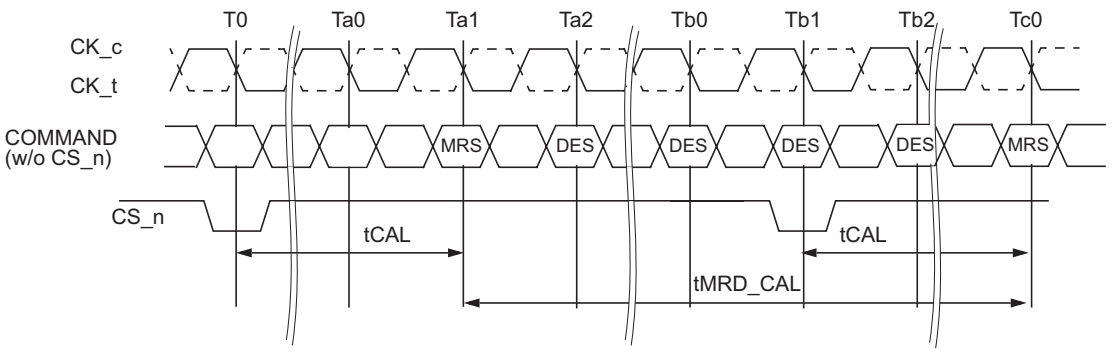
CAL enabling MRS to next MRS command, tMRD_CAL



NOTE 1 MRS command at Ta1 enables CAL mode.

NOTE 2 tMOD_CAL=tMOD+tCAL.

tMRD_CAL, mode register cycle time with CAL enabled



NOTE 1 MRS at Ta1 may or may not modify CAL, tMRD_CAL is computed based on new tCAL setting.

NOTE 2 tMOD_CAL=tMOD+tCAL.

Multi Purpose Register

DQ Training with MPR

The DDR4 DRAM contains four 8bit programmable MPR registers used for DQ bit pattern storage. These registers once programmed are activated with MRS read commands to drive the MPR bits on to the DQ bus during link training.

And DDR4 SDRAM only supports following command, MRS, RD, RDA WR, WRA, DES, REF and Reset during MPR enable Mode: MR3 [A2 = 1].

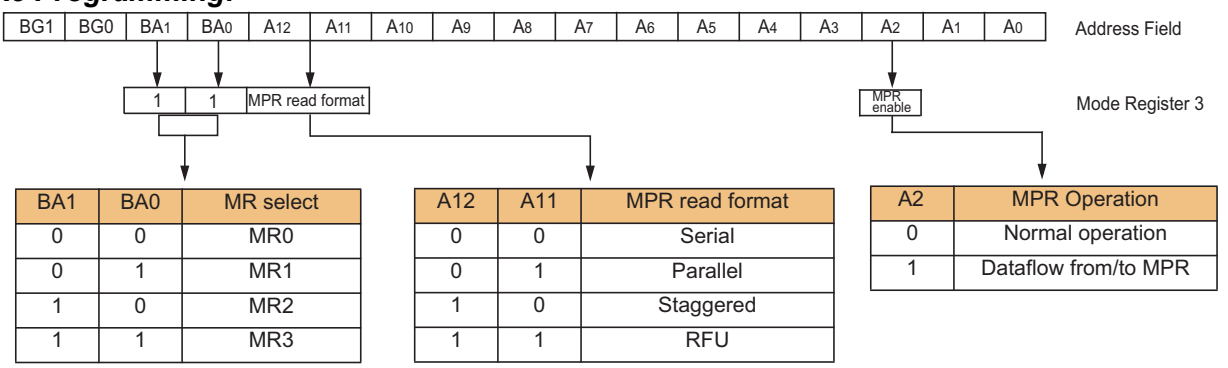
Note that in MPR mode RDA/WRA has the same functionality as a READ/WRITE command which means the auto pre-charge part of RDA/WRA is ignored. Power-Down mode and Self-Refresh command also is not allowed during MPR enable Mode. No other command can be issued within tRFC after REF command and 1x Refresh is only allowed when MPR mode is Enable. During MPR operations, MPR read or write sequence must be complete prior to a refresh com-mand.

MR3 definition

Mode register MR3 controls the Multi-Purpose Registers (MPR) used for training. MR3 is written by asserting $\overline{CS}$, $\overline{RAS}$/A16,$\overline{CAS}$/A15 and $\overline{WE}$/A14 low, $\overline{ACT}$, BA0 and BA1 high and BG1[1] and BG0 low while controlling the states of the address pinsaccording to the table below.

NOTE 1. x4/x8 only

MR3 Programming:



BA1	BA0	MR select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

A12	A11	MPR read format
0	0	Serial
0	1	Parallel
1	0	Staggered
1	1	RFU

A2	MPR Operation
0	Normal operation
1	Dataflow from/to MPR

Read or Write with MPR LOCATION :

BA1	BA0	MPR Location
0	0	MPR location 0
0	1	MPR location 1
1	0	MPR location 2
1	1	MPR location 3

Default value for MPR0 = 01010101
Default value for MPR1 = 00110011
Default value for MPR2 = 00001111
Default value for MPR3 = 00000000

MPR Reads

MPR reads are supported using BL8 and BC4(Fixed) modes. BC4 on the fly is not supported for MPR reads.

MPR reads using BC4:

BA1 and BA0 indicate the MPR location within the selected page in MPR Mode.

A10 and other address pins are don't care including BG1 and BG0.Read commands for BC4 are supported with starting column address of A2:A0 of '000' and '100'.

Data Bus Inversion (DBI) is not allowed during MPR Read operation.

DDR4 MPR mode is enabled by programming bit A2=1 and then reads are done from a specific MPR location.

MPR location is specified with the Read command using Bank address bits BA1 and BA0.

Each MPR location is 8 bit wide.

STEPS:

DLL must be locked prior to MPR Reads. If DLL is Enabled : MR1[A0 = 1]

Precharge all

Wait until tRP is satisfied

MRS MR3, Opcode A2=’1’b

- Redirect all subsequent read and writes to MPR locations

Wait until tMRD and tMOD satisfied.

Read command

- A[1:0] = ‘00’b (data burst order is fixed starting at nibble, always 00b here)
- A[2]= ‘0’b (For BL=8, burst order is fixed at 0,1,2,3,4,5,6,7)
  (For BC=4, burst order is fixed at 0,1,2,3,T,T,T,T)

or

- A[2]= 1 (For BL=8 : Not Support)
  (For BC=4, burst order is fixed at 4,5,6,7,T,T,T,T)
- A12/BC= 0 or 1 : Burst length supports only BL8(Fixed) and BC4(Fixed), not supports BC4(OTF).

When MR0 A[1:0] is set ‘01’, A12/BC must be always ‘1’b in MPR read commands (BL8 only).

- BA1 and BA0 indicate the MPR location
- A10 and other address pins are don’t care including BG1and BG0

After RL= AL + CL, DRAM bursts out the data from MPR location. The format of data on return is described in a later section andcontrolled by MR3 bits A0,A1, A11 and A12.

Memory controller repeats these calibration reads until read data capture at memory controller is optimized. Read MPR location canbe a different location as specified by the Read command

After end of last MPR read burst, wait until tMPRR is satisfied

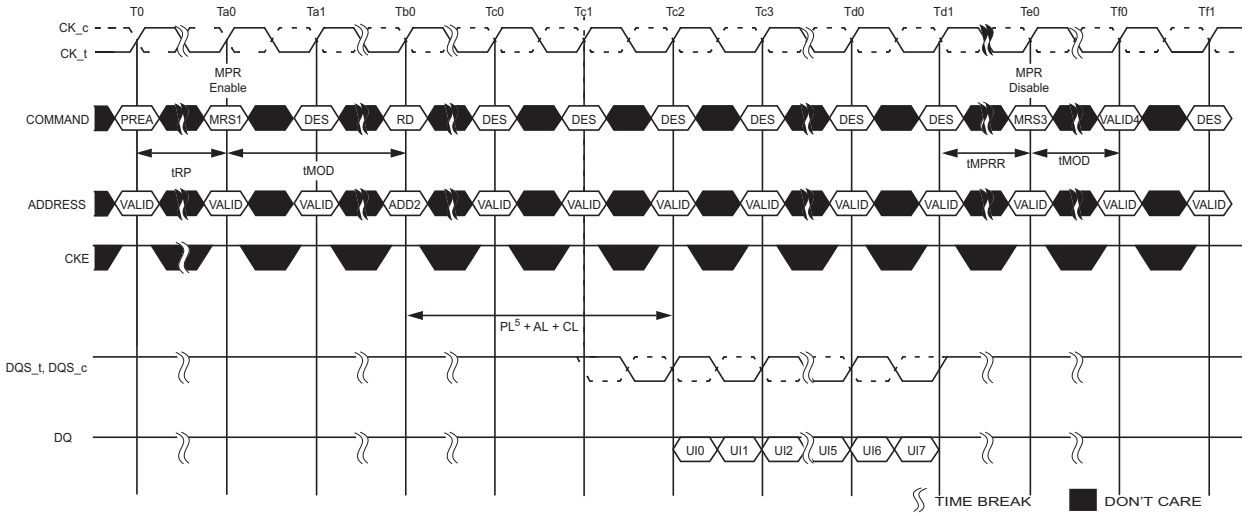
MRS MR3, Opcode A2= ‘0b’

All subsequent reads and writes from DRAM array

Wait until tMRD and tMOD are satisfied

Continue with regular DRAM commands like Activate.

MPR Read Timing



NOTE 1 Multi-Purpose Registers Read/Write Enable (MR3 A2 = 1)

NOTE 2 Address setting

- A[1:0] = ‘00’b (data burst order is fixed starting at nibble, always 00b here)

- A[2]= ‘0’b (For BL=8, burst order is fixed at 0,1,2,3,4,5,6,7)

- BA1 and BA0 indicate the MPR location

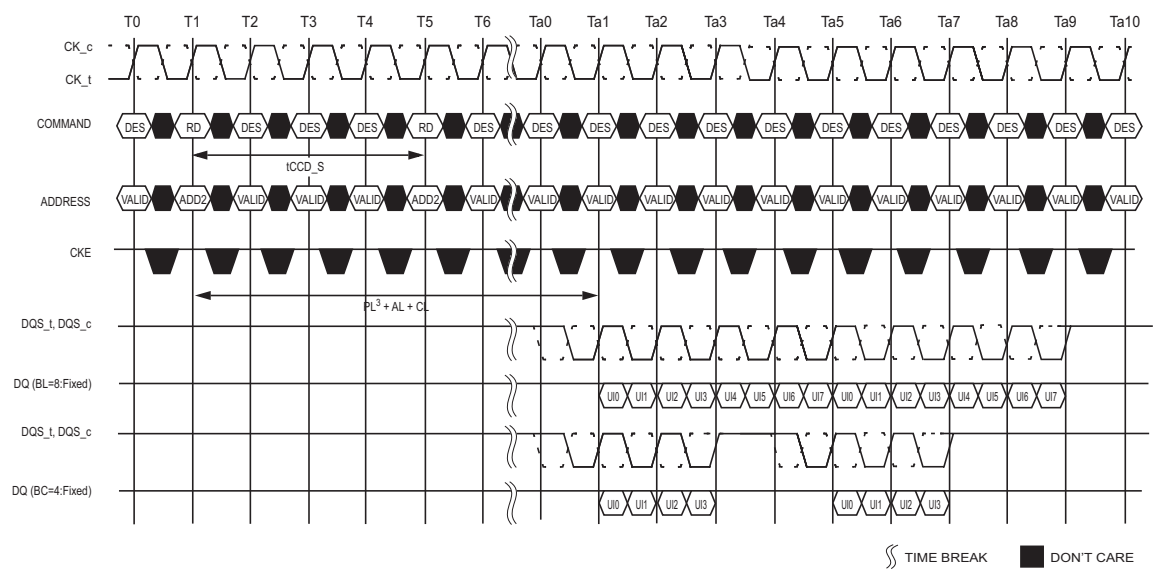
- A10 and other address pins are don’t care including BG1 and BG0. A12 is don’t care when MR0 A[1:0] = ‘00’ or ‘10’ and must be ‘1’b when MR0 A[1:0] = ‘01’

NOTE 3 Multi-Purpose Registers Read/Write Disable (MR3 A2 = 0)

NOTE 4 Continue with regular DRAM command.

NOTE 5 PL (Parity latency) is added to Data output delay when C/A parity latency mode is enabled.

MPR Back to Back Read Timing



NOTE 1 tCCD_S = 4, Read Preamble = 1tCK

NOTE 2 Address setting

- A[1:0] = ‘00’b (data burst order is fixed starting at nibble, always 00b here)

- A[2]= ‘0’b (For BL=8, burst order is fixed at 0,1,2,3,4,5,6,7)

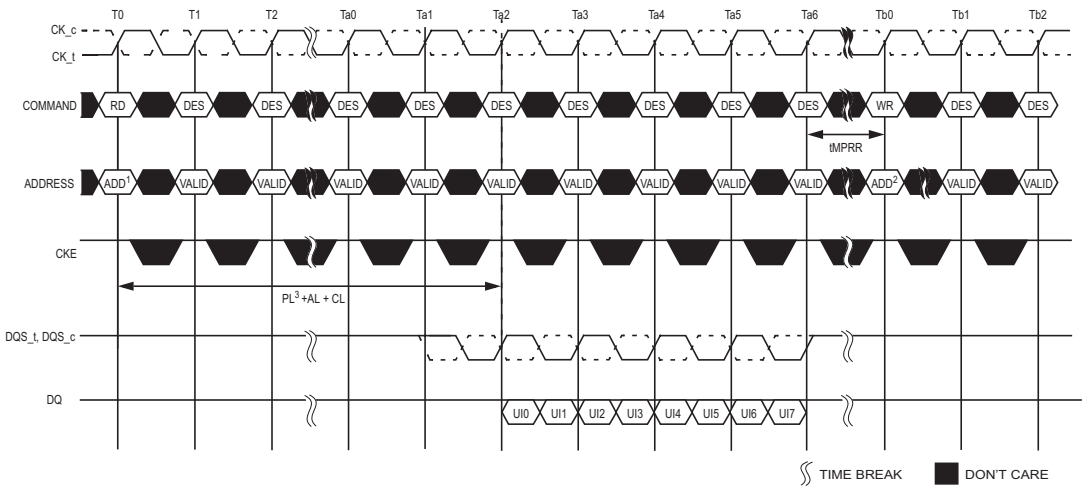
(For BC=4, burst order is fixed at 0,1,2,3,T,T,T,T)

- BA1 and BA0 indicate the MPR location

- A10 and other address pins are don’t care including BG1 and BG0. A12 is don’t care when MR0 A[1:0] = ‘00’ or ‘10’ and must be ‘1’b when MR0 A[1:0] = ‘01’

NOTE 3 PL (Parity latency) is added to Data output delay when C/A parity latency mode is enabled.

MPR Read to Write Timing



NOTE 1 Address setting

- A[1:0] = ‘00’b (data burst order is fixed starting at nibble, always 00b here)

- A[2]= ‘0’b (For BL=8, burst order is fixed at 0,1,2,3,4,5,6,7)

- BA1 and BA0 indicate the MPR location

- A10 and other address pins are don’t care including BG1 and BG0. A12 is don’t care when MR0 A[1:0] = ‘00’ or ‘10’ and must be ‘1’b when MR0 A[1:0] = ‘01’

NOTE 2 Address setting

- BA1 and BA0 indicate the MPR location

- A [7:0] = data for MPR

- A10 and other address pins are don’t care

NOTE 3 PL (Parity latency) is added to Data output delay when C/A parity latency mode is enabled.

MPR Writes

DDR4 allows 8 bit writes to the MPR location using the address bus A7:A0.

UI and Address Mapping for MPR Location

MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
SDRAM Address	A7	A6	A5	A4	A3	A2	A1	A0
UI	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7

STEPS:

DLL must be locked prior to MPR Writes. If DLL is Enabled : MR1[A0 = 1]

Precharge all

Wait until tRP is satisfied

MRS MR3, Opcode A2='1'b

Redirect all subsequent read and writes to MPR locations

Wait until tMRD and tMOD satisfied.

Write command

BA1 and BA0 indicate the MPR location

A [7:0] = data for MPR

Wait until tWR_MPR satisfied, so that DRAM to complete MPR write transaction.

Memory controller repeats these calibration writes and reads until data capture at memory controller is optimized.

After end of last MPR read burst, wait until tMPRR is satisfied

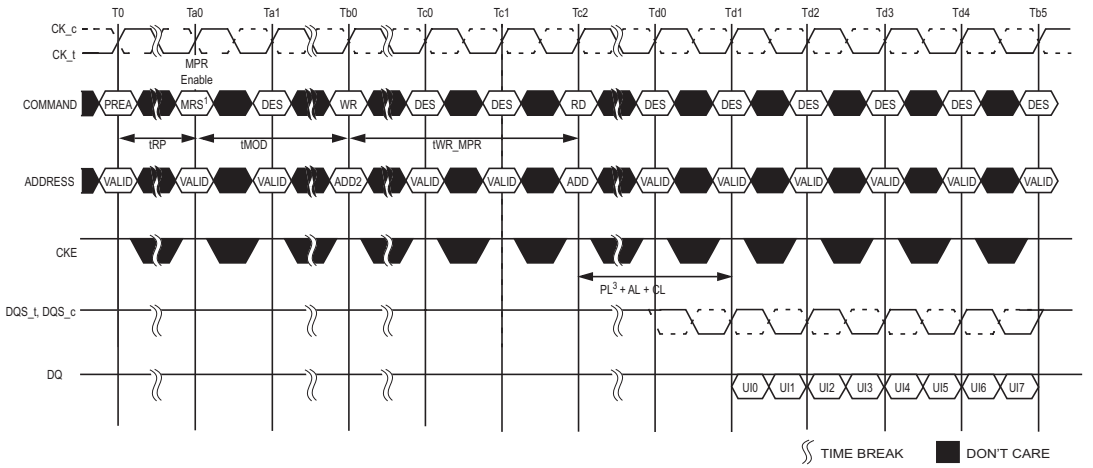
MRS MR3, Opcode A2= '0b'

All subsequent reads and writes from DRAM array

Wait until tMRD and tMOD are satisfied

Continue with regular DRAM commands like Activate.

MPR Write Timing and Write to Read Timing



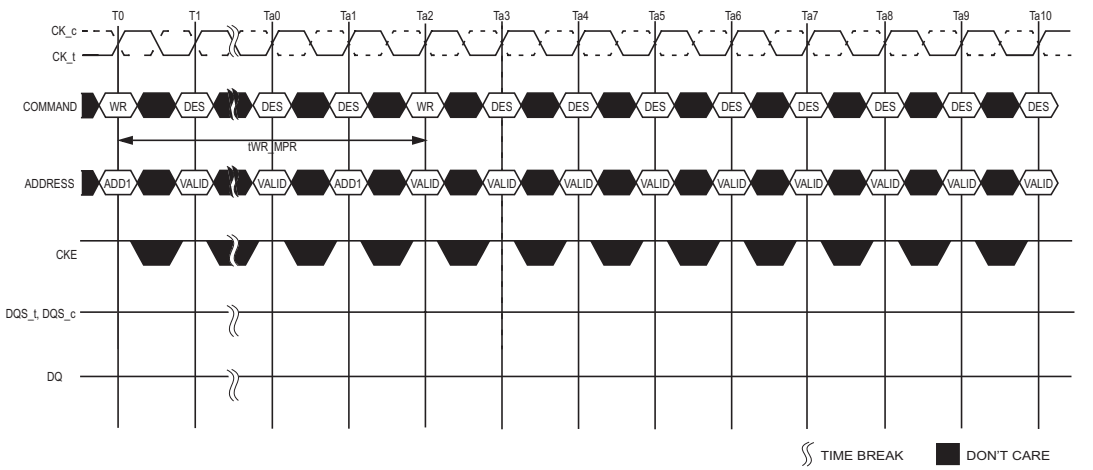
NOTE 1 Multi-Purpose Registers Read/Write Enable (MR3 A2 = 1)

NOTE 2 Address setting

- BA1 and BA0 indicate the MPR location
- A [7:0] = data for MPR
- A10 and other address pins are don't care.

NOTE 3 PL (Parity latency) is added to Data output delay when C/A parity latency mode is enabled.

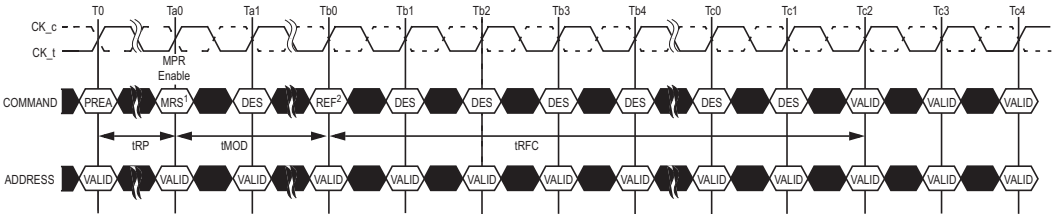
MPR Back to Back Write Timing



NOTE 1 Address setting

- BA1 and BA0 indicate the MPR location
- A [7:0] = data for MPR
- A10 and other address pins are don't care.

Refresh Command Timing

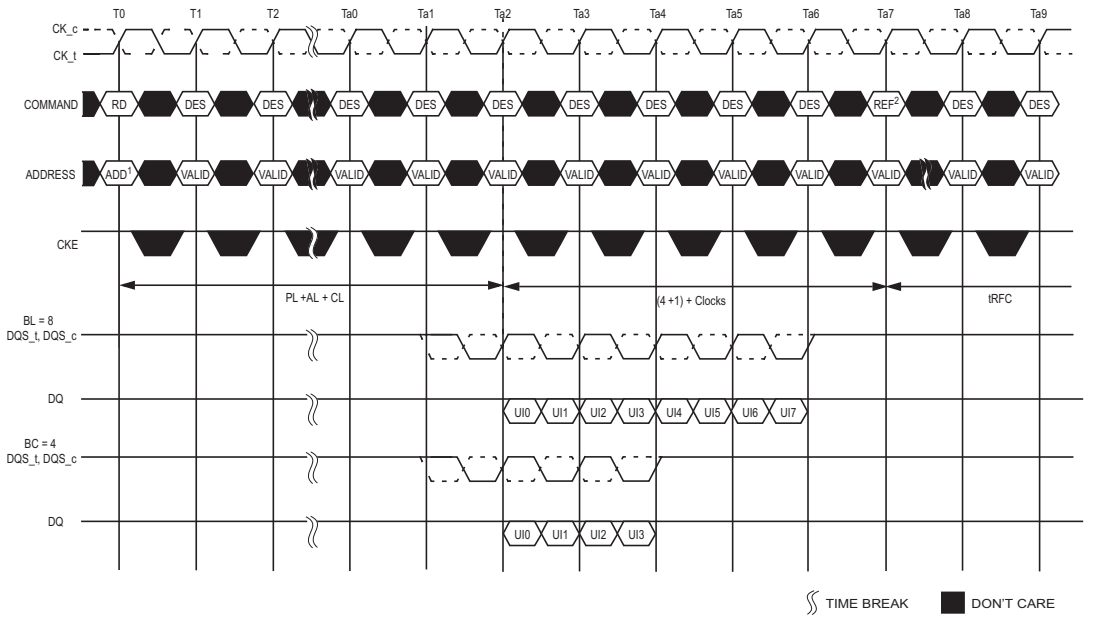


NOTE 1 Multi-Purpose Registers Read/Write Enable (MR3 A2 = 1)

- Redirect all subsequent read and writes to MPR locations

NOTE 2 1x Refresh is only allowed when MPR mode is Enable.

Read to Refresh Command Timing



NOTE 1 Address setting

- A[1:0] = ‘00’b (data burst order is fixed starting at nibble, always 00b here)

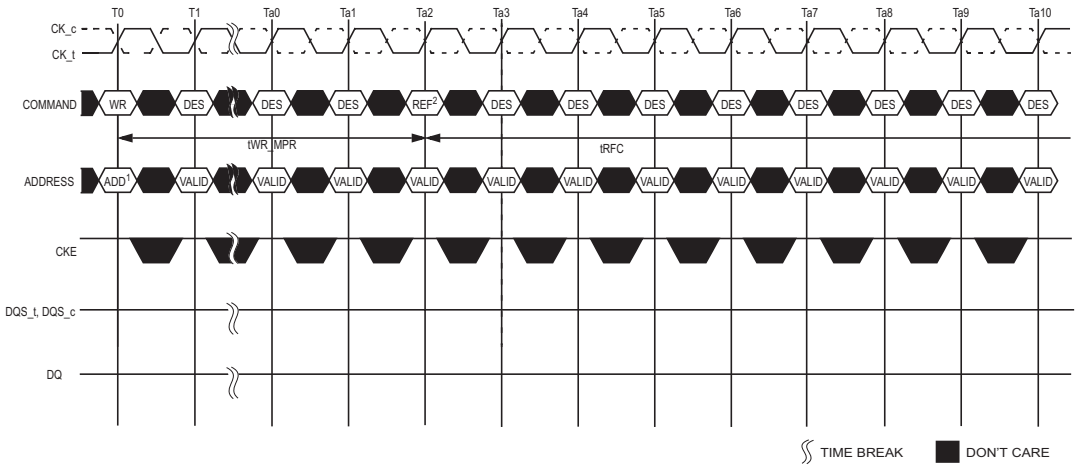
- A[2]= ‘0’b (For BL=8, burst order is fixed at 0,1,2,3,4,5,6,7)

- BA1 and BA0 indicate the MPR location

- A10 and other address pins are don’t care including BG1 and BG0. A12 is don’t care when MR0 A[1:0] = ‘00’ or ‘10’ and must be ‘1’b when MR0 A[1:0] = ‘01’

NOTE 2 1x Refresh is only allowed when MPR mode is Enable.

Write to Refresh Command Timing



NOTE 1 Address setting

- BA1 and BA0 indicate the MPR location
- A [7:0] = data for MPR
- A10 and other address pins are don't care.

NOTE 2 1x Refresh is only allowed when MPR mode is Enable.

MPR Read Data format

Mode bits in MR3: (A12, A11) are used to select the data return format for MPR reads. The DRAM is required to drive associated strobes with the read data returned for all read data formats.

Serial return implies that the same pattern is returned on all DQ lanes as shown in figure below. Data from the MPR is used on all DQ lanes for the serial return case. Reads from MPR page0, MPR page1 and MPR page3 are allowed with serial data return mode.In this example the pattern programmed in the MPR register is 0111 111: MPR Location [7:0].

x4 Device

Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	1	1	1	1	1	1	1
DQ1	0	1	1	1	1	1	1	1
DQ2	0	1	1	1	1	1	1	1
DQ3	0	1	1	1	1	1	1	1

x8 Device

Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	1	1	1	1	1	1	1
DQ1	0	1	1	1	1	1	1	1
DQ2	0	1	1	1	1	1	1	1

Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ3	0	1	1	1	1	1	1	1
DQ4	0	1	1	1	1	1	1	1
DQ5	0	1	1	1	1	1	1	1
DQ6	0	1	1	1	1	1	1	1
DQ7	0	1	1	1	1	1	1	1

x16 Device

Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	1	1	1	1	1	1	1
DQ1	0	1	1	1	1	1	1	1
DQ2	0	1	1	1	1	1	1	1
DQ3	0	1	1	1	1	1	1	1
DQ4	0	1	1	1	1	1	1	1
DQ5	0	1	1	1	1	1	1	1
DQ6	0	1	1	1	1	1	1	1
DQ7	0	1	1	1	1	1	1	1
DQ8	0	1	1	1	1	1	1	1
DQ9	0	1	1	1	1	1	1	1
DQ10	0	1	1	1	1	1	1	1
DQ11	0	1	1	1	1	1	1	1
DQ12	0	1	1	1	1	1	1	1
DQ13	0	1	1	1	1	1	1	1
DQ14	0	1	1	1	1	1	1	1
DQ15	0	1	1	1	1	1	1	1

Parallel return implies that the MPR data is retuned in the first UI and then repeated in the remaining UI's of the burst as shown in the figure below. Data from Page0 MPR registers can be used for the parallel return case as well. Read from MPR page1, MPR page2 and MPR page3 are not allowed with parallel data return mode. In this example the pattern programmed in the Page 0 MPR registeris 0111 1111:MPR Location [7:0]. For the case of x4, only the first four bits are used (0111:MPR Location [7:4] in this example). For thecase of x16, the same pattern is repeated on upper and lower bytes.

x4 Device

Parallel	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	0	0	0	0	0	0	0
DQ1	1	1	1	1	1	1	1	1
DQ2	1	1	1	1	1	1	1	1

Parallel	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ3	1	1	1	1	1	1	1	1

x8 Device

Parallel	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	0	0	0	0	0	0	0
DQ1	1	1	1	1	1	1	1	1
DQ2	1	1	1	1	1	1	1	1
DQ3	1	1	1	1	1	1	1	1
DQ4	1	1	1	1	1	1	1	1
DQ5	1	1	1	1	1	1	1	1
DQ6	1	1	1	1	1	1	1	1
DQ7	1	1	1	1	1	1	1	1

x16 Device

Parallel	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	0	0	0	0	0	0	0
DQ1	1	1	1	1	1	1	1	1
DQ2	1	1	1	1	1	1	1	1
DQ3	1	1	1	1	1	1	1	1
DQ4	1	1	1	1	1	1	1	1
DQ5	1	1	1	1	1	1	1	1
DQ6	1	1	1	1	1	1	1	1
DQ7	1	1	1	1	1	1	1	1
DQ8	1	1	1	1	1	1	1	1
DQ9	1	1	1	1	1	1	1	1
DQ10	1	1	1	1	1	1	1	1
DQ11	1	1	1	1	1	1	1	1
DQ12	1	1	1	1	1	1	1	1
DQ13	1	1	1	1	1	1	1	1
DQ14	1	1	1	1	1	1	1	1
DQ15	1	1	1	1	1	1	1	1

The third mode of data return is the staggering of the MPR data across the lanes. In this mode a read command is issued to a specific MPR and then the data is returned on the DQ from different MPR registers. Read from MPR page1, MPR page2, and MPR page3 are not allowed with staggered data return mode.

For a x4 device, a read to MPR0 will result in data from MPR0 being driven on DQ0, data from MPR1 on DQ1 and so forth as shown below.

A read command to MPR1 will result in data from MPR1 being driven on DQ0, data from MPR2 on DQ1 and so forth as shown below. Reads from MPR2 and MPR3 are also shown below.

MPR Readout Staggered Format, x4

MPR0(BA[1:0]="00')		MPR1(BA[1:0]="01')		MPR2(BA[1:0]="10')		MPR3(BA[1:0]="11')	
Stagger	**UI0-7**	**Stagger**	**UI0-7**	**Stagger**	**UI0-7**	**Stagger**	**UI0-7**
DQ0	MPR0	DQ0	MPR1	DQ0	MPR2	DQ0	MPR3
DQ1	MPR1	DQ1	MPR2	DQ1	MPR3	DQ1	MPR0
DQ2	MPR2	DQ2	MPR3	DQ2	MPR0	DQ2	MPR1
DQ3	MPR3	DQ3	MPR0	DQ3	MPR1	DQ3	MPR2

It is expected that the DRAM can respond to back to back read commands to MPR for all DDR4 frequencies so that a stream as follows can be created on the data bus with no bubbles or clocks between read data. In this case controller issues a sequence of RD MPR0, RD MPR1, RD MPR2, RD MPR3, RD MPR0, RD MPR1, RD MPR2 and RD MPR3.

MPR Readout Staggered Format, x4 (Back to Back read commands)

Stagger	**UI0-7**	**UI8-15**	**UI16-23**	**UI23-31**	**UI32-39**	**UI40-47**	**UI48-55**	**UI56-63**
DQ0	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3
DQ1	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0
DQ2	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1
DQ3	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2

The following figure shows a read command to MPR0 for a x8 device.The same pattern is repeated on the lower nibble as on the upper nibble. Reads to other MPR location follows the same format as for x4 case.

A read example to MPR0 for x8 and x16 device is shown below.

MPR Readout Staggered Format, x8 and x16

x8		x16			
Stagger	**UI0-7**	**Stagger**	**UI0-7**	**Stagger**	**UI0-7**
DQ0	MPR0	DQ0	MPR0	DQ8	MPR0
DQ1	MPR1	DQ1	MPR1	DQ9	MPR1
DQ2	MPR2	DQ2	MPR2	DQ10	MPR2
DQ3	MPR3	DQ3	MPR3	DQ12	MPR3
DQ4	MPR0	DQ4	MPR0	DQ13	MPR0
DQ5	MPR1	DQ5	MPR1	DQ14	MPR1
DQ6	MPR2	DQ6	MPR2	DQ15	MPR2
DQ7	MPR3	DQ7	MPR3	DQ16	MPR3

Four MPR pages are provided in DDR4 SDRAM. Page 0 is for both read and write, and pages 1,2 and 3 are read-only. Any MPR location (MPR0-3) in page 0 can be readable through any of three readout modes (serial, parallel or staggered), but pages 1, 2 and 3 support only the serial readout mode.

After power up, the content of MPR page 0 should have the default value as defined in the table. MPR page 0 can be writeable only when MPR write command is issued by controller. Unless MPR write command is issued, DRAM must keep the default value permanently, and should never change the content on its own for any purpose.

MPR page0 (Training pattern)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	note
BA1:BA0	00 = MPR0	0	1	0	1	0	1	0	1	Read/Write (default value)
	01= MPR1	0	0	1	1	0	0	1	1	
	10 = MPR2	0	0	0	0	1	1	1	1	
	11 = MPR3	0	0	0	0	0	0	0	0	

NOTE 1 MPRx using A7:A0 that A7 is mapped to location [7] and A0 is mapped to location [0].

MPR page1 (CA parity error log)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	note
BA1:BA0	00 = MPR0	A7	A6	A5	A4	A3	A2	A1	A0	Read-only
	01= MPR1	$\overline{CAS}$/A15	$\overline{WE}$/A14	A13	A12	A11	A10	A9	A8	
	10 = MPR2	PAR	$\overline{ACT}$	BG1	BG0	BA1	BA0	A17	$\overline{RAS}$/A16	
	11 = MPR3	CRC Error Status	CA Parity Error Status	CA Parity Latency[4]			C2	C1	C0	
				MR5.A[2]	MR5.A[1]	MR5.A[0]				

NOTE 1 MPR used for C/A parity error log readout is enabled by setting A[2] in MR3

NOTE 2 For higher density of DRAM, where A[17] is not used, MPR2[1] should be treated as don't care.

NOTE 3 If a device is used in monolithic application, where C[2:0] are not used, then MPR3[2:0] should be treated as don't care.

MPR page2 (MRS Readout)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	note
BA1:BA0	00 = MPR0	RFU	RFU	RFU	Temperature Sensor Status[1]		CRC Write Enable	Rtt_WR		read-only
		-	-	-	-	-	MR2	MR2		
		-	-	-	-	-	A12	A10	A9	
	01= MPR1	Vref DQ Trng range	Vref DQ training Value						Gear-down Enable	
		MR6	MR6							
		A6	A5	A4	A3	A2	A1	A0	A3	
	10 = MPR2	CAS Latency				RFU	CAS Write Latency			
		MR0				-	MR2			
		A6	A5	A4	A2	-	A5	A4	A3	
	11 = MPR3	Rtt_Nom			Rtt_Park			Driver Impedance		
		MR1			MR5			MR2		
		A10	A9	A6	A8	A7	A6	A2	A1	

NOTE 1 Temperature Sen-sor Status Readout

MPR0 bit A4	MPR0 bit A3	Refresh Rate Range	MR3[5]
0	0	Sub 1x refresh (>tREFI)	**MR3 bit A5=1 (Temperature sensor readout = Enabled)** DRAM updates the temperature sensor status to MPR Page 2 (MPR0 bits A[4:3]). Temperature data is guaranteed by the DRAM to be no more than 32ms old at the time of MPR Read of the Temperature Sensor Status bits. **MR3 bit A5=0 (Temperature sensor readout = Disabled)** DRAM disables updates to the temperature sensor status in MPR Page 2(MPR0-bit A[4:3])
0	1	1x refresh rate (= tREFI)	
1	0	2x refresh rate (1/2 x tREFI)	
1	1	RFU	

MPR page3 (Vendor purpose only)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	note
BA1:BA0	00 = MPR0	don't care	don't care	don't care	don't care	don't care	don't care	don't care	1	read-only
	01= MPR1	don't care	don't care	don't care	don't care	don't care	don't care	don't care	1	
	10 = MPR2	don't care	don't care	don't care	don't care	don't care	don't care	don't care	1	
	11 = MPR3	don't care	don't care	don't care	don't care	don't care	don't care	don't care	0	

Gear Down Mode

The following ballot represents the sequence for the gear down mode. The DRAM defaults in 1/2 rate(1N) clock mode and utilizes a low frequency MRS command followed by a sync pulse to align the proper clock edge for operating the control lines $\overline{CS}$, CKE and ODT in 1/4rate(2N) mode. For operation in 1/2 rate mode no MRS command for geardown or sync pulse is required. DRAM defaults in 1/2 rate mode.

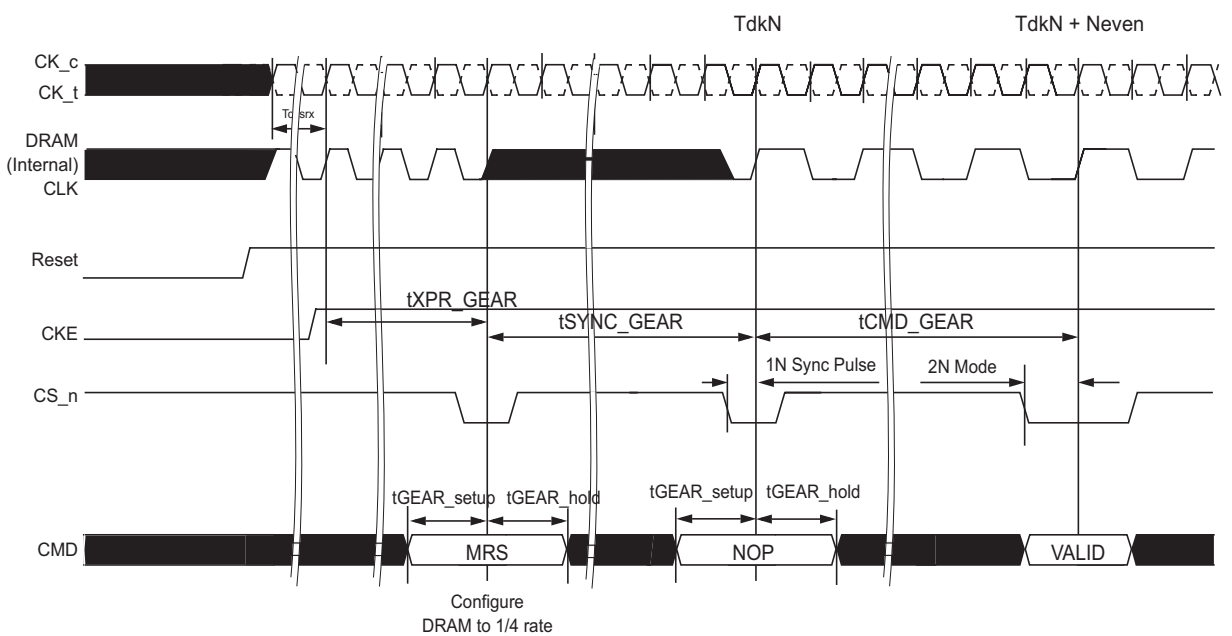
General sequence for operation in geardown during initialization

- DRAM defaults to a 1/2 rate(1N mode) internal clock at power up/reset
- Assertion of reset
- Assertion of CKE enables the rank
- MRS is accessed with a low frequency N*tck MRS geardown CMD.(Ntck static MRS command qualified by 1N $\overline{CS}$).
- MC sends 1N sync pulse with a low frequency N*tck NOP CMD; CK tSYCN_GEAR is an even number of clocks; Sync pulse on even edge from MRS CMD.
- Normal operation in 2N starts tCMD_GEAR clocks later

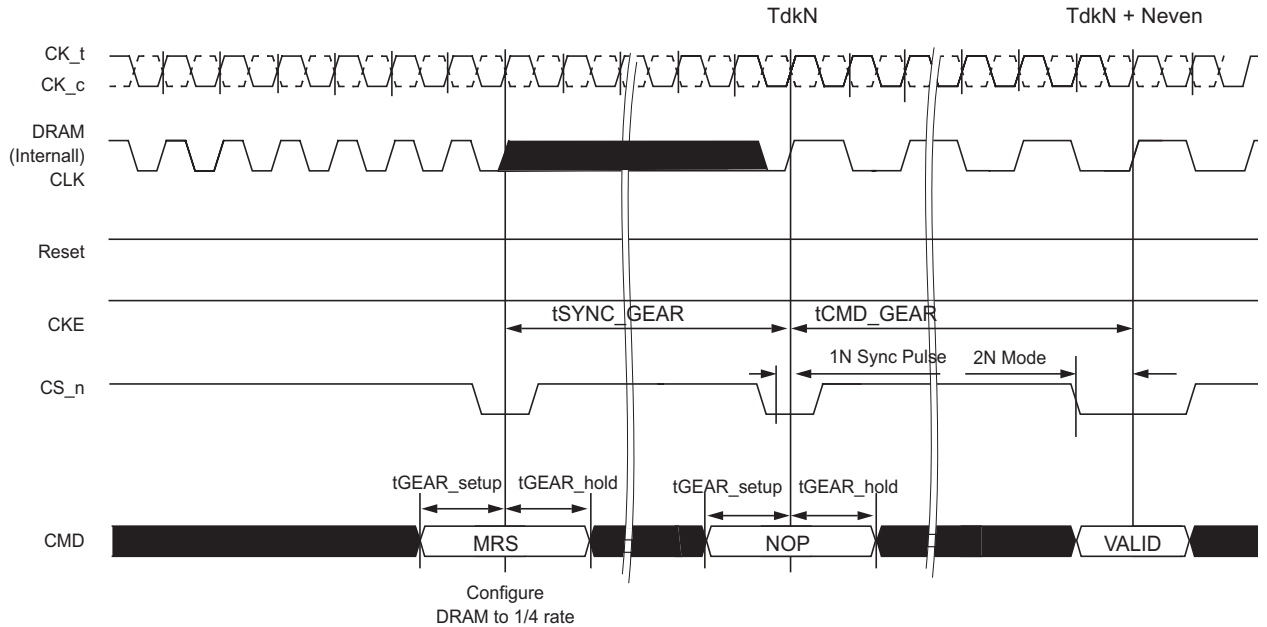
For the operation of geardown mode in 1/4 rate, the following MR settings should be applied.

- CAS Latency (MR0 A[6:4,2]) : Even numbers
- Write Recovery and Read to Precharge (MR0 A[11:9]) : Even numbers
- Additive Latency (MR1 A[4:3]) : 0, CL -2
- CAS Write Latency (MR2 A[5:3]) : Even numbers
- $\overline{CS}$ to Command/Address Latency Mode (MR4 A[8:6]) : Even numbers
- CA Parity Latency Mode (MR5 A[2:0]) : Even numbers

Gear down (2N) mode entry sequence during initialization



Gear down (2N) mode entry sequence during normal operation

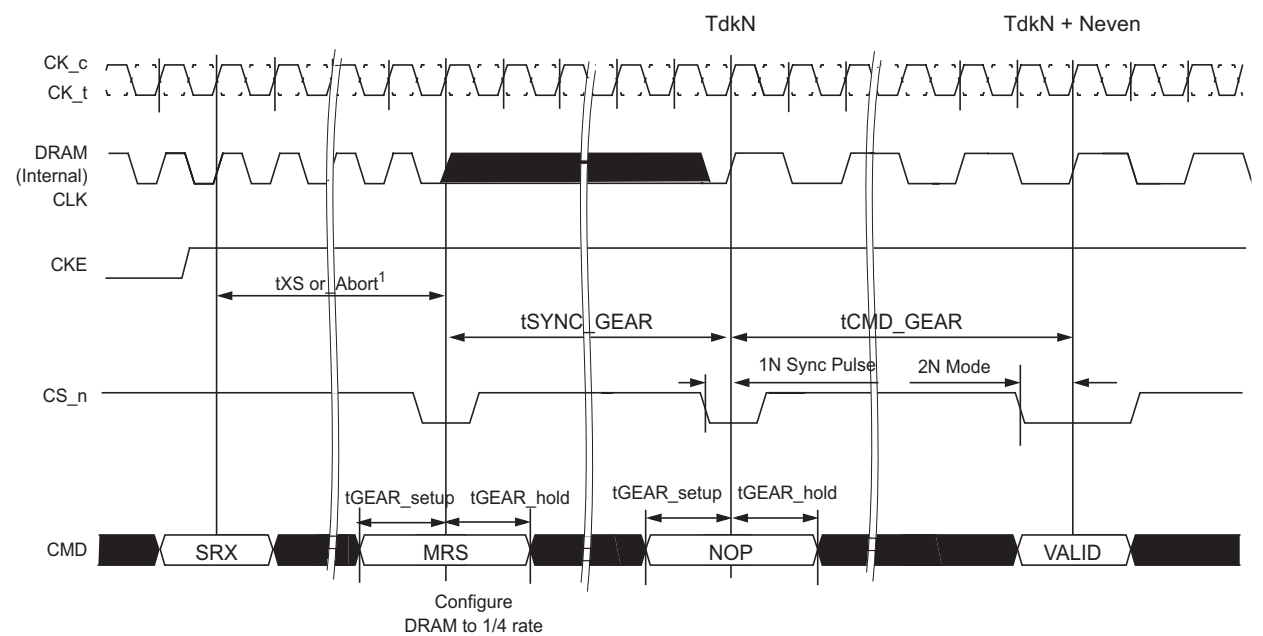


If operation is 1/2 rate(1N) mode before and after self refresh, no MRS command or sync pulse is required during self refresh exit. The min exit delay is tXS, or tXS_Abort to the first valid command.

If operation is in 1/4 rate mode after self refresh exit, the DRAM requires a MRS command and sync pulse as illustrated in the figure below.

DRAM must internally reset to 1N mode from 2N mode during self Refresh and Max Power Saving Mode to properly align internal clock edge with the sync pulse.Illustration below for the DRAM operating in 1/4 rate mode before and after self refresh entry and exit.

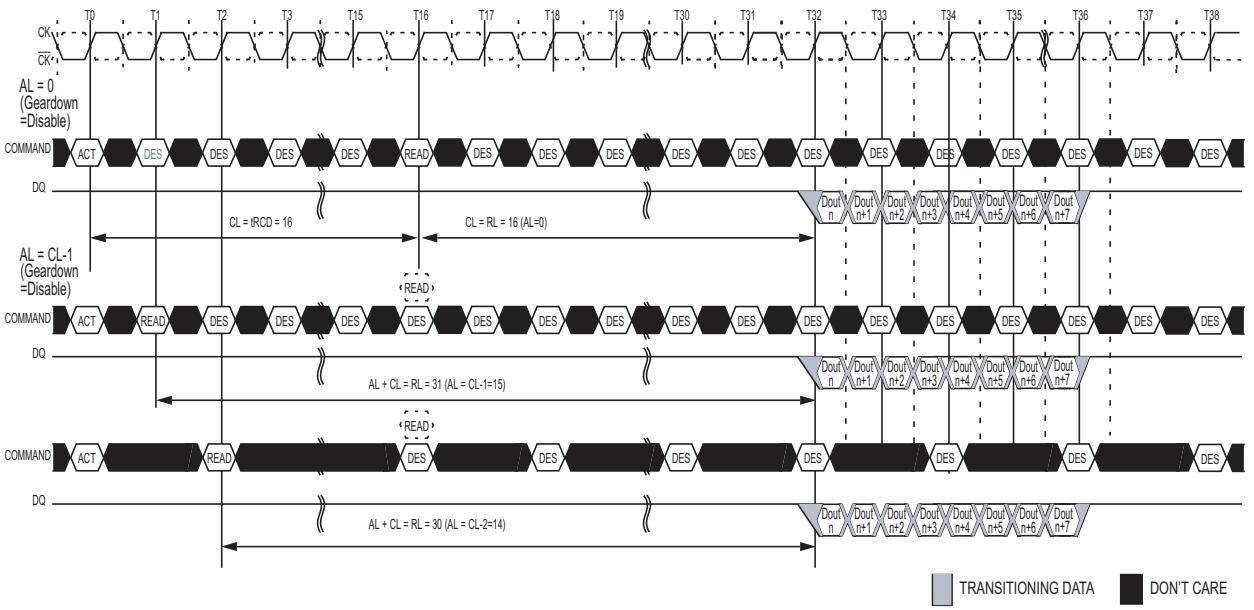
Gear down (2N) mode entry sequence after self refresh exit (SRX)



NOTE 1 CKE High Assert to Gear Down Enable Time (tXS, tXS_Abort) depend on MR setting. A correspondence of tXS/tXS_Abort and MR Setting isas follows.

- MR4[A9] = 0 : tXS
- MR4[A9] = 1 : tXS_Abort

Comparison Timing Diagram Between Geardown Disable and Enable



NOTE 1 BL=8, tRCD=CL=16

NOTE 2 DOUT n = data-out from column n.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read $\overline{DBI}$ = Disable.

Maximum Power Saving Mode

This mode provides lowest power consuming mode which could be similar to the Self-Refresh status with no internal refresh activity.When DDR4 SDRAM is in the maximum power saving mode, it does not need to guarantee data retention nor respond to any external command (except maximum power saving mode exit and asserting $\overline{\text{RESET}}$ signal LOW) to minimize the power consumption.

Mode entry

Max power saving mode is entered through an MRS command. For devices with shared control/address signals, a single DRAM device can be entered into the max power saving mode using the per DRAM Addressability MRS command.

Note that large $\overline{\text{CS}}$ hold time to CKE upon the mode exit may cause DRAM malfunction, thus it is required that the CA parity, CAL and Gear Down modes are disabled prior to the max power saving mode entry MRS command.

Maximum Power Saving mode Entry

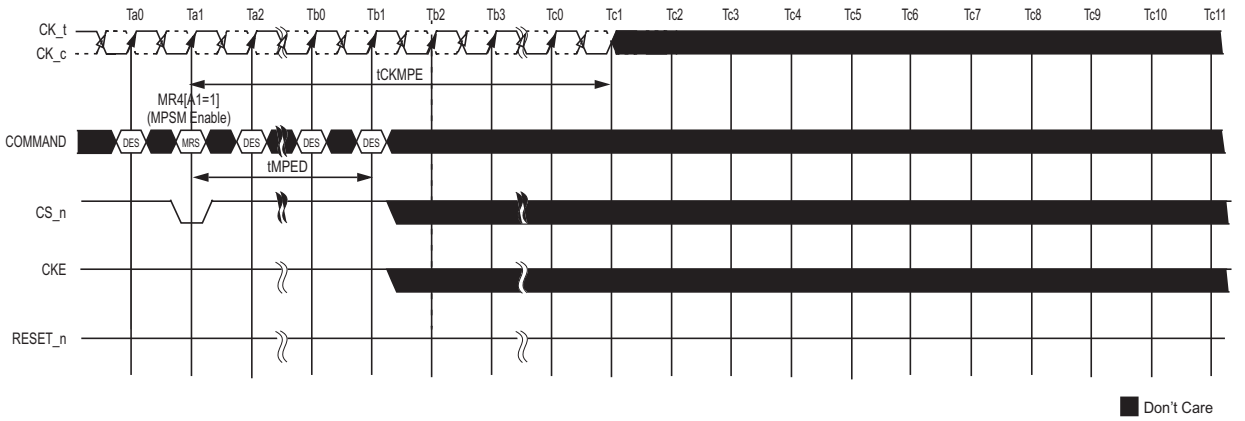
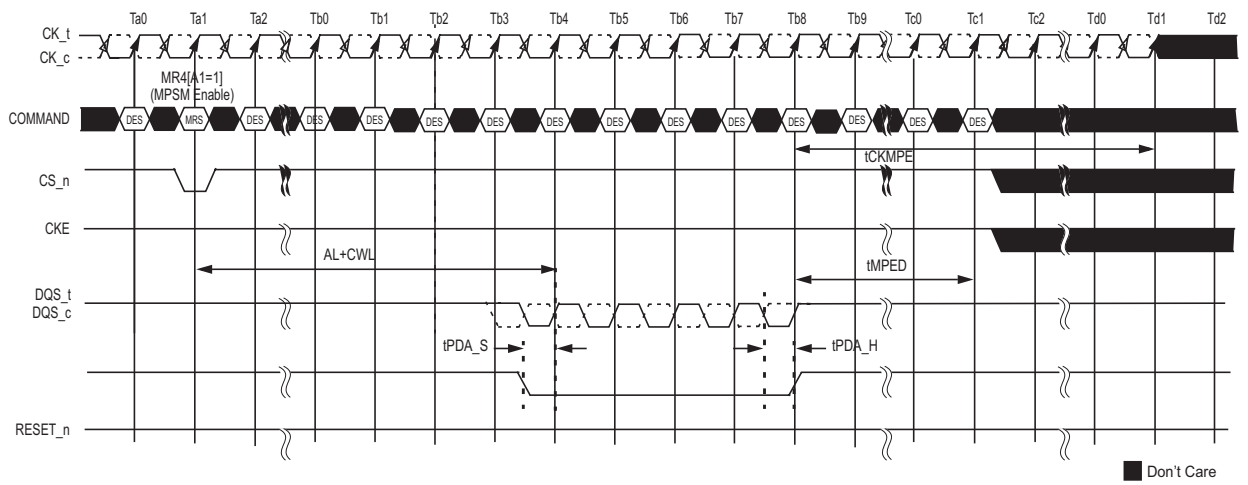


Figure below illustrates the sequence and timing parameters required for the maximum power saving mode with the per DRAM addressability (PDA).

Maximum Power Saving mode Entry with PDA

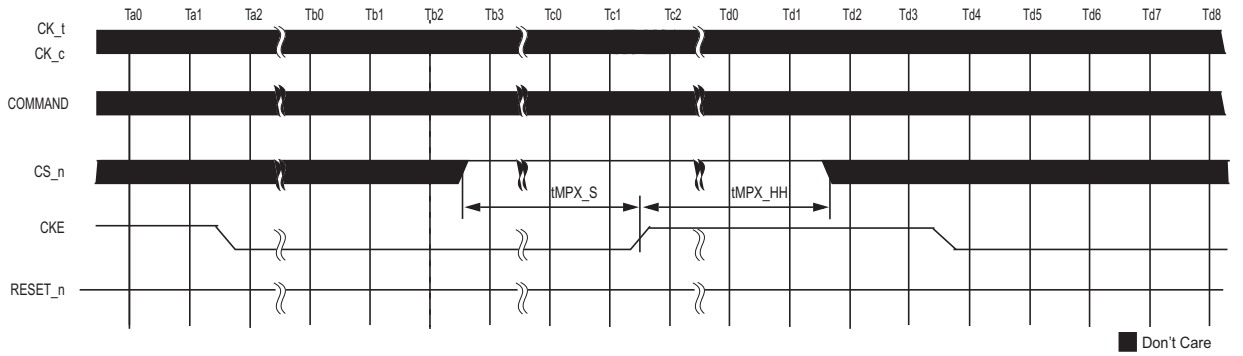


When entering Maximum Power Saving mode, only DES commands are allowed until tMPED is satisfied. After tMPED period from the mode entry command, DRAM is not responsive to any input signals except CS, CKE and RESET signals, and all other input signals can be High-Z. CLK should be valid for tCKMPE period and then can be High-Z.

CKE transition during the mode

CKE toggle is allowed when DRAM is in the maximum power saving mode. To prevent the device from exiting the mode, CS should be issued 'High' at CKE 'L' to 'H' edge with appropriate setup tMPX_S and hold tMPX_HH timings.

CKE Transition Limitation to hold Maximum Power Saving Mode

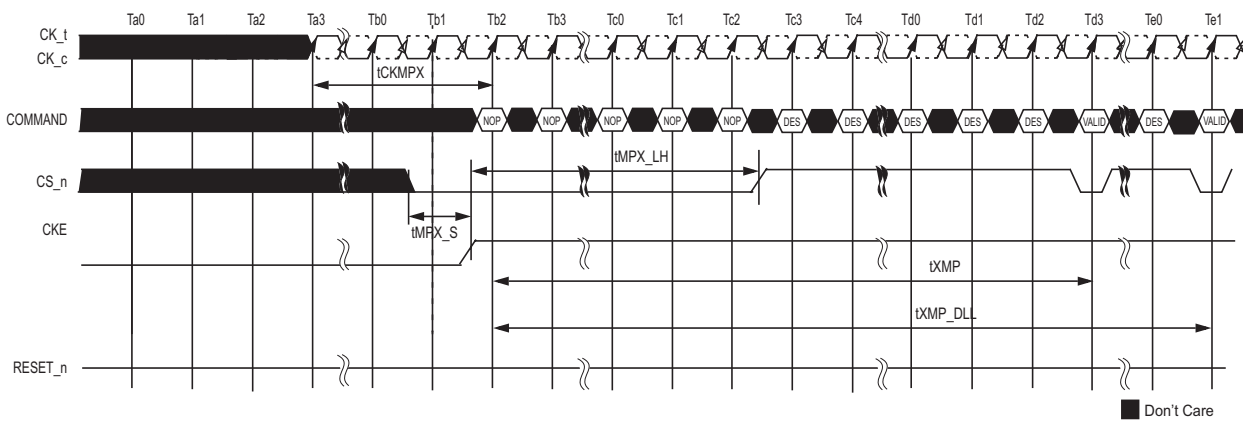


Mode exit

DRAM monitors CS signal level and when it detects CKE 'L' to 'H' transition, and either exits from the power saving mode or stay in the mode depending on the CS signal level at the CKE transition. Because CK receivers are shut down during this mode, CS = 'L' is captured by rising edge of the CKE signal. If CS signal level is detected 'L', then the DRAM initiates internal exit procedure from the power saving mode. CK must be restarted and stable tCKMPX period before the device can exit the maximum power saving mode. During the exit time tXMP, any valid commands except DES command is not allowed to DDR4 SDRAM and also tXMP_DLL, any valid commands requiring a locked DLL is not allowed to DDR4 SDRAM.

When recovering from this mode, the DRAM clears the MRS bits of this mode. It means that the setting of MR4 [A1] is move to '0' automatically.

Maximum Power Saving Mode Exit Sequence



Timing Parameters by Speed Grade

Timing Parameters by Speed Bin for DDR4-2133 and DDR4-2400

Speed		DDR4-2133		DDR4-2400			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Note**
Clock Timing							
Minimum Clock Cycle Time (DLL off mode)	t_{CK} (DLL-off)	8	-	8	-	ns	22
Average Clock Period	t_{CK}(avg)	0.938	<1.071	0.833	<0.938	ns	
Average high pulse width	t_{CH}(avg)	0.48	0.52	0.48	0.52	t_{CK}(avg)	
Average low pulse width	t_{CL}(avg)	0.48	0.52	0.48	0.52	t_{CK}(avg)	
Absolute Clock Period	t_{CK}(abs)	Min: tCK(avg)min+tJIT(per)min_tot Max: tCK(avg)max+ tJIT(per)max_tot				t_{CK}(avg)	
Absolute clock HIGH pulse width	t_{CH}(abs)	0.45	-	0.45	-	t_{CK}(avg)	23
Absolute clock LOW pulse width	t_{CL}(abs)	0.45	-	0.45	-	t_{CK}(avg)	24
Clock Period Jitter- total	JIT(per)_tot	-47	47	-42	42	ps	25
Clock Period Jitter- deterministic	JIT(per)_dj	-23	23	-21	21	ps	26
Clock Period Jitter during DLL locking period	t_{JIT}(per, lck)	-38	38	-33	33	ps	
Cycle to Cycle Period Jitter	t_{JIT}(cc)_total	94		83		ps	25
Cycle to Cycle Period Jitter deterministic	t_{JIT}(cc)_dj	47		42		ps	26
Cycle to Cycle Period Jitter during DLL locking period	t_{JIT}(cc, lck)	75		67		ps	
Duty Cycle Jitter	tJIT(duty)	TBD	TBD	TBD	TBD	ps	
Cumulative error across 2 cycles	t_{ERR}(2per)	-69	69	-61	61	ps	
Cumulative error across 3 cycles	t_{ERR}(2per)	-82	82	-73	73	ps	
Cumulative error across 4 cycles	t_{ERR}(2per)	-91	91	-81	81	ps	
Cumulative error across 4 cycles	t_{ERR}(2per)	-98	98	-87	87	ps	
Cumulative error across 6 cycles	t_{ERR}(2per)	-104	104	-92	92	ps	
Cumulative error across 7 cycles	t_{ERR}(2per)	-109	109	-97	97	ps	
Cumulative error across 8 cycles	t_{ERR}(2per)	-113	113	-101	101	ps	
Cumulative error across 9 cycles	t_{ERR}(2per)	-117	117	-104	104	ps	
Cumulative error across 10 cycles	t_{ERR}(2per)	-120	120	-107	107	ps	
Cumulative error across 11 cycles	t_{ERR}(2per)	-123	123	-110	110	ps	
Cumulative error across 12 cycles	t_{ERR}(2per)	-126	126	-112	112	ps	
Cumulative error across 13 cycles	t_{ERR}(2per)	-129	129	-114	114	ps	
Cumulative error across 14 cycles	t_{ERR}(2per)	-131	131	-116	116	ps	
Cumulative error across 15 cycles	t_{ERR}(2per)	-133	133	-118	118	ps	
Cumulative error across 16 cycles	t_{ERR}(2per)	-135	135	-120	120	ps	
Cumulative error across 17 cycles	t_{ERR}(2per)	-137	137	-122	122	ps	
Cumulative error across 18 cycles	t_{ERR}(2per)	-139	139	-124	124	ps	
Cumulative error across n = 13, 14 . . .49, 50 cycles	t_{ERR}(nper)	tERR(nper)min = ((1 + 0.68ln(n)) * tJIT(per)_total min) tERR(nper)max = ((1 + 0.68ln(n)) * tJIT(per)_total max)				ps	

Speed		DDR4-2133		DDR4-2400			
Parameter	Symbol	Min	Max	Min	Max	Unit	Note
Command and Address setup time to CK, $\overline{CK}$ referenced to Vih(ac) / Vil(ac) levels	t_{IS}(base)	80	-	62	-	ps	
Command and Address setup time to CK, $\overline{CK}$ referenced to Vref levels	t_{IS}(Vref)	180	-	162	-	ps	
Command and Address hold time to CK, $\overline{CK}$ referenced to Vih(dc) / Vil(dc) levels	t_{IH}(base)	105	-	87	-	ps	
Command and Address hold time to CK, $\overline{CK}$ referenced to Vref levels	t_{IH}(Vref)	180	-	162	-	ps	
Control and Address Input pulse width for each input	t_{IPW}	460	-	410	-	ps	
Command and Address Timing							
$\overline{CAS}$ to $\overline{CAS}$ command delay for same bank	t_{CCD_L}	6	-	6	-	nCK	
$\overline{CAS}$ to $\overline{CAS}$ command delay for different bank group	t_{CCD_S}	4	-	4	-	nCK	
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	$t_{RRD\_S(2K)}$	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	nCK	
ACTIVATE to ACTIVATE Command delay to different bank group for 1KB page size	$t_{RRD\_S(1K)}$	Max(4nCK, 3.7ns)	-	Max(4nCK, 3.3ns)	-	nCK	
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	$t_{RRD\_S(1/2K)}$	Max(4nCK, 3.7ns)	-	Max(4nCK, 3.3ns)	-	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	$t_{RRD\_L(2K)}$	Max(4nCK, 6.4ns)	-	Max(4nCK, 6.4ns)	-	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	$t_{RRD\_L(2K)}$	Max(4nCK, 5.3ns)	-	Max(4nCK, 4.9ns)	-	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	$t_{RRD\_L(1/2K)}$	Max(4nCK, 5.3ns)	-	Max(4nCK, 4.9ns)	-	nCK	
Four activate window for 2KB page size	t_{FAW_2K}	Max(28nCK, 30ns)	-	Max(28nCK, 30ns)	-	ns	
Four activate window for 1KB page size	t_{FAW_1K}	Max(20nCK, 21ns)	-	Max(20nCK, 21ns)	-	ns	
Four activate window for 1/2KB page size	$t_{FAW\_1/2K}$	Max(16nCK, 15ns)	-	Max(16nCK, 13ns)	-	ns	
Delay from start of internal write transaction to internal read command for different bank group	t_{WTR_S}	max(2nCK, 2.5ns)	-	max(2nCK, 2.5ns)	-		1,2,e
Delay from start of internal write transaction to internal read command for same bank group	t_{WTR_L}	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-		1
Internal READ Command to PRECHARGE Command delay	t_{RTP}	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-		
WRITE recovery time	t_{WR}	15	-	15	-	ns	1
Write recovery time when CRC and DM are enabled	$t_{WR\_CRC\_DM}$	t_{WR}+max(5nCK,3.75ns)	-	t_{WR}+max(5nCK,3.75ns)	-	ns	1,26

Speed		DDR4-2133		DDR4-2400		Unit	Note
Parameter	Symbol	Min	Max	Min	Max		
delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled	$t_{WTR\_S\_CRC\_DM}$	t_{WTR_S}+max(5nCK,3.75ns)	-	t_{WTR_S}+max(5nCK,3.75ns)	-	ns	2,29
delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	$t_{WTR\_L\_CRC\_DM}$	t_{WTR_L}+max(5nCK,3.75ns)	-	t_{WTR_L}+max(5nCK,3.75ns)	-	ns	3,30
DLL locking time	t_{DLLK}	768	-	768	-	nCK	
Mode Register Set command cycle time	t_{MRD}	8	-	8	-	nCK	
Mode Register Set command update delay	t_{MOD}	max(24nCK, 15ns)	-	max(24nCK, 15ns)	-		
Multi-Purpose Register Recovery Time	t_{MPRR}	1	-	1	-	nCK	33
Multi Purpose Register Write Recovery Time	t_{WR_MPR}	t_{MOD} (min)+ AL + PL	-	t_{MOD} (min)+ AL + PL	-		
Auto precharge write recovery + precharge time	$t_{DAL(min)}$	Programmed WR + roundup (tRP / tCK(avg))				nCK	
$\overline{CS}$ to Command Address Latency							
$\overline{CS}$ to Command Address Latency	t_{CAL}	4	-	5	-	nCK	
DRAM Data Timing							
DQS,$\overline{DQS}$ to DQ skew, per group, per access	t_{DQSQ}	-	TBD	-	TBD	t_{CK}(avg)/2	13,18
DQS,$\overline{DQS}$ to DQ Skew deterministic, per group, per access	t_{DQSQ}	-	TBD	-	TBD	t_{CK}(avg)/2	13,16,18
DQ output hold time from DQS,$\overline{DQS}$	t_{QH}	TBD	-	TBD	-	t_{CK}(avg)/2	13,17,18
DQ output hold time deterministic from DQS,$\overline{DQS}$	t_{QH}	TBD	-	TBD	-	UI	14,16,18
DQS,$\overline{DQS}$ to DQ Skew total, per group, per access; DBI enabled	t_{DQSQ}	-	TBD	-	TBD	UI	13,19
DQ output hold time total from DQS,$\overline{DQS}$; DBI enabled	t_{QH}	TBD	-	TBD	-	UI	13,19
DQ to DQ offset , per group, per access referenced to DQS,$\overline{DQS}$	t_{DQSQ}	TBD	TBD	TBD	TBD	UI	15,16
Data Strobe Timing							
DQS,$\overline{DQS}$ differential READ Preamble (2 clock preamble)	t_{RPRE}	0.9	TBD	0.9	TBD	nCK	
DQS,$\overline{DQS}$ differential READ Postamble	t_{RPST}	TBD	TBD	TBD	TBD	nCK	
DQS,$\overline{DQS}$ differential output high time	t_{QSH}	0.4	-	0.4	-	nCK	21
DQS,$\overline{DQS}$ differential output low time	t_{QSL}	0.4	-	0.4	-	nCK	20
DQS,$\overline{DQS}$ differential WRITE Preamble	t_{WPRE}	0.9	-	0.9	-	nCK	
DQS,$\overline{DQS}$ differential WRITE Postamble	t_{WPST}	TBD	TBD	TBD	TBD	nCK	
DQS and $\overline{DQS}$ low-impedance time	t_{LZ}(DQS)	-360	180	-300	150	ps	
DQS and $\overline{DQS}$ high-impedance time (Referenced from RL+BL/2)	t_{HZ}(DQS)	-	180	-	150	ps	

Speed		DDR4-2133		DDR4-2400			
Parameter	Symbol	Min	Max	Min	Max	Unit	Note
DQS,$\overline{DQS}$ differential input low pulse width	t_{DQSL}	0.46	0.54	0.46	0.54	nCK	
DQS,$\overline{DQS}$ differential input high pulse width	t_{DQSH}	0.46	0.54	0.46	0.54	nCK	
DQS,$\overline{DQS}$ rising edge to CK,$\overline{CK}$ rising edge (1 clock preamble)	t_{DQSS}	-0.27	0.27	-0.27	0.27	nCK	
DQS,$\overline{DQS}$ falling edge setup time to CK,$\overline{CK}$	t_{DSS}	0.18	-	0.18	-	nCK	
DQS,$\overline{DQS}$ falling edge hold time from CK,$\overline{CK}$	t_{DSH}	0.18	-	0.18	-	nCK	
MPSM Timing							
Command path disable delay upon MPSM entry	t_{MPED}	Min: t_{MOD}(min) +t_{CPDED}(min)					
Valid clock requirement after MPSM entry	t_{CKMPE}	Min: t_{MOD}(min) +t_{CPDED}(min)					
Valid clock requirement before MPSM exit	t_{CKMPX}	Min: t_{CKSRX}(min)					
Exit MPSM to commands not requiring a locked DLL	t_{XMP}	TBD	-	TBD	-		
Exit MPSM to commands requiring a locked DLL	t_{XMPDLL}	Min: t_{XMP}(min) + t_{XSDLL}(min)					
CS setup time to CKE	t_{MPX_S}	TBD	-	TBD	-		
CS hold time to CKE	t_{MPX_H}	TBD	-	TBD	-		
Calibration Timing							
Power-up and RESET calibration time	t_{ZQinit}	1024	-	1024	-	nCK	
Normal operation Full calibration time	t_{ZQoper}	512	-	512	-	nCK	
Normal operation Short calibration time	t_{ZQCS}	128	-	128	-	nCK	
Reset/Self Refresh Timing							
Exit Reset from CKE HIGH to a valid command	t_{XPR}	Max: max(5nCK,t_{RFC}(min)+10ns)					
Exit Self Refresh to commands not requiring a locked DLL	t_{XS}	Min: t_{RFC}(min)+10ns					
SRX to commands not requiring a locked DLL in Self Refresh ABORT	$t_{XS\_ABORT(min)}$	Min: t_{RFC4}(min)+10ns					
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	$t_{XS\_FAST(min)}$	Min: t_{RFC4}(min)+10ns					
Exit Self Refresh to commands requiring a locked DLL	t_{XSDLL}	Min: t_{DLLK}(min)					
Minimum CKE low width for Self refresh entry to exit timing	t_{CKESR}	Min: t_{CKE}(min)+1nCK					
Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled	t_{CKESR_PAR}	Min: t_{CKE}(min)+1nCK+PL					
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	t_{CKSRE}	Min: max(5nCK,10ns)					
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	t_{CKSRE_PAR}	Min: max(5nCK,10ns)+PL					

Speed		DDR4-2133		DDR4-2400			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Note**
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	t_{CKSRX}	Min: max(5nCK,10ns)					
Power Down Timing							
Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	t_{XP}	Min: max(4nCK,6ns)					
CKE minimum pulse width	t_{CKE}	Min: max (3nCK,5ns)					31,32
Command pass disable delay	t_{CPDED}	4	-	4	-	nCK	
Power Down Entry to Exit Timing	t_{PD}	t_{CKE}(min)	$9xt_{REFI}$	t_{CKE}(min)	$9xt_{REFI}$		6
Timing of ACT command to Power Down entry	$t_{ACTPDEN}$	2	-	2	-	nCK	7
Timing of PRE or PREA command to Power Down entry	t_{PRPDEN}	2	-	2	-	nCK	7
Timing of RD/RDA command to Power Down entry	t_{RDPDEN}	RL+4+1	-	RL+4+1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	t_{WRPDEN}	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	$t_{WRAPDEN}$	WL+4+WR+1	-	WL+4+WR+1	-	nCK	5
Timing of WR command to Power Down entry (BC4MRS)	$t_{WRPBC4DEN}$	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	$t_{WRAPBC4DEN}$	WL+2+WR+1	-	WL+2+WR+1	-	nCK	5
Timing of REF command to Power Down entry	$t_{REFPDEN}$	2	-	1	-	nCK	7
Timing of MRS command to Power Down entry	$t_{MRSPDEN}$	t_{MOD}(min)	-	t_{MOD}(min)	-	ps	
PDA Timing							
Mode Register Set command cycle time in PDA mode	t_{MRD_PDA}	max(16nCK, 10ns)		max(16nCK, 10ns)			
Mode Register Set command update delay in PDA mode	t_{MOD_PDA}	t_{MOD}					
ODT Timing							
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	t_{AONAS}	1.0	9.0	1.0	9.0	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	t_{AOFAS}	1.0	9.0	1.0	9.0	ns	
RTT dynamic change skew	t_{ADC}	0.3	0.7	0.3	0.7	t_{CK}(avg)	
Write Leveling Timing							
First DQS/$\overline{DQS}$ rising edge after write leveling mode is programmed	t_{WLMRD}	40	-	40	-	nCK	

Speed		DDR4-2133		DDR4-2400		Unit	Note
Parameter	Symbol	Min	Max	Min	Max		
DQS/$\overline{DQS}$ delay after write leveling mode is programmed	$t_{WLDQSEN}$	25	-	25	-	nCK	
Write leveling setup time from rising CK/$\overline{CK}$ crossing to rising DQS/$\overline{DQS}$ crossing	t_{WLS}	0.13	-	0.13	-	t_{CK}(avg)	
Write leveling hold time from rising CK/$\overline{CK}$ crossing to rising DQS/$\overline{DQS}$ crossing	t_{WLH}	0.13	-	0.13	-	t_{CK}(avg)	
Write leveling output delay	t_{WLO}	0	9.5	0	9.5	ns	
Write leveling output error	t_{WLOE}	0	2	0	2	ns	
CA Parity Timing							
Commands not guaranteed to be executed during this time	$t_{PAR\_UNKNOWN}$	-	PL	-	PL		
Delay from errant command to $\overline{ALERT}$ assertion	$t_{PAR\_ALERT\_ON}$	-	PL+6ns	-	PL+6ns		
Pulse width of $\overline{ALERT}$ signal when asserted	$t_{PAR\_ALERT\_PW}$	64	128	72	114	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	$t_{PAR\_ALERT\_RSP}$	-	57	-	64	nCK	
Parity Latency	PL	4		5		nCK	
CRC Error Timing							
CRC error to $\overline{ALERT}$ latency	t_{CRC_ALERT}	3	13	3	13	ns	
CRC $\overline{ALERT}$ pulse width	CRC_ALERT_PW	6	10	6	10	nCK	
Geardown timing							
Exit RESET from CKE HIGH to a valid MRS geardown (T2/Reset)	t_{XPR_GEAR}	-		-			
CKE High Assert to Gear Down Enable time(T2/CKE)	t_{XS_GEAR}	-		-			
MRS command to Sync pulse time(T3)	t_{SYNC_GEAR}	-	-	-	-		27
Sync pulse to First valid command(T4)	t_{CMD_GEAR}	-		-			27
Geardown setup time	t_{GEAR_setup}	-	-	-	-	nCK	
Geardown hold time	t_{GEAR_hold}	-	-	-	-	nCK	
t_{REFI}							
t_{RFC1} (min)	2Gb	160	-	160	-	ns	
	4Gb	260	-	260	-	ns	
	8Gb	350	-	350	-	ns	
	16Gb	TBD	-	TBD	-	ns	
t_{RFC2} (min)	2Gb	110	-	110	-	ns	
	4Gb	160	-	160	-	ns	
	8Gb	260	-	260	-	ns	
	16Gb	TBD	-	TBD	-	ns	

Speed		DDR4-2133		DDR4-2400			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Note**
t_{RFC4} (min)	2Gb	90	-	90	-	ns	
	4Gb	110	-	110	-	ns	
	8Gb	160	-	160	-	ns	
	16Gb	TBD	-	TBD	-	ns	

Timing Parameters by Speed Bin for DDR4-2666 and DDR4-3200

Speed		DDR4-2666		DDR4-3200			
Parameter	Symbol	Min	Max	Min	Max	Unit	Note
Clock Timing							
Minimum Clock Cycle Time (DLL off mode)	t_{CK} (DLL-off)	8	20	8	-	ns	22
Average Clock Period	t_{CK}(avg)	0.750	<0.833	0.625	<0.750	ns	
Average high pulse width	t_{CH}(avg)	0.48	0.52	0.48	0.52	t_{CK}(avg)	
Average low pulse width	t_{CL}(avg)	0.48	0.52	0.48	0.52	t_{CK}(avg)	
Absolute Clock Period	t_{CK}(abs)	Min: tCK(avg)min+tJIT(per)min_tot Max: tCK(avg)max+ tJIT(per)max_tot				t_{CK}(avg)	
Absolute clock HIGH pulse width	t_{CH}(abs)	0.45	-	0.45	-	t_{CK}(avg)	23
Absolute clock LOW pulse width	t_{CL}(abs)	0.45	-	0.45	-	t_{CK}(avg)	24
Clock Period Jitter- total	JIT(per)_tot	-38	38	-0.1	0.1	ps	25
Clock Period Jitter- deterministic	JIT(per)_dj	-19	19	TBD	TBD	ps	26
Clock Period Jitter during DLL locking period	t_{JIT}(per, lck)	-30	30	TBD	TBD	ps	
Cycle to Cycle Period Jitter	t_{JIT}(cc)_total	75		TBD		ps	25
Cycle to Cycle Period Jitter deterministic	t_{JIT}(cc)_dj	TBD		TBD		ps	26
Cycle to Cycle Period Jitter during DLL locking period	t_{JIT}(cc, lck)	60		TBD		ps	
Duty Cycle Jitter	tJIT(duty)	TBD	TBD	TBD	TBD	ps	
Cumulative error across 2 cycles	t_{ERR}(2per)	-55	55	TBD	TBD	ps	
Cumulative error across 3 cycles	t_{ERR}(2per)	-66	66	TBD	TBD	ps	
Cumulative error across 4 cycles	t_{ERR}(2per)	-73	73	TBD	TBD	ps	
Cumulative error across 5 cycles	t_{ERR}(2per)	-78	78	TBD	TBD	ps	
Cumulative error across 6 cycles	t_{ERR}(2per)	-83	83	TBD	TBD	ps	
Cumulative error across 7 cycles	t_{ERR}(2per)	-87	87	TBD	TBD	ps	
Cumulative error across 8 cycles	t_{ERR}(2per)	-91	91	TBD	TBD	ps	
Cumulative error across 9 cycles	t_{ERR}(2per)	-94	94	TBD	TBD	ps	
Cumulative error across 10 cycles	t_{ERR}(2per)	-96	96	TBD	TBD	ps	
Cumulative error across 11 cycles	t_{ERR}(2per)	-99	99	TBD	TBD	ps	
Cumulative error across 12 cycles	t_{ERR}(2per)	-101	101	TBD	TBD	ps	
Cumulative error across 13 cycles	t_{ERR}(2per)	-103	103	TBD	TBD	ps	
Cumulative error across 14 cycles	t_{ERR}(2per)	-104	104	TBD	TBD	ps	
Cumulative error across 15 cycles	t_{ERR}(2per)	-106	106	TBD	TBD	ps	
Cumulative error across 16 cycles	t_{ERR}(2per)	-108	108	TBD	TBD	ps	
Cumulative error across 17 cycles	t_{ERR}(2per)	-110	110	TBD	TBD	ps	
Cumulative error across 18 cycles	t_{ERR}(2per)	-112	112	TBD	TBD	ps	
Cumulative error across n = 13, 14 . . .49, 50 cycles	t_{ERR}(nper)	tERR(nper)min = ((1 + 0.68ln(n)) * tJIT(per)_total min) tERR(nper)max = ((1 + 0.68ln(n)) * tJIT(per)_total max)				ps	
Command and Address setup time to CK, $\overline{CK}$ referenced to Vih(ac) / Vil(ac) levels	t_{IS}(base)	55	-	TBD	-	ps	

Speed		DDR4-2666		DDR4-3200			
Parameter	Symbol	Min	Max	Min	Max	Unit	Note
Command and Address setup time to CK, $\overline{CK}$ referenced to Vref levels	t_{IS}(Vref)	145	-	TBD	-	ps	
Command and Address hold time to CK, $\overline{CK}$ referenced to Vih(dc) / Vil(dc) levels	t_{IH}(base)	80	-	TBD	-	ps	
Command and Address hold time to CK, $\overline{CK}$ referenced to Vref levels	t_{IH}(Vref)	145	-	TBD	-	ps	
Control and Address Input pulse width for each input	t_{IPW}	385	-	TBD	-	ps	
Command and Address Timing							
$\overline{CAS}$ to $\overline{CAS}$ command delay for same bank	t_{CCD_L}	max(5 nCK,5ns)	-	TBD	-	nCK	
$\overline{CAS}$ to $\overline{CAS}$ command delay for different bank group	t_{CCD_S}	4	-	TBD	-	nCK	
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	$t_{RRD\_S(2K)}$	Max(4nCK,5.3ns)	-	TBD	-	nCK	
ACTIVATE to ACTIVATE Command delay to different bank group for 1KB page size	$t_{RRD\_S(1K)}$	Max(4nCK,3ns)	-	TBD	-	nCK	
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	$t_{RRD\_S(1/2K)}$	Max(4nCK,3ns)	-	TBD	-	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	$t_{RRD\_L(2K)}$	Max(4nCK,6.4ns)	-	TBD	-	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	$t_{RRD\_L(1K)}$	Max(4nCK,4.9ns)	-	TBD	-	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	$t_{RRD\_L(1/2K)}$	Max(4nCK,4.9ns)	-	TBD	-	nCK	
Four activate window for 2KB page size	t_{FAW_2K}	Max(28nCK,30ns)	-	TBD	-	ns	
Four activate window for 1KB page size	t_{FAW_1K}	Max(20nCK,21ns)	-	TBD	-	ns	
Four activate window for 1/2KB page size	$t_{FAW\_1/2K}$	Max(16nCK,12ns)	-	TBD	-	ns	
Delay from start of internal write transaction to internal read command for different bank group	t_{WTR_S}	Max(2nCK,2.5ns)	-	TBD	-		1,2,e
Delay from start of internal write transaction to internal read command for same bank group	t_{WTR_L}	Max(4nCK,7.5ns)	-	TBD	-		1
Internal READ Command to PRECHARGE Command delay	t_{RTP}	Max(4nCK,7.5ns)	-	TBD	-		
WRITE recovery time	t_{WR}	15	-	TBD	-	ns	1
Write recovery time when CRC and DM are enabled	$t_{WR\_CRC\_DM}$	tWR+Max(5nCK,3.75ns)	-	TBD	-	ns	1,26

Speed		DDR4-2666		DDR4-3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max		
delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled	$t_{WTR\_S\_CRC\_DM}$	tWTR_S+max(5nCK,3.75ns)	-	TBD	-	ns	2,29
delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	$t_{WTR\_L\_CRC\_DM}$	tWTR_L+max(5nCK,3.75ns)	-	TBD	-	ns	3,30
DLL locking time	t_{DLLK}	1024	-	TBD	-	nCK	
Mode Register Set command cycle time	t_{MRD}	8	-	TBD	-	nCK	
Mode Register Set command update delay	t_{MOD}	Max(24nCK,15ns)	-	TBD	-		
Multi-Purpose Register Recovery Time	t_{MPRR}	1	-	TBD	-	nCK	33
Multi Purpose Register Write Recovery Time	t_{WR_MPR}	tMOD(min)+AL+PL	-	TBD	-		
Auto precharge write recovery + precharge time	$t_{DAL(min)}$	Programmed WR + roundup (tRP / tCK(avg))				nCK	
$\overline{CS}$ to Command Address Latency							
$\overline{CS}$ to Command Address Latency	t_{CAL}	Max(3nCK,3.748ns)	-	TBD	-	nCK	
DRAM Data Timing							
DQS,$\overline{DQS}$ to DQ skew, per group, per access	t_{DQSQ}	-	0.18	-	TBD	t_{CK}(avg)/2	13,18
DQ output hold time from DQS,$\overline{DQS}$	t_{QH}	0.74	-	TBD	-	t_{CK}(avg)/2	13,17,18
DQ output hold time deterministic from DQS,$\overline{DQS}$	t_{QH}	TBD	-	TBD	-	UI	14,16,18
DQS,$\overline{DQS}$ to DQ Skew total, per group, per access; DBI enabled	t_{DQSQ}	-	TBD	-	TBD	UI	13,19
DQ output hold time total from DQS,$\overline{DQS}$; DBI enabled	t_{QH}	TBD	-	TBD	-	UI	13,19
DQ to DQ offset , per group, per access referenced to DQS,$\overline{DQS}$	t_{DQSQ}	TBD	TBD	TBD	TBD	UI	15,16
Data Strobe Timing							
DQS,$\overline{DQS}$ differential READ Preamble (1 clock preamble)	t_{RPRE}	0.9	TBD	TBD	TBD	nCK	
DQS,$\overline{DQS}$ differential READ Postamble	t_{RPST}	10.33	TBD	TBD	TBD	nCK	
DQS,$\overline{DQS}$ differential output high time	t_{QSH}	0.4	TBD	TBD	TBD	nCK	21
DQS,$\overline{DQS}$ differential output low time	t_{QSL}	0.4	TBD	TBD	TBD	nCK	20
DQS,$\overline{DQS}$ differential WRITE Preamble	t_{WPRE}	0.9	TBD	TBD	TBD	nCK	
DQS,$\overline{DQS}$ differential WRITE Postamble	t_{WPST}	0.33	TBD	TBD	TBD	nCK	
DQS and $\overline{DQS}$ low-impedance time	t_{LZ}(DQS)	-310	170	TBD	TBD	ps	
DQS and $\overline{DQS}$ high-impedance time (Referenced from RL+BL/2)	t_{HZ}(DQS)	-	170	TBD	TBD	ps	
DQS,$\overline{DQS}$ differential input low pulse width	t_{DQSL}	0.46	0.54	TBD	TBD	nCK	

Speed		DDR4-2666		DDR4-3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max		
DQS,$\overline{DQS}$ differential input high pulse width	t_{DQSH}	0.46	0.54	TBD	TBD	nCK	
DQS,$\overline{DQS}$ rising edge to CK,$\overline{CK}$ rising edge (1 clock preamble)	t_{DQSS}	-0.27	0.27	TBD	TBD	nCK	
DQS,$\overline{DQS}$ falling edge setup time to CK,$\overline{CK}$	t_{DSS}	0.18	-	TBD	TBD	nCK	
DQS,$\overline{DQS}$ falling edge hold time from CK,$\overline{CK}$	t_{DSH}	0.18	-	TBD	TBD	nCK	
MPSM Timing							
Command path disable delay upon MPSM entry	t_{MPED}	tMOD(min)+tCPDED(min)					
Valid clock requirement after MPSM entry	t_{CKMPE}	tMOD(min)+tCPDED(min)					
Valid clock requirement before MPSM exit	t_{CKMPX}	tCKSRX(min)					
Exit MPSM to commands not requiring a locked DLL	t_{XMP}	tXS(min)	-	TBD	-		
Exit MPSM to commands requiring a locked DLL	t_{XMPDLL}	tXMP(min)+tXSDLL(min)					
CS setup time to CKE	t_{MPX_S}	tISmin+tIH-min	-	TBD	-		
CS hold time to CKE	t_{MPX_H}	TBD	-	TBD	-		
Calibration Timing							
Power-up and RESET calibration time	t_{ZQinit}	1024	-	TBD	-	nCK	
Normal operation Full calibration time	t_{ZQoper}	512	-	TBD	-	nCK	
Normal operation Short calibration time	t_{ZQCS}	128	-	TBD	-	nCK	
Reset/Self Refresh Timing							
Exit Reset from CKE HIGH to a valid command	t_{XPR}	Max(5nCK,tRFC(min)+10ns)					
Exit Self Refresh to commands not requiring a locked DLL	t_{XS}	tRFC(min)+10ns					
SRX to commands not requiring a locked DLL in Self Refresh ABORT	$t_{XS\_ABORT(min)}$	Min: t_{RFC4}(min)+10ns					
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	$t_{XS\_FAST(min)}$	Min: t_{RFC4}(min)+10ns					
Exit Self Refresh to commands requiring a locked DLL	t_{XSDLL}	tDLLK(min)					
Minimum CKE low width for Self refresh entry to exit timing	t_{CKESR}	tCKE(min)+1nck					
Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled	t_{CKESR_PAR}	Min: t_{CKE}(min)+1nCK+PL					
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	t_{CKSRE}	Max:(5nCK,10ns)					
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	t_{CKSRE_PAR}	Max:(5nCK,10ns)+P:L					

Speed		DDR4-2666		DDR4-3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max		
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	t_{CKSRX}	max(snck,10ns)					
Power Down Timing							
Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	t_{XP}	max(4nCK,6ns)					
CKE minimum pulse width	t_{CKE}	max(3nCK,5ns)					31,32
Command pass disable delay	t_{CPDED}	4	-	TBD	-	nCK	
Power Down Entry to Exit Timing	t_{PD}	tCKE(min)	-	TBD	-		6
Timing of ACT command to Power Down entry	$t_{ACTPDEN}$	2	-	TBD	-	nCK	7
Timing of PRE or PREA command to Power Down entry	t_{PRPDEN}	2	-	TBD	-	nCK	7
Timing of RD/RDA command to Power Down entry	t_{RDPDEN}	RL+4+1	-	TBD	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	t_{WRPDEN}	WL+4+(tWR/tCK(avg)	-	TBD	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	$t_{WRAPDEN}$	WL+4+WR+1	-	TBD	-	nCK	5
Timing of WR command to Power Down entry (BC4MRS)	$t_{WRPBC4DEN}$	WL+2+(tWR/tCK(avg)	-	TBD	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	$t_{WRAPBC4DEN}$	WL+2+WR+1	-	TBD	-	nCK	5
Timing of REF command to Power Down entry	$t_{REFPDEN}$	2	-	TBD	-	nCK	7
Timing of MRS command to Power Down entry	$t_{MRSPDEN}$	tMOD(min)	-	TBD	-	ps	
PDA Timing							
Mode Register Set command cycle time in PDA mode	t_{MRD_PDA}	max(16nCKm,10ns)	-	TBD	-		
Mode Register Set command update delay in PDA mode	t_{MOD_PDA}	tMOD					
ODT Timing							
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	t_{AONAS}	1	9	TBD	TBD	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	t_{AOFAS}	1	9	TBD	TBD	ns	
RTT dynamic change skew	t_{ADC}	0.28	0.72	TBD	TBD	t_{CK}(avg)	
Write Leveling Timing							
First DQS/$\overline{DQS}$ rising edge after write leveling mode is programmed	t_{WLMRD}	40	-	TBD	TBD	nCK	

Speed		DDR4-2666		DDR4-3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max		
DQS/$\overline{DQS}$ delay after write leveling mode is programmed	$t_{WLDQSEN}$	25	-	TBD	TBD	nCK	
Write leveling setup time from rising CK/$\overline{CK}$ crossing to rising DQS/$\overline{DQS}$ crossing	t_{WLS}	0.13	-	TBD	TBD	t_{CK}(avg)	
Write leveling hold time from rising CK/$\overline{CK}$ crossing to rising DQS/$\overline{DQS}$ crossing	t_{WLH}	0.13	-	TBD	TBD	t_{CK}(avg)	
Write leveling output delay	t_{WLO}	0	9.5	TBD	TBD	ns	
Write leveling output error	t_{WLOE}	0	2	0	2	ns	
CA Parity Timing							
Commands not guaranteed to be executed during this time	$t_{PAR\_UNKNOWN}$	-	PL	-	TBD		
Delay from errant command to $\overline{ALERT}$ assertion	$t_{PAR\_ALERT\_ON}$	-	PL+6ns	-	TBD		
Pulse width of $\overline{ALERT}$ signal when asserted	$t_{PAR\_ALERT\_PW}$	80	160	TBD	TBD	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	$t_{PAR\_ALERT\_RSP}$	-	71	TBD	TBD	nCK	
Parity Latency	PL	5		TBD		nCK	
CRC Error Timing							
CRC error to $\overline{ALERT}$ latency	t_{CRC_ALERT}	3	13	TBD	TBD	ns	
CRC $\overline{ALERT}$ pulse width	CRC_ALERT_PW	6	10	TBD	TBD	nCK	
Geardown timing							
Exit RESET from CKE HIGH to a valid MRS geardown (T2/Reset)	t_{XPR_GEAR}	t_{XPR}		t_{XPR}			
CKE High Assert to Gear Down Enable time(T2/CKE)	t_{XS_GEAR}	t_{XS}		t_{XS}			
MRS command to Sync pulse time(T3)	t_{SYNC_GEAR}	t_{MOD}(min)+4nCK	-	t_{MOD}(min)+4nCK	-		27
Sync pulse to First valid command(T4)	t_{CMD_GEAR}	t_{MOD}		t_{MOD}			27
Geardown setup time	t_{GEAR_setup}	2	-	2	-	nCK	
Geardown hold time	t_{GEAR_hold}	2	-	2	-	nCK	
t_{REFI}							
t_{RFC1} (min)	2Gb	160	-	160	-	ns	
	4Gb	260	-	260	-	ns	
	8Gb	350	-	350	-	ns	
	16Gb	TBD	-	TBD	-	ns	
t_{RFC2} (min)	2Gb	110	-	110	-	ns	
	4Gb	160	-	160	-	ns	
	8Gb	260	-	260	-	ns	
	16Gb	TBD	-	TBD	-	ns	

Speed		DDR4-2666		DDR4-3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max		
t_{RFC4} (min)	2Gb	90	-	90	-	ns	
	4Gb	110	-	110	-	ns	
	8Gb	160	-	160	-	ns	
	16Gb	TBD	-	TBD	-	ns	

NOTE 1 Start of internal write transaction is defined as follows :

For BL8 (Fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL.

For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL.

For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL.

NOTE 2 A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled.

NOTE 3 Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.

NOTE 4 tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR/tCK to the next integer.

NOTE 5 WR in clock cycles as programmed in MR0.

NOTE 6 tREFI depends on TOPER.

NOTE 7 CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.

NOTE 8 For these parameters, the DDR4 SDRAM device supports tnPARAM[nCK]=RU{tPARAM[ns]/tCK(avg)[ns]}, which is in clock cycles assuming all inputclock jitter specifications are satisfied.

NOTE 9 When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.

NOTE 10 When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.

NOTE 11 When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.

NOTE 12 The max values are system dependent.

NOTE 13 DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are tbd.

NOTE 14 The deterministic component of the total timing. Measurement method tbd.

NOTE 15 DQ to DQ static offset relative to strobe per group. Measurement method tbd.

NOTE 16 This parameter will be characterized and guaranteed by design.

NOTE 17 When the device is operated with the input clock jitter, this parameter needs to be derated by the actual tjit(per)_total of the input clock. (output deratings are relative to the SDRAM input clock). Example tbd.

NOTE 18 DRAM DBI mode is off.

NOTE 19 DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.

NOTE 20 tQSL describes the instantaneous differential output low pulse width on DQS - $\overline{\text{DQS}}$, as measured from on falling edge to the next consecutive rising edge.

NOTE 21 tQSH describes the instantaneous differential output high pulse width on DQS - $\overline{\text{DQS}}$, as measured from on falling edge to the next consecutive rising edge.

NOTE 22 There is no maximum cycle time limit besides the need to satisfy the refresh interval tREFI.

NOTE 23 tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge .

NOTE 24 tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.

NOTE 25 Total jitter includes the sum of deterministic and random jitter terms for a specified BER. BER target and measurement method are tbd.

NOTE 26 The deterministic jitter component out of the total jitter. This parameter is characterized and gauranteed by design.

NOTE 27 This parameter has to be even number of clocks.

NOTE 28 When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.

NOTE 29 When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.

NOTE 30 When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.

NOTE 31 After CKE is registered LOW, CKE signal level shall be maintained below VILDC for tCKE specification (Low pulse width).

NOTE 32 After CKE is registered HIGH, CKE signal level shall be maintained above VIHDC for tCKE specification (

HIGH pulse width).

NOTE 33 Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.

NOTE 34 Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.

NOTE 35 This parameter must keep consistency with Speed-Bin Tables.

NOTE 36 DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.

NOTE 37 applied when DRAM is in DLL on mode.

NOTE 38 Assume no jitter on input clock signals to the DRAM

NOTE 39 Value is only valid for RONNOM =34 ohms

NOTE 40 1tCK toggle mode with setting MR4:A11 to 0

NOTE 41 2tCK toggle mode with setting MR4:A11 to 1, which is valid for DDR4-2400/2666 speed grade.

NOTE 42 1tCK mode with setting MR4:A12 to 0

NOTE 43 2tCK mode with setting MR4:A12 to 1, which is valid for DDR4-2400/2666 speed grade.

NOTE 44 The maximum read preamble is bounded by tLZ(DQS)min on the left side and tDQSCK(max) on the right side. See Clock to Data Strobe Relationship --- “Clock to Data Strobe Relationship”. Boundary of DQS Low-Z occur one cycle earlier in 2tCK toggle mode which is illustrated in Read Preamble ---- “Read Preamble”.

NOTE 45 DQ falling signal middle-point of transferring from High to Low to first rising edge of DQS diff-signal cross-point

NOTE 46 last falling of DQS diff-signal cross-point to DQ rising signal middle-point of transferring from Low to High

NOTE 47 VrefDQ value must be set to either its midpoint or Vcent_DQ(midpoint) in order to capture DQ0 or DQL0 low level for entering PDA mode.

NOTE 48 The maximun read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side. See Clock to Data Strobe Relationship

NOTE 49 Reference level of DQ output signal is specified with a midpoint as a widest part of Output signal eye which should be approximately 0.7*VDDQ as center level of the static signle-ended output peak-to-peak swing with a driver impedance of 34 ohms and an effective test load of 50 ohms to VTT =VDDQ

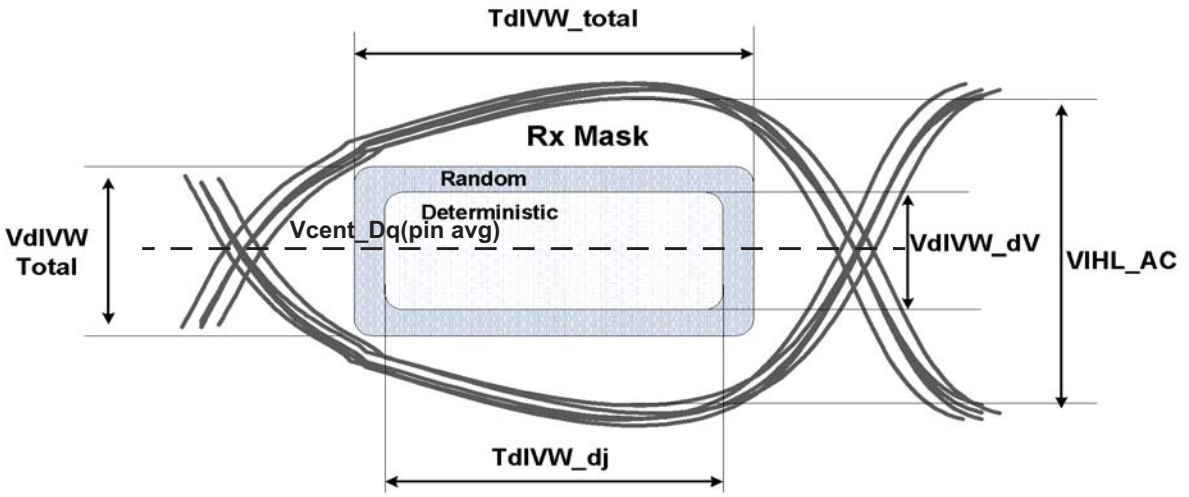
NOTE 50 For MR7 commands, the minimum delay to a subsequent non-MRS command is 5nCK.

UI=tCK(avg).min/2

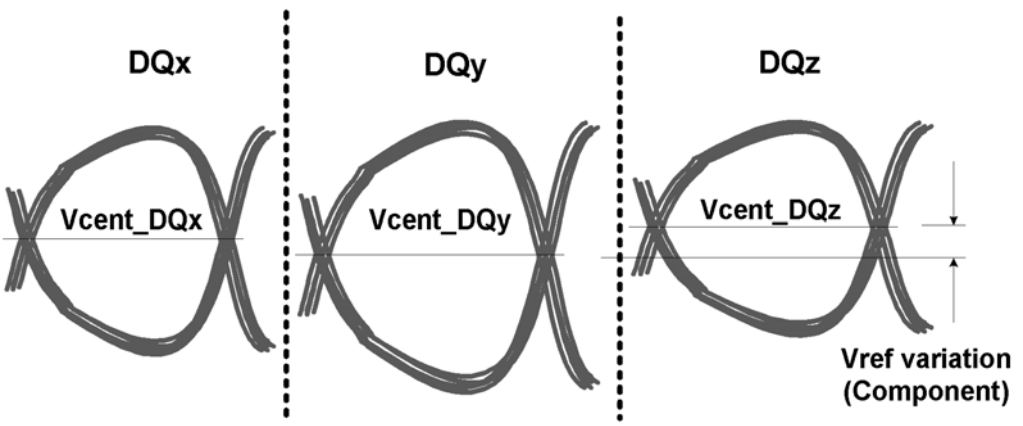
The DQ input receiver compliance mask for voltage and timing

The DQ input receiver compliance mask for voltage and timing is shown in the figure below. The receiver mask (Rx Mask) defines area the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal; it is not the valid data-eye.

DQ Receiver(Rx) compliance mask



Across pin Vref DQ voltage variation

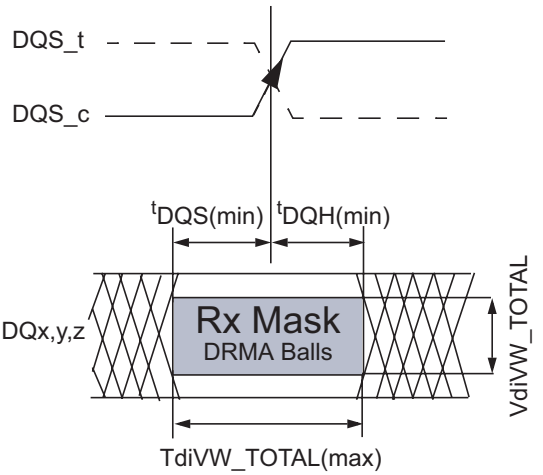


Vcent_DQ(pin avg) is defined as the midpoint between the largest Vref_DQ voltage level and the smallest Vref_DQ voltage level across all DQ pins for a given DRAM component. Each DQ pin Vref level is defined by the center, i.e. widest opening, of the cumulative data input eye as depicted in below.This clarifies that any DRAM component level variation must be accounted for within the DRAM Rx mask.The component level Vref will be set by the system to account for Ron and ODT settings.

DQ to DQS Timings at DRAM Balls

DQS, DQS Data-in at DRAM ball

Minimum Data-Eye / Maximum Rx Mask

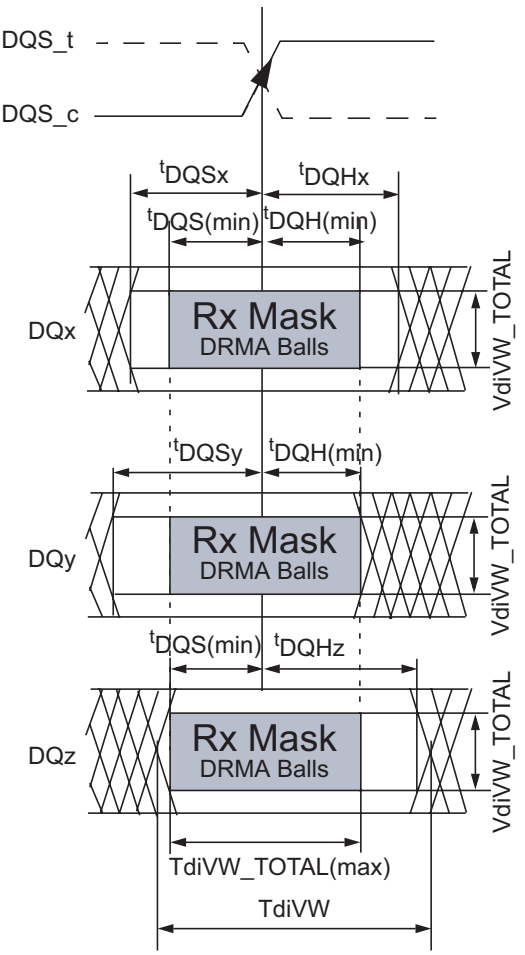


$$\frac{\text{TdiVW\_TOTAL(max)}}{2} = {}^{t}\text{DQS(min)}^{*} = {}^{t}\text{DQH(min)}^{*}$$

*NOTE: tDQS(min) and tDQH(min) are not new timing parameters, they are derived from the value of Tdivw_TOTAL(max)

DQS, DQS Data-in at DRAM ball

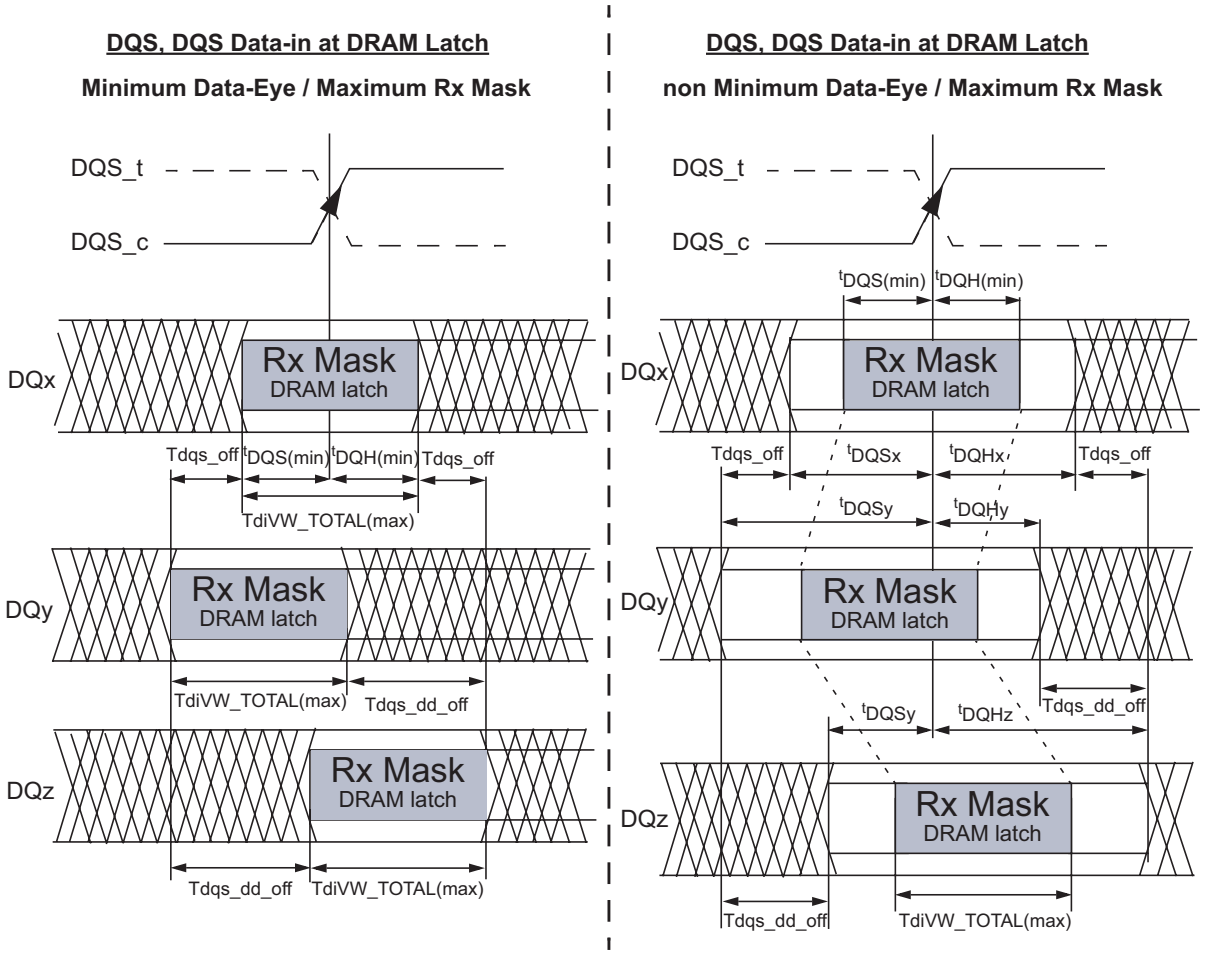
non Minimum Data-Eye / Maximum Rx Mask



NOTE: DQx represents an optimally centered input
DQy represents earliest valid transitioning input
DQz represents latest valid transitioning input

All of the timing terms in figure below are measured at the VdIVW_total voltage levels centered around Vcent_DQ(pin avg) and are referenced to the DQS/DQS center aligned to the DQ per pin.

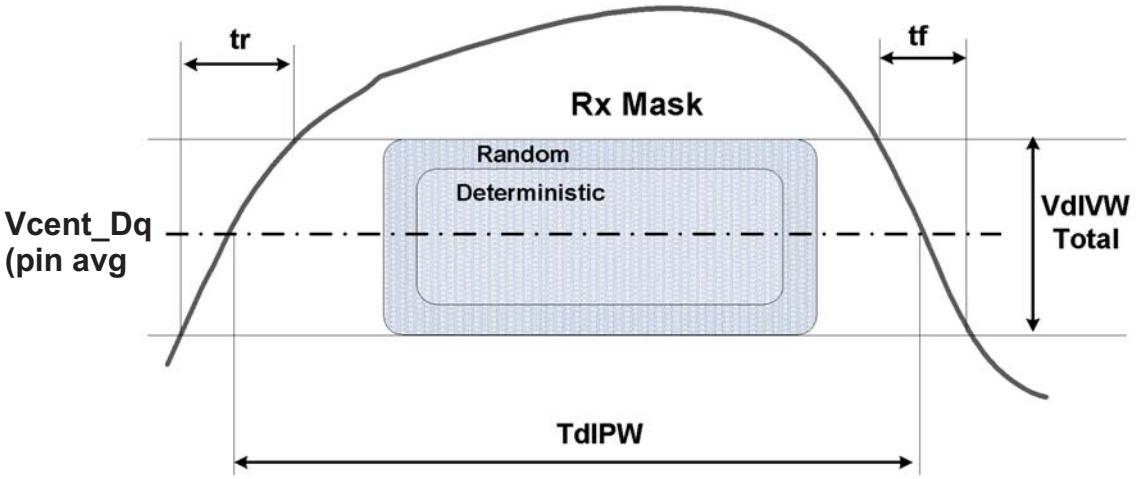
DQ to DQS Timings at DRAM latch



NOTE: DQx represents an optimally centered input
DQy represents earliest valid transitioning input
DQz represents latest valid transitioning input

All of the timing terms in figure below are measured at the VdIVW_total voltage levels centered around Vcent_DQ(pin avg) and are referenced to the DQS/$\overline{\text{DQS}}$ center aligned. Typical view assumes DQx, DQy, and DQz edges are aligned at DRAM balls.

DQ TdIPW and SRIN_dIVW definition (for each input pulse)



NOTE 1 SRIN_dIVW=VdIVW_Total/(tr or tf), signal must be monotonic within tr and tf range.

*DRAM DQs In Receive Mode ; * UI=tck(avg)min/2*

Symbol	Parameter	DDR4-2133		DDR4-2400		DDR4-2666/3200		Unit	NOTE
		min	max	min	max	min	max		
VdIVW_total	Rx Mask voltage - p-p tota	-	136 (note12)	-	130	-	120	mV	1,2,4,6
VdIVW_dV	Rx Mask voltage - deterministic	-	136	-	130	-	120	mV	1,5,13
TdIVW_total	Rx timing window total	-	0.2 (note12)	-	0.2	-	0.22	UI*	1,2,4,6
TdIVW_dj	Rx deterministic timing	-	0.2	-	0.2	-	0.22	UI*	1,5,13
VIHL_AC	DQ AC input swing pk-pk	186	-	160	-	150	-	mV	7
TdIPW	DQ input pulse width	0.58	TBD	0.58	-	0.58	-	UI*	8
Tdqs_off	DQ to DQS Setup offset	-	TBD	-	TBD	-	TBD	UI*	9
Tdqh_off	DQ to DQS Hold offset	-	TBD	-	TBD	-	TBD	UI*	9
Tdqs_dd_off	DQ to DQ Setup offset	-	TBD	-	TBD	-	TBD	UI*	10
Tdqh_dd_off	DQ to DQ Hold offset	-	TBD	-	TBD	-	TBD	UI*	10
SRIN_dIVW	Input Slew Rate over VdIVW_total	TBD	9	TBD	9	TBD	9	V/ns	11

NOTE 1 Data Rx mask voltage and timing total input valid window where VdIVW is centered around Vcent_DQ(pin avg). The data Rx mask is applied per bit and should include voltage and temperature drift terms. The design specification is BER <1e-16 and how this varies for lower BER is tbd. The BER will be characterized and extrapolated if necessary using a dual dirac method from a higher BER(tbd).
NOTE 2 Rx mask voltage AC swing peak-peak requirement over TdIVW_total with at least half of TdIVW_total(max) above Vcent_DQ(pin avg) and at least half of TdIVW_total(max) below Vcent_DQ(pin avg).
NOTE 3 Rx differential DQ to DQS jitter total timing window at the VdIVW voltage levels centered around Vcent_DQ(pin

avg).
NOTE 4 Defined over the DQ internal Vref range 1.
NOTE 5 Deterministic component of the total Rx mask voltage or timing. Parameter will be characterized and guaranteed by design. Measurement method tbd.
NOTE 6 Overshoot and Undershoot Specifications tbd.
NOTE 7 DQ input pulse signal swing into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level. VIHL AC is the peak to peak voltage centered around Vcent_DQ(pin avg).
NOTE 8 DQ minimum input pulse width defined at the Vcent_DQ(pin avg).
NOTE 9 DQ to DQS setup or hold offset defined within byte from DRAM ball to DRAM internal latch; tDQS and tDQH are the minimum DQ setup and hold per DQ pin; each is equal to one-half of TdIVW_total(max).
NOTE 10 DQ to DQ setup or hold delta offset within byte. Defined as the static difference in Tdqs_off(max) and Tdqs_off(min) or Tdqh(max) - Tdqh(min) for a given component, from DRAM ball to DRAM internal latch.
NOTE 11 Input slew rate over VdIVW Mask centered at Vcent_DQ(pin avg). Slowest DQ slew rate to fastest DQ slew rate per transition edge must be within tbd V/ns of each other.
NOTE 12 The total timing and voltage terms(tdIVW_total & VdIVWtotal) are valid for any BER lower {lower fail rate} than the spec.
NOTE 13 VdIVW_total - VdIVW_dV and TdIVW_total - TdIVW_dj define the difference between random and deterministic fail mask. When VdIVW_total - VdIVW_dV = 0 and TdIVW_total - TdIVW_dj = 0, random error is assumed to be zero.

DDR4 Function Matrix

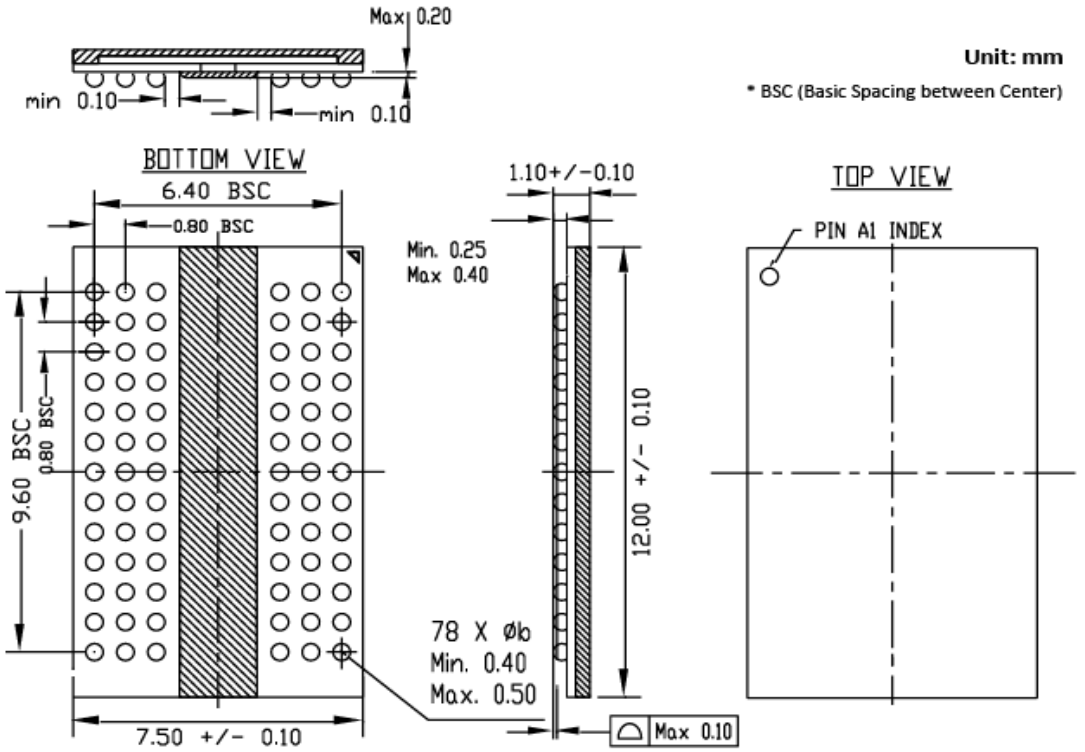
Function Matrix (By ORG. V: Supported, Blank: Not supported)

Functions	x4	x8	x16	NOTE
Write Leveling	V	V	V	
Temperature controlled Refresh	V	V	V	
Low Power Auto Self Refresh	V	V	V	
Fine Granularity Refresh	V	V	V	
Multi Purpose Register	V	V	V	
Data Mask		V	V	
Data Bus Inversion		V	V	
TDQS		V		
ZQ calibration	V	V	V	
DQ Vref Training	V	V	V	
Per DRAM Addressability	V	V		
Mode Register Readout	V	V	V	
CAL	V	V	V	
WRITE CRC	V	V	V	
CA Parity	V	V	V	
Control Gear Down Mode	V	V	V	
Programmable Preamble	V	V	V	
Maximum Power Down Mode	V	V		
Boundary Scan Mode			V	
Additive Latency	V	V	V	

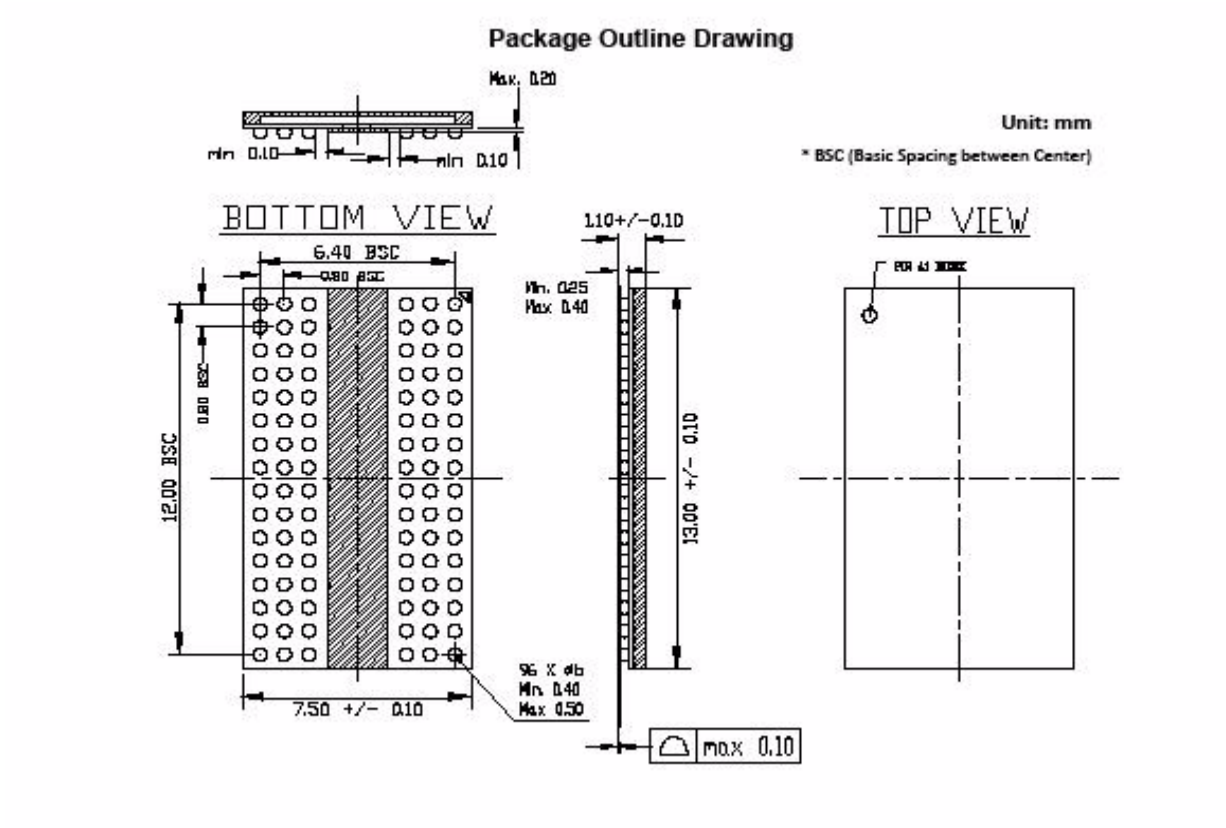
Function Matrix (By Speed. V: Supported, Blank: Not supported)

Functions	DDR4-2133	DDR4-2400	DDR4-2666/3200	NOTE
Write Leveling	V	V	V	
Temperature controlled Refresh	V	V	V	
Low Power Auto Self Refresh	V	V	V	
Fine Granularity Refresh	V	V	V	
Multi Purpose Register	V	V	V	
Data Mask	V	V	V	
Data Bus Inversion	V	V	V	
TDQS	V	V	V	
ZQ calibration	V	V	V	
DQ Vref Training	V	V	V	
Per DRAM Addressability	V	V		
Mode Register Readout	V	V	V	
CAL	V	V	V	
WRITE CRC			V	
CA Parity	V	V	V	
Control Gear Down Mode			V	
Programmable Preamble			V	
Maximum Power Down Mode	V	V	V	
Boundary Scan Mode	V	V	V	

Package Diagram (x8)
78-Ball Fine Pitch Ball Grid Array Outline



Package Diagram (x16)
96-Ball Fine Pitch Ball Grid Array Outline



Revision History

Revision No.	History	Draft Date	Remark
1.0	First release	April. 2019	

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