

	6	7
System Frequency (f_{CK})	166 MHz	143 MHz
Clock Cycle Time (t_{CK3})	6 ns	7 ns
Clock Access Time (t_{AC3}) \overline{CAS} Latency = 3	5.4 ns	5.4 ns
Clock Access Time (t_{AC2}) \overline{CAS} Latency = 2	5.4 ns	6 ns

Features

- 4 banks x 4Mbit x 16 organization
- 4 banks x 8Mbit x 8 organization
- High speed data transfer rates up to 166 MHz
- Full Synchronous Dynamic RAM, with all signals referenced to clock rising edge
- Single Pulsed \overline{RAS} Interface
- Data Mask for Read/Write Control
- Four Banks controlled by BA0 & BA1
- Programmable \overline{CAS} Latency: 2, 3
- Programmable Wrap Sequence: Sequential or Interleave
- Programmable Burst Length:
1, 2, 4, 8 and full page for Sequential Type
1, 2, 4, 8 for Interleave Type
- Multiple Burst Read with Single Write Operation
- Automatic and Controlled Precharge Command
- Random Column Address every CLK (1-N Rule)
- Power Down Mode
- Auto Refresh and Self Refresh
- Refresh Interval: 8192 cycles/64 ms
- Available in 54 Pin TSOP II and 54 Ball FBGA (x16 only)
- LVTTTL Interface
- Single +3.3 V ± 0.3 V Power Supply

Description

The D54C3256(16/80)4VJ is a four bank Synchronous DRAM organized as 4 banks x 4Mbit x 16, or 4 banks x 8Mbit x 8. The D54C3256(16/80)4VJ achieves high speed data transfer rates up to 166 MHz by employing a chip architecture that prefetches multiple bits and then synchronizes the output data to a system clock.

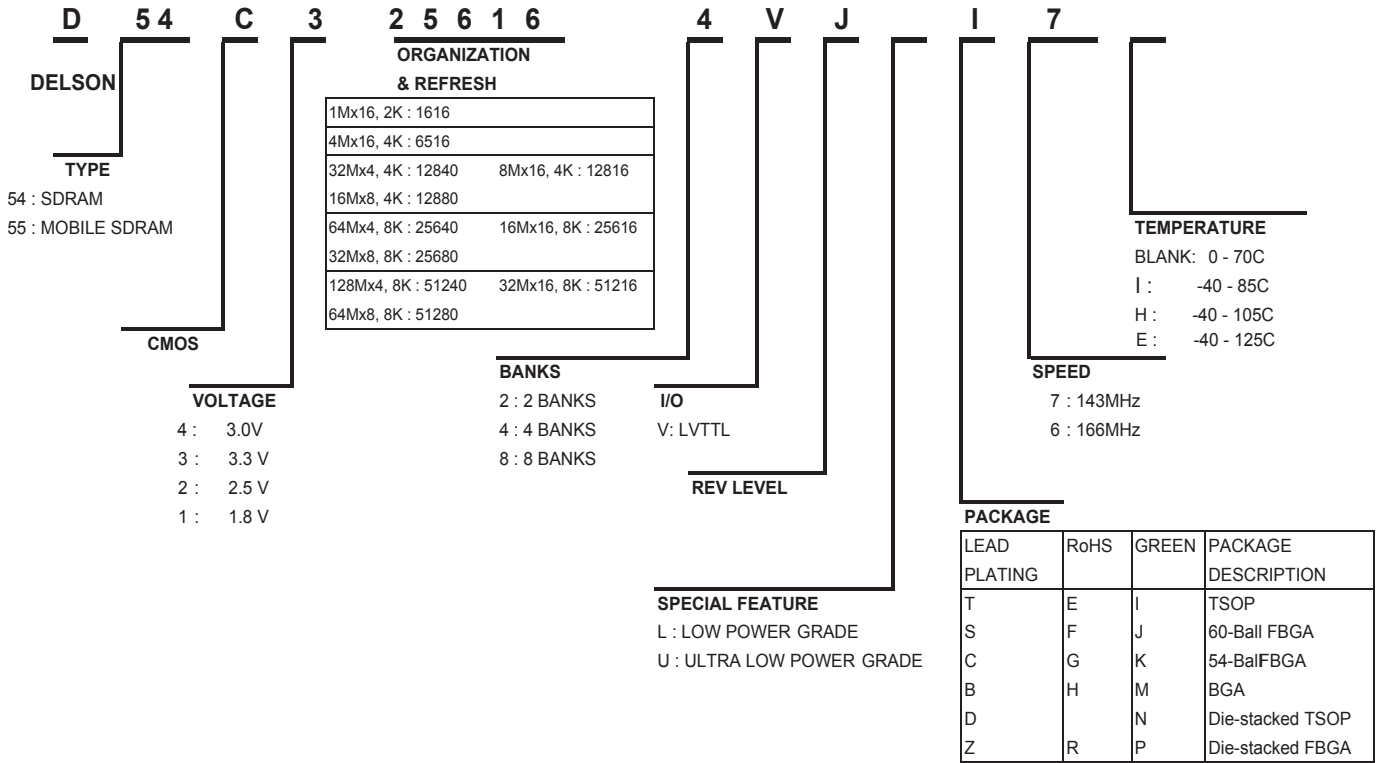
All of the control, address, data input and output circuits are synchronized with the positive edge of an externally supplied clock.

Operating the four memory banks in an interleaved fashion allows random access operation to occur at higher rate than is possible with standard DRAMs. A sequential and gapless data rate of up to 166 MHz is possible depending on burst length, \overline{CAS} latency and speed grade of the device.

Device Usage Chart

Operating Temperature Range	Package Outline	Access Time (ns)		Power	Temperature Mark
	I	6	7	Std.	
0°C to 70°C	•	•	•	•	Blank
-40°C to 85°C	•	•	•	•	I

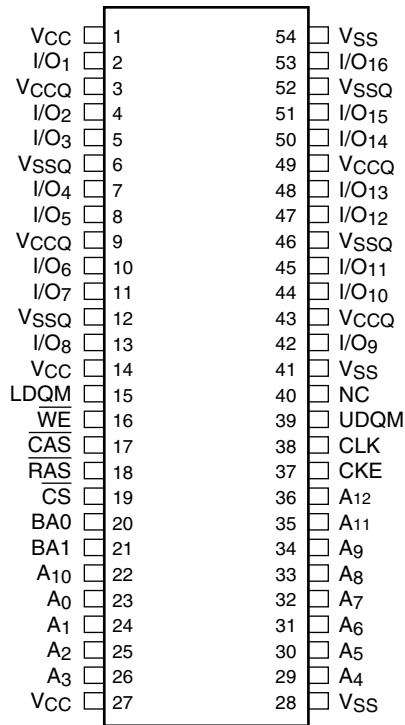
Part Number Information



* RoHS: Restriction of Hazardous Substances

Description	Pkg.	Pin Count
TSOP-II	I	54

**54 Pin Plastic TSOP-II
x16 PIN CONFIGURATION
Top View**



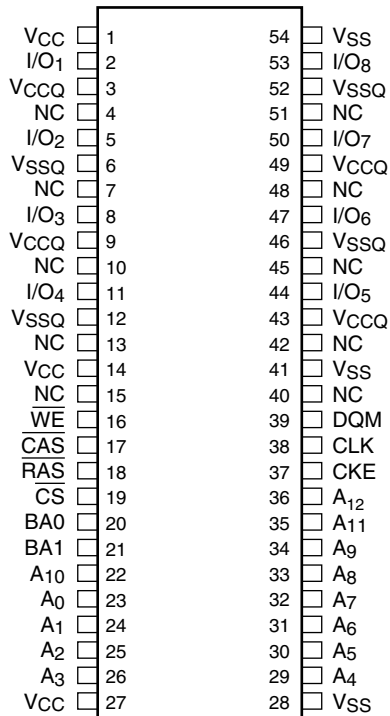
356164V-01

Pin Names

CLK	Clock Input
CKE	Clock Enable
\overline{CS}	Chip Select
\overline{RAS}	Row Address Strobe
\overline{CAS}	Column Address Strobe
\overline{WE}	Write Enable
A ₀ -A ₁₂	Address Inputs
BA ₀ , BA ₁	Bank Select
I/O ₁ -I/O ₁₆	Data Input/Output
LDQM, UDQM	Data Mask
V _{CC}	Power (+3.0V~3.3V)
V _{SS}	Ground
V _{CCQ}	Power for I/O's (+3.0V~3.3V)
V _{SSQ}	Ground for I/O's
NC	Not connected

Description	Pkg.	Pin Count
TSOP-II	I	54

**54 Pin Plastic TSOP-II
x8 PIN CONFIGURATION
Top View**



356804V-01

Pin Names

CLK	Clock Input
CKE	Clock Enable
\overline{CS}	Chip Select
\overline{RAS}	Row Address Strobe
\overline{CAS}	Column Address Strobe
\overline{WE}	Write Enable
A ₀ -A ₁₂	Address Inputs
BA0, BA1	Bank Select
I/O ₁ -I/O ₈	Data Input/Output
DQM	Data Mask
V _{CC}	Power (+3.0V~3.3V)
V _{SS}	Ground
V _{CCQ}	Power for I/O's (+3.0V~3.3V)
V _{SSQ}	Ground for I/O's
NC	Not connected

Description	Pkg.	Pin Count
FBGA	K	54

**54 BALL FBGA
x16 PIN CONFIGURATION
Top View**

1	2	3		7	8	9
VSS	DQ15	VSSQ	A	VDDQ	DQ0	VDD
DQ14	DQ13	VDDQ	B	VSSQ	DQ2	DQ1
DQ12	DQ11	VSSQ	C	VDDQ	DQ4	DQ3
DQ10	DQ9	VDDQ	D	VSSQ	DQ6	DQ5
DQ8	NC	VSS	E	VDD	LDQM	DQ7
UDQM	CLK	CKE	F	$\overline{\text{CAS}}$	$\overline{\text{RAS}}$	$\overline{\text{WE}}$
A12	A11	A9	G	BA0	BA1	$\overline{\text{CS}}$
A8	A7	A6	H	A0	A1	A10
VSS	A5	A4	J	A3	A2	VDD

Pin Names

CLK	Clock Input
CKE	Clock Enable
$\overline{\text{CS}}$	Chip Select
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{WE}}$	Write Enable
A ₀ -A ₁₂	Address Inputs
BA0, BA1	Bank Select
DQ ₀ -DQ ₁₅	Data Input/Output
LDQM, UDQM	Data Mask
V _{CC}	Power (+3.0V~3.3V)
V _{SS}	Ground
V _{CCQ}	Power for I/O's (+3.0V~3.3V)
V _{SSQ}	Ground for I/O's
NC	Not connected

< Top-view >

Capacitance*

$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $f = 1\text{ Mhz}$

Symbol	Parameter	Max.	Unit
C _{I1}	Input Capacitance (A0 to A12)	5	pF
C _{I2}	Input Capacitance RAS, CAS, WE, CS, CLK, CKE, DQM	5	pF
C _{IO}	Output Capacitance (I/O)	6.5	pF
C _{CLK}	Input Capacitance (CLK)	4	pF

*Note: Capacitance is sampled and not 100% tested.

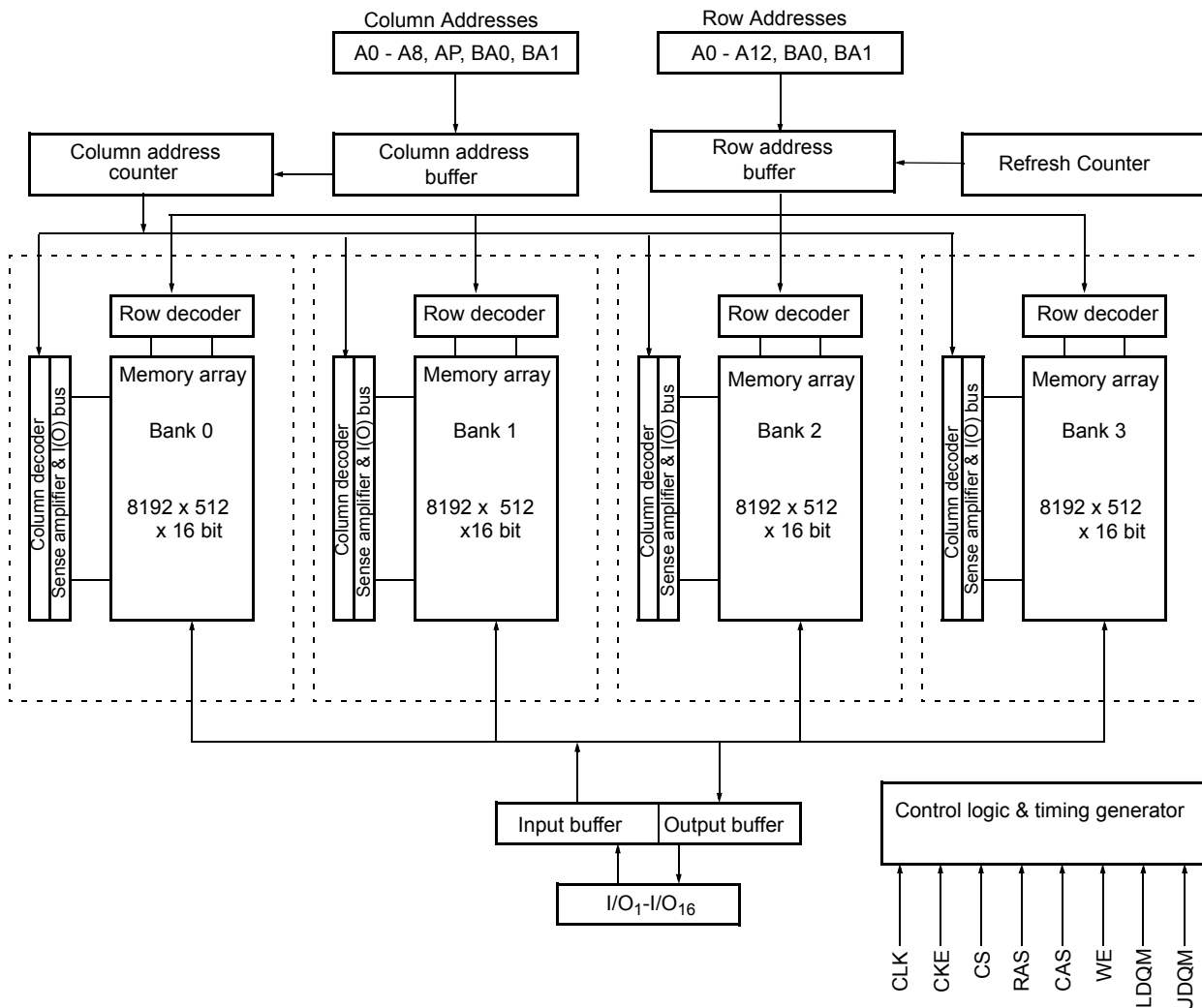
Absolute Maximum Ratings*

Operating temperature range 0 to 70 °C for normal
 -40 to 85 °C for Industrial
 Storage temperature range -55 to 150 °C
 Input/output voltage -0.3 to (V_{CC}+0.3) V
 Power supply voltage -0.3 to 4.6 V
 Power dissipation 1 W
 Data out current (short circuit) 50 mA

*Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

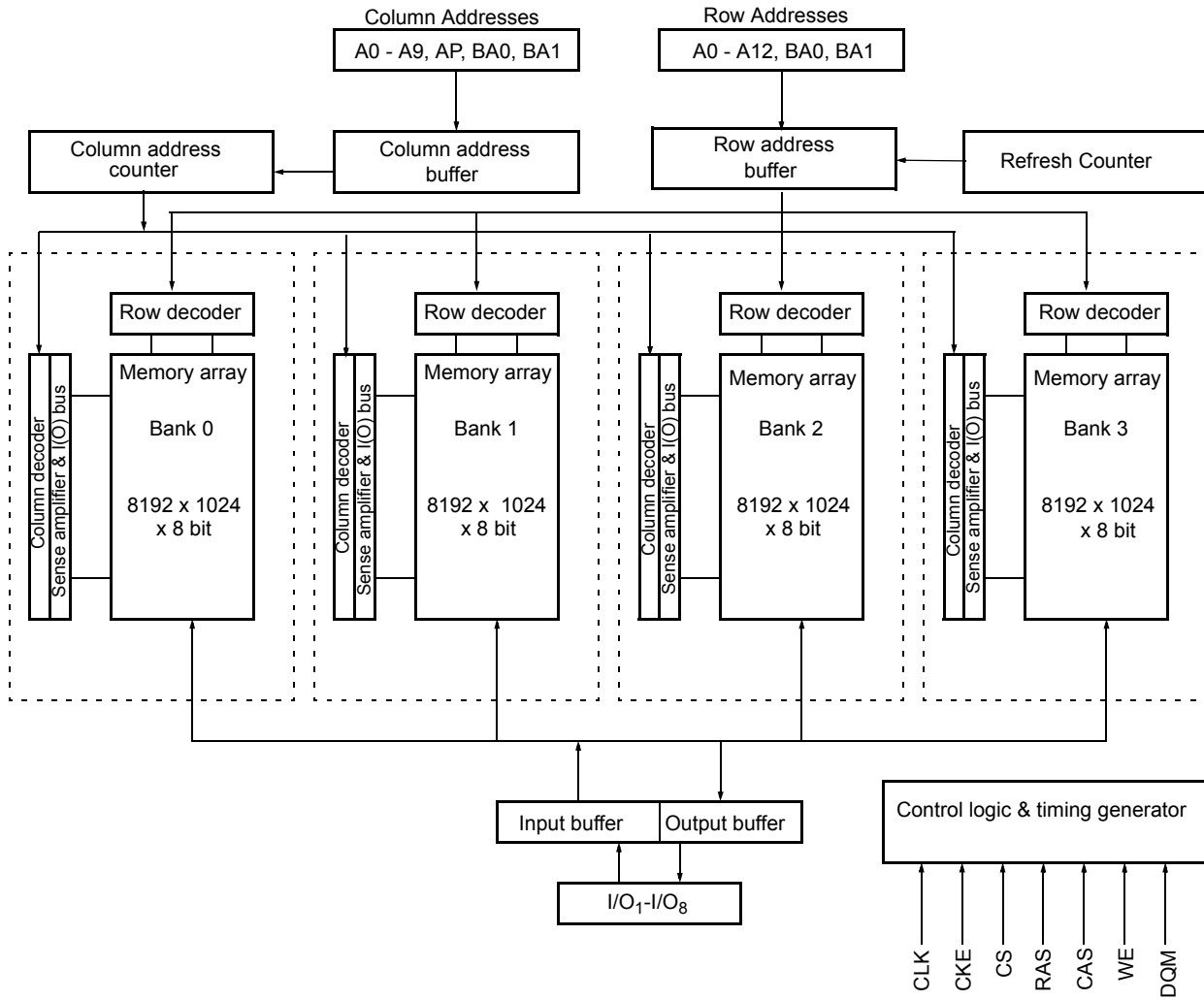
Block Diagram

x16 Configuration



Block Diagram

x8 Configuration



Signal Pin Description

Pin	Type	Signal	Polarity	Function
CLK	Input	Pulse	Positive Edge	The system clock input. All of the SDRAM inputs are sampled on the rising edge of the clock.
CKE	Input	Level	Active High	Activates the CLK signal when high and deactivates the CLK signal when low, thereby initiates either the Power Down mode or the Self Refresh mode.
\overline{CS}	Input	Pulse	Active Low	\overline{CS} enables the command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
\overline{RAS} , \overline{CAS} , \overline{WE}	Input	Pulse	Active Low	When sampled at the positive rising edge of the clock, \overline{CAS} , \overline{RAS} , and \overline{WE} define the command to be executed by the SDRAM.
A0 - A12	Input	Level	—	<p>During a Bank Activate command cycle, A0-A12 defines the row address (RA0-RA12) when sampled at the rising clock edge.</p> <p>During a Read or Write command cycle, A0-An defines the column address (CA0-CAn) when sampled at the rising clock edge. CAn depends from the SDRAM organization:</p> <ul style="list-style-type: none"> • 32M x 8 SDRAM CA0–CA9. • 16M x 16 SDRAM CA0–CA8. <p>In addition to the column address, A10(=AP) is used to invoke autoprecharge operation at the end of the burst read or write cycle. If A10 is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If A10 is low, autoprecharge is disabled. During a Precharge command cycle, A10(=AP) is used in conjunction with BA0 and BA1 to control which bank(s) to precharge. If A10 is high, all four banks will BA0 and BA1 are used to define which bank to precharge.</p>
BA0, BA1	Input	Level	—	Selects which bank is to be active.
DQx	Input Output	Level	—	Data Input/Output pins operate in the same manner as on conventional DRAMs.
LDQM UDQM	Input	Pulse	Active High	The Data Input/Output mask places the DQ buffers in a high impedance state when sampled high. In Read mode, DQM has a latency of two clock cycles and controls the output buffers like an output enable. In Write mode, DQM has a latency of zero and operates as a word mask by allowing input data to be written if it is low but blocks the write operation if DQM is high.
VCC, VSS	Supply			Power and ground for the input buffers and the core logic.
VCCQ VSSQ	Supply	—	—	Isolated power supply and ground for the output buffers to provide improved noise immunity.

Operation Definition

All of SDRAM operations are defined by states of control signals \overline{CS} , \overline{RAS} , \overline{CAS} , \overline{WE} , and DQM at the positive edge of the clock. The following list shows the thruth table for the operation commands.

Operation	Device State	CKE n-1	CKE n	\overline{CS}	\overline{RAS}	\overline{CAS}	\overline{WE}	DQM	A0-9, A11, A12	A10	BS0 BS1
Row Activate	Idle ³	H	X	L	L	H	H	X	V	V	V
Read	Active ³	H	X	L	H	L	H	X	V	L	V
Read w/Autoprecharge	Active ³	H	X	L	H	L	H	X	V	H	V
Write	Active ³	H	X	L	H	L	L	X	V	L	V
Write with Autoprecharge	Active ³	H	X	L	H	L	L	X	V	H	V
Row Precharge	Any	H	X	L	L	H	L	X	X	L	V
Precharge All	Any	H	X	L	L	H	L	X	X	H	X
Mode Register Set	Idle	H	X	L	L	L	L	X	V	V	V
No Operation	Any	H	X	L	H	H	H	X	X	X	X
Device Deselect	Any	H	X	H	X	X	X	X	X	X	X
Auto Refresh	Idle	H	H	L	L	L	H	X	X	X	X
Self Refresh Entry	Idle	H	L	L	L	L	H	X	X	X	X
Self Refresh Exit	Idle (Self Refr.)	L	H	H	X	X	X	X	X	X	X
				L	H	H	X				
Power Down Entry	Idle Active ⁴	H	L	H	X	X	X	X	X	X	X
				L	H	H	X				
Power Down Exit	Any (Power Down)	L	H	H	X	X	X	X	X	X	X
				L	H	H	L				
Data Write/Output Enable	Active	H	X	X	X	X	X	L	X	X	X
Data Write/Output Disable	Active	H	X	X	X	X	X	H	X	X	X

Notes:

1. V = Valid , x = Don't Care, L = Low Level, H = High Level
2. CKEn signal is input level when commands are provided, CKEn-1 signal is input level one clock before the commands are provided.
3. These are state of bank designated by BS0, BS1 signals.
4. Power Down Mode can not entry in the burst cycle.

Power On and Initialization

The default power on state of the mode register is supplier specific and may be undefined. The following power on and initialization sequence guarantees the device is preconditioned to each users specific needs. Like a conventional DRAM, the Synchronous DRAM must be powered up and initialized in a predefined manner. During power on, all VCC and VCCQ pins must be built up simultaneously to the specified voltage when the input signals are held in the "NOP" state. The power on voltage must not exceed $VCC+0.3V$ on any of the input pins or VCC supplies. The CLK signal must be started at the same time. After power on, an initial pause of 200 ms is required followed by a precharge of both banks using the precharge command. To prevent data contention on the DQ bus during power on, it is required that the DQM and CKE pins be held high during the initial pause period. Once all banks have been precharged, the Mode Register Set Command must be issued to initialize the Mode Register. A minimum of eight Auto Refresh cycles (CBR) are also required. These may be done before or after programming the Mode Register. Failure to follow these steps may lead to unpredictable start-up modes.

Programming the Mode Register

The Mode register designates the operation mode at the read or write cycle. This register is divided into 4 fields. A Burst Length Field to set the length of the burst, an Addressing Selection bit to program the column access sequence in a burst cycle (interleaved or sequential), a CAS Latency Field to set the access time at clock cycle and a Operation mode field to differentiate between normal operation (Burst read and burst Write) and a special Burst Read and Single Write mode. The mode set operation must be done before any activate command after the initial power up. Any content of the mode register can be altered by re-executing the

mode set command. All banks must be in pre-charged state and CKE must be high at least one clock before the mode set operation. After the mode register is set, a Standby or NOP command is required. Low signals of RAS, CAS, and WE at the positive edge of the clock activate the mode set operation. Address input data at this timing defines parameters to be set as shown in the previous table.

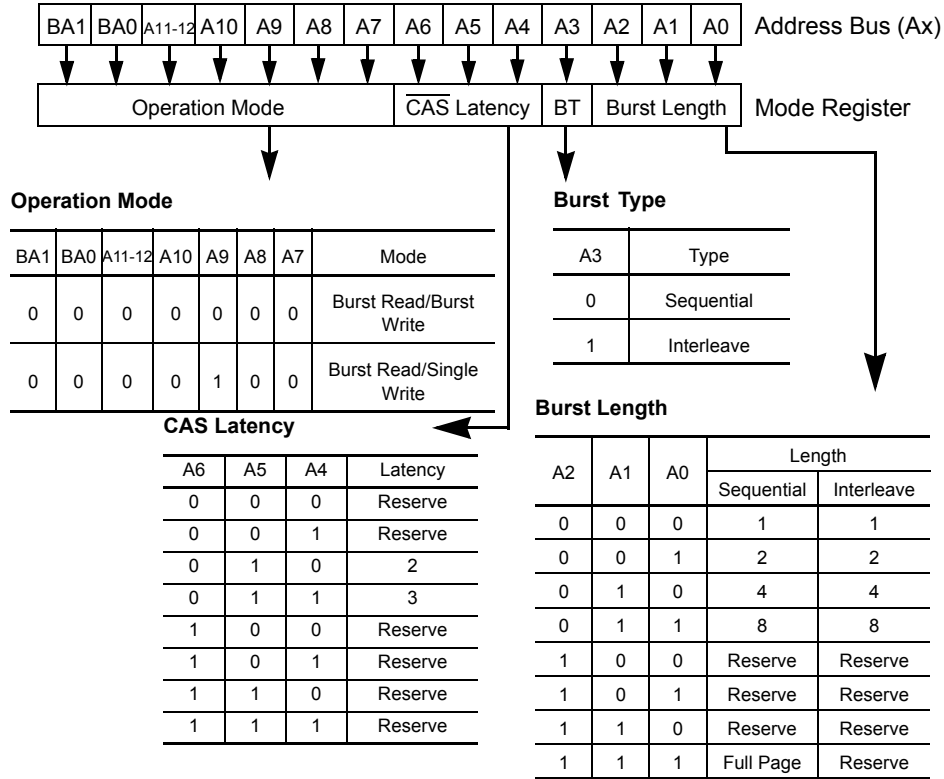
Read and Write Operation

When \overline{RAS} is low and both \overline{CAS} and \overline{WE} are high at the positive edge of the clock, a RAS cycle starts. According to address data, a word line of the selected bank is activated and all of sense amplifiers associated to the wordline are set. A CAS cycle is triggered by setting \overline{RAS} high and \overline{CAS} low at a clock timing after a necessary delay, t_{RCD} , from the \overline{RAS} timing. \overline{WE} is used to define either a read ($\overline{WE} = H$) or a write ($\overline{WE} = L$) at this stage.

SDRAM provides a wide variety of fast access modes. In a single CAS cycle, serial data read or write operations are allowed at up to a 125 MHz data rate. The numbers of serial data bits are the burst length programmed at the mode set operation, i.e., one of 1, 2, 4, 8 and full page. Column addresses are segmented by the burst length and serial data accesses are done within this boundary. The first column address to be accessed is supplied at the CAS timing and the subsequent addresses are generated automatically by the programmed burst length and its sequence. For example, in a burst length of 8 with interleave sequence, if the first address is '2', then the rest of the burst sequence is 3, 0, 1, 6, 7, 4, and 5.

Full page burst operation is only possible using sequential burst type. Full Page burst operation does not terminate once the burst length has been reached. (At the end of the page, it will wrap to the start address and continue.) In other words, unlike burst length of 2, 4, and 8, full page burst continues until it is terminated using another command.

Address Input for Mode Set (Mode Register Operation)



Similar to the page mode of conventional DRAM's, burst read or write accesses on any column address are possible once the RAS cycle latches the sense amplifiers. The maximum t_{RAS} or the refresh interval time limits the number of random column accesses. A new burst access can be done even before the previous burst ends. The interrupt operation at every clock cycles is supported. When the previous burst is interrupted, the remaining addresses are overridden by the new address with the full burst length. An interrupt which accompanies with an operation change from a read to a write is possible by exploiting DQM to avoid bus contention.

When two or more banks are activated sequentially, interleaved bank read or write operations are possible. With the programmed burst length, alternate access and precharge operations on two or more banks can realize fast serial data access modes among many different pages. Once two or more banks are activated, column to column interleave operation can be done between different pages.

